AMD Xilinx - XA3S200A-4FTG256I Datasheet

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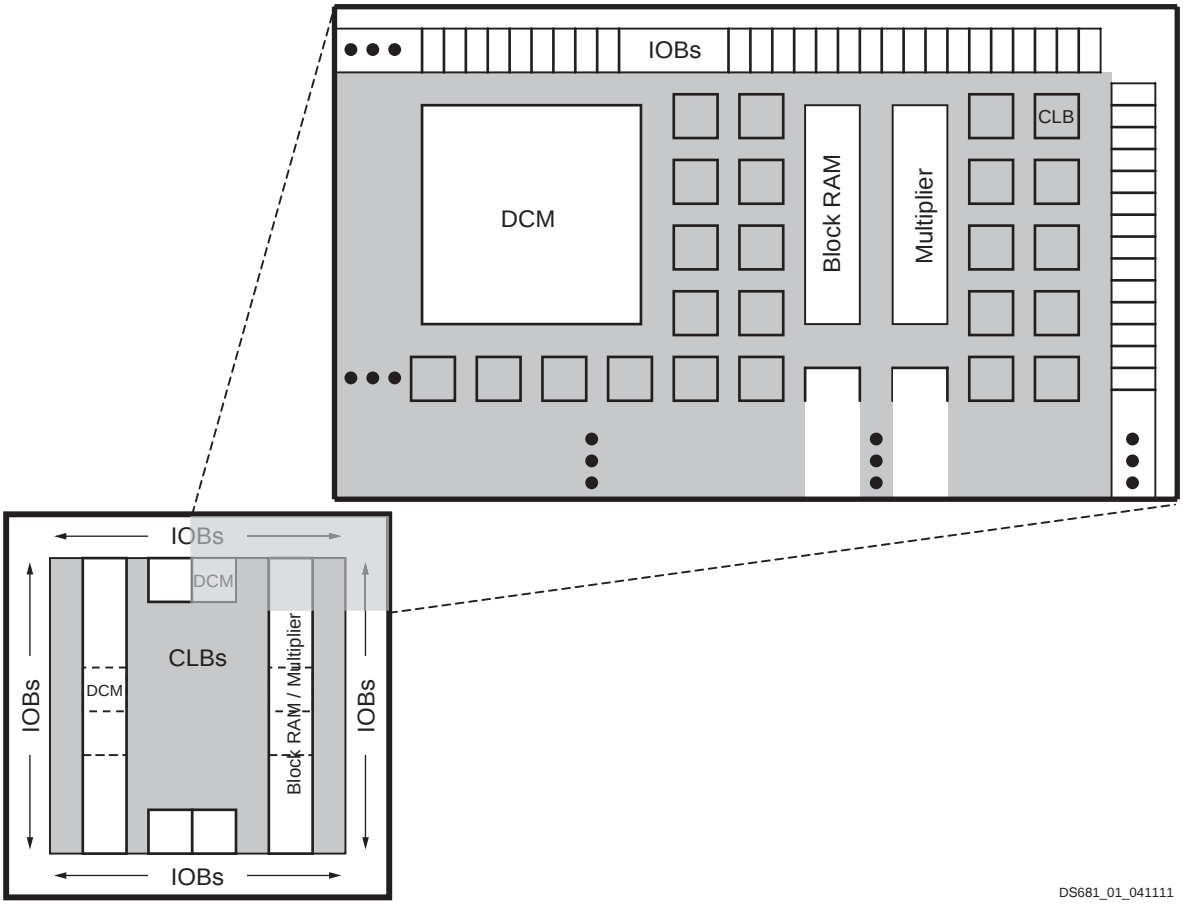
Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	448
Number of Logic Elements/Cells	4032
Total RAM Bits	294912
Number of I/O	195
Number of Gates	200000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3s200a-4ftg256i



Notes:

1. The XA3S700A and XA3S1400A have two additional DCMs on both the left and right sides as indicated by the dashed lines.

Figure 1: XA Spartan-3A Family Architecture

Configuration

XA Spartan-3A FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a SPI serial Flash or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes:

- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Additionally, each XA Spartan-3A FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

Table 12: DC Characteristics of User I/Os Using Single-Ended Standards

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL[3]	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24[6]	–24		
LVCMOS33[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16[6]		
	24[4]	24	–24[6]		
LVCMOS25[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16[4]	16	–16[6]		
	24[4]	24[6]	–24[6]		
LVCMOS18[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6[6]		
	8	8	–8		
	12[4]	12	–12[6]		
	16[4]	16	–16		
LVCMOS15[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8[4]	8	–8		
	12[4]	12	–12		
LVCMOS12[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4[4]	4	–4		
	6[4]	6	–6		
PCI33_3[5]		1.5	–0.5	10% V_{CCO}	90% V_{CCO}

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

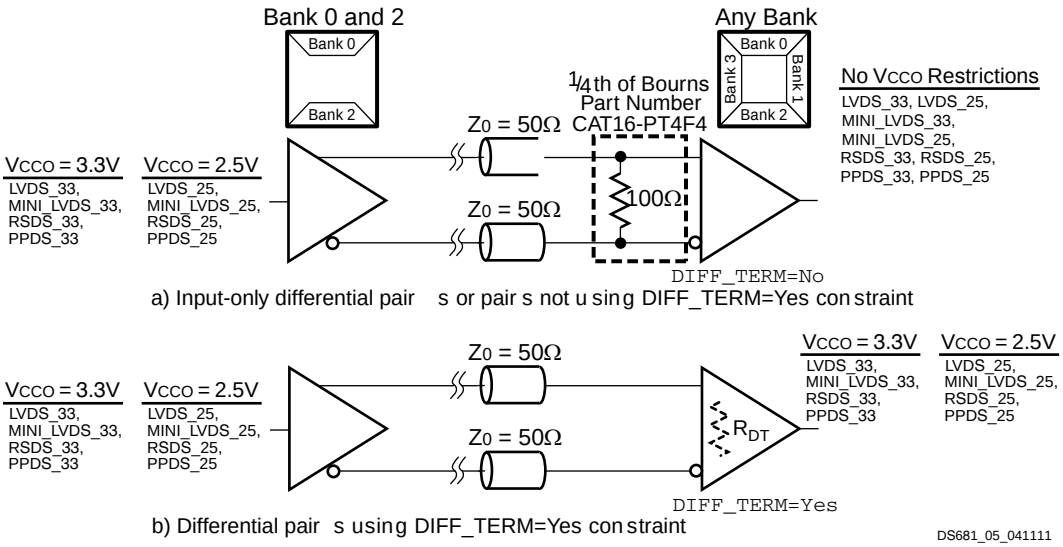


Figure 6: External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

BLVDS_25 I/O Standard

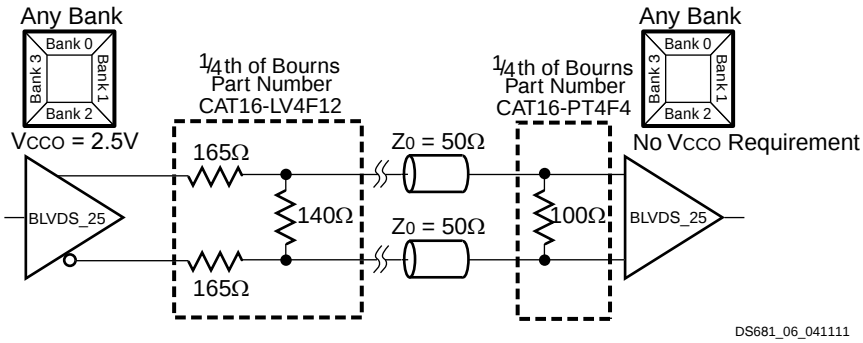


Figure 7: External Termination Resistors for BLVDS_25 I/O Standard

TMDS_33 I/O Standard

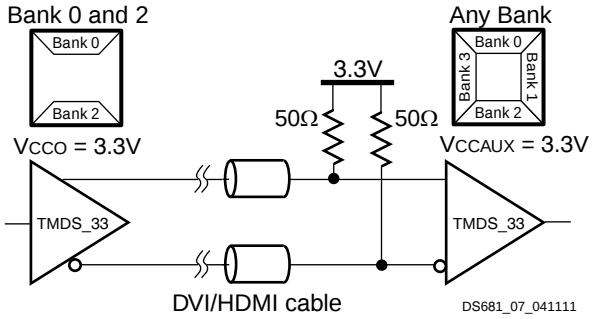


Figure 8: External Input Resistors Required for TMDS_33 I/O Standard

Input Propagation Times

Table 21: Propagation Times for the IOB Input Path

Symbol	Descripti on	Conditions	IFD_ DELAY_ VALUE	Device	Speed Grade: -4	Units
					Max	
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25[(2)]	0	XA3S200A	2.04	ns
				XA3S400A	1.74	ns
				XA3S700A	1.74	ns
				XA3S1400A	1.97	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25[(2)]	1	XA3S200A	2.43	ns
			2		3.16	ns
			3		4.01	ns
			4		4.60	ns
			5		4.43	ns
			6		5.46	ns
			7		6.33	ns
			8		6.94	ns
			1	XA3S400A	2.25	ns
			2		2.90	ns
			3		3.66	ns
			4		4.19	ns
			5		4.18	ns
			6		5.03	ns
			7		5.88	ns
			8		6.42	ns
			1	XA3S700A	2.18	ns
			2		3.06	ns
			3		3.95	ns
			4		4.54	ns
			5		4.37	ns
			6		5.42	ns
			7		6.33	ns
			8		6.96	ns
			1	XA3S1400A	2.40	ns
			2		3.15	ns
			3		3.99	ns
			4		4.55	ns
			5		4.42	ns
			6		5.32	ns
			7		6.21	ns
			8		6.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 22.

Table 25: Output Timing Adjustments for IOB ***(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below	Units
			Speed Grade: -4	
LVCMOS15	Slow	2 mA	6.42	ns
		4 mA	3.97	ns
		6 mA	3.21	ns
		8 mA	2.53	ns
		12 mA	2.06	ns
	Fast	2 mA	5.83	ns
		4 mA	3.05	ns
		6 mA	1.95	ns
		8 mA	1.60	ns
		12 mA	1.30	ns
	QuietIO	2 mA	34.11	ns
		4 mA	25.66	ns
		6 mA	24.64	ns
		8 mA	22.06	ns
		12 mA	20.64	ns
LVCMOS12	Slow	2 mA	7.14	ns
		4 mA	4.87	ns
		6 mA	5.67	ns
	Fast	2 mA	6.77	ns
		4 mA	5.02	ns
		6 mA	4.09	ns
	QuietIO	2 mA	50.76	ns
		4 mA	43.17	ns
		6 mA	37.31	ns
PCI33_3			0.34	ns
HSTL_I			0.86	ns
HSTL_III			1.16	ns
HSTL_I_18			0.35	ns
HSTL_II_18			0.30	ns
HSTL_III_18			0.47	ns
SSTL18_I			0.40	ns
SSTL18_II			0.30	ns
SSTL2_I			0	ns
SSTL2_II			–0.05	ns
SSTL3_I			0	ns
SSTL3_II			0.17	ns

Table 25: Output Timing Adjustments for IOB ***(Cont'd)***

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	Speed Grade: -4	
Differential Standards		
LVDS_25	1.50	ns
LVDS_33	0.47	ns
BLVDS_25	0.11	ns
MINI_LVDS_25	1.11	ns
MINI_LVDS_33	0.41	ns
LVPECL_25	Input Only	
LVPECL_33	Input Only	
RSDS_25	1.73	ns
RSDS_33	0.64	ns
TMDS_33	0.07	ns
PPDS_25	1.28	ns
PPDS_33	0.88	ns
DIFF_HSTL_I_18	0.43	ns
DIFF_HSTL_II_18	0.41	ns
DIFF_HSTL_III_18	0.36	ns
DIFF_HSTL_I	1.01	ns
DIFF_HSTL_III	1.16	ns
DIFF_SSTL18_I	0.49	ns
DIFF_SSTL18_II	0.41	ns
DIFF_SSTL2_I	0.91	ns
DIFF_SSTL2_II	0.11	ns
DIFF_SSTL3_I	1.18	ns
DIFF_SSTL3_II	0.28	ns

Notes:

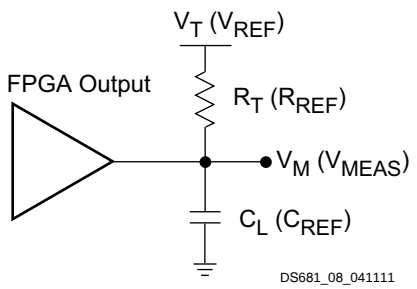
1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert output- and three-state-path times originally specified for the LVCMOS25 standard with 12 mA drive and Fast slew rate to times that correspond to other signal standards. Do not adjust times that measure when outputs go into a high-impedance state.

Timing Measurem ent Methodology

When measuring timing parameters at the programmable I/Os, different signal standards call for different test conditions. Table 26 lists the conditions to use for each standard.

The method for measuring Input timing is as follows: A signal that swings between a Low logic level of V_L and a High logic level of V_H is applied to the Input under test. Some standards also require the application of a bias voltage to the V_{REF} pins of a given bank to properly set the input-switching threshold. The measurement point of the Input signal (V_M) is commonly located halfway between V_L and V_H.

The Output test setup is shown in Figure 9. A termination voltage V_T is applied to the termination resistor R_T, the other end of which is connected to the Output. For each standard, R_T and V_T generally take on the standard values recommended for minimizing signal reflections. If the standard does not ordinarily use terminations (for example, LVCMOS, LVTTL), then R_T is set to 1 M : to indicate an open connection, and V_T is set to zero. The same measurement point (V_M) that was used at the Input is also used at the Output.



Notes:

1. The names shown in parentheses are used in the IBIS file.

Figure 9: Output Test Setup

Table 30: CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Clock-to-Output Times				
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	2.01	ns
Setup Times				
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.59	–	ns
Hold Times				
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	–	ns

Table 31: CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Clock-to-Output Times				
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.82	ns
Setup Times				
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.18	–	ns
Hold Times				
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	–	ns

Clock Buffer/Multiplexer Switching Characteristics

Table 32: Clock Distribution Switching Characteristics

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
T_{GIO}	Global clock buffer (BUFG, BUFGMUX, BUFGCE) I input to O-output delay	–	0.23	ns
T_{GSI}	Global clock multiplexer (BUFGMUX) select S-input setup to I0 and I1 inputs. Same as BUFGCE enable CE-input	–	0.63	ns
F_{BUFG}	Frequency of signals distributed on global buffers (all sides)	0	333	MHz

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 8.

18 x 18 Embedded Multiplier Timing

Table 33: 18 x 18 Embedded Multiplier Timing

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Combinatorial Delay				
T_{MULT}	Combinational multiplier propagation delay from the A and B inputs to the P outputs, assuming 18-bit inputs and a 36-bit product (AREG, BREG, and PREG registers unused)	–	4.88	ns
Clock-to-Output Times				
T_{MSCKP_P}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using the PREG register(2,3)	–	1.30	ns
T_{MSCKP_A} T_{MSCKP_B}	Clock-to-output delay from the active transition of the CLK input to valid data appearing on the P outputs when using either the AREG or BREG register(2,4)	–	4.97	ns
Setup Times				
T_{MSDCK_P}	Data setup time at the A or B input before the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(3)	3.98	–	ns
T_{MSDCK_A}	Data setup time at the A input before the active transition at the CLK when using the AREG input register(4)	0.00	–	ns
T_{MSDCK_B}	Data setup time at the B input before the active transition at the CLK when using the BREG input register(4)	0.00	–	ns
Hold Times				
T_{MSCKD_P}	Data hold time at the A or B input after the active transition at the CLK when using only the PREG output register (AREG, BREG registers unused)(3)	0.00	–	ns
T_{MSCKD_A}	Data hold time at the A input after the active transition at the CLK when using the AREG input register(4)	0.45	–	ns
T_{MSCKD_B}	Data hold time at the B input after the active transition at the CLK when using the BREG input register(4)	0.45	–	ns
Clock Frequency				
F_{MULT}	Internal operating frequency for a two-stage 18x18 multiplier using the AREG and BREG input registers and the PREG output register(1)	0	250	MHz

Notes:
1. Combinational delay is less and pipelined performance is higher when multiplying input data with less than 18 bits.
2. The PREG register is typically used in both single-stage and two-stage pipelined multiplier implementations.
3. The PREG register is typically used when inferring a single-stage multiplier.
4. Input registers AREG or BREG are typically used when inferring a two-stage multiplier.
5. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 36: Switching Characteristics for the DLL

Symbol	Description		Device	Speed Grade: -4		Units
				Min	Max	
Output Frequency Ranges						
CLKOUT_FREQ_CLK0	Frequency for the CLK0 and CLK180 outputs		All	5	250	MHz
CLKOUT_FREQ_CLK90	Frequency for the CLK90 and CLK270 outputs			5	200	MHz
CLKOUT_FREQ_2X	Frequency for the CLK2X and CLK2X180 outputs			10	334	MHz
CLKOUT_FREQ_DV	Frequency for the CLKDV output			0.3125	166	MHz
Output Clock Jitter (2,3,4)						
CLKOUT_PER_JITT_0	Period jitter at the CLK0 output		All	–	±100	ps
CLKOUT_PER_JITT_90	Period jitter at the CLK90 output			–	±150	ps
CLKOUT_PER_JITT_180	Period jitter at the CLK180 output			–	±150	ps
CLKOUT_PER_JITT_270	Period jitter at the CLK270 output			–	±150	ps
CLKOUT_PER_JITT_2X	Period jitter at the CLK2X and CLK2X180 outputs			–	±[0.5% of CLKIN period + 100]	ps
CLKOUT_PER_JITT_DV1	Period jitter at the CLKDV output when performing integer division			–	±150	ps
CLKOUT_PER_JITT_DV2	Period jitter at the CLKDV output when performing non-integer division			–	±[0.5% of CLKIN period + 100]	ps
Duty Cycle (4)						
CLKOUT_DUTY_CYCLE_DLL	Duty cycle variation for the CLK0, CLK90, CLK180, CLK270, CLK2X, CLK2X180, and CLKDV outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKIN period + 350]	ps
Phase Alignment (4)						
CLKIN_CLKFB_PHASE	Phase offset between the CLKIN and CLKFB inputs		All	–	±150	ps
CLKOUT_PHASE_DLL	Phase offset between DLL outputs	CLK0 to CLK2X (not CLK2X180)		–	±[1% of CLKIN period + 100]	ps
		All others		–	±[1% of CLKIN period + 150]	ps
Lock Time						
LOCK_DLL(3)	When using the DLL alone: The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. When the DCM is locked, the CLKIN and CLKFB signals are in phase	5 MHz dF$_{CLKIN}$ d 15 MHz	All	–	5	ms
		F$_{CLKIN}$! 15 MHz		–	600	P^{3}s
Delay Lines						
DCM_DELAY_STEP(5)	Finest delay resolution, averaged over all steps		All	15	35	ps

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 35.
2. Indicates the maximum amount of output jitter that the DCM adds to the jitter on the CLKIN input.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Some jitter and duty-cycle specifications include 1% of input clock period or 0.01 UI. For example, the data sheet specifies a maximum jitter of "±[1% of CLKIN period + 150]". Assume the CLKIN frequency is 100 MHz. The equivalent CLKIN period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 150 ps] = ±250ps.
5. The typical delay step size is 23 ps.

Digital Frequency Synthesizer

Table 37: Recommended Operating Conditions for the DFS

Symbol		Description		Speed Grade: -4		Units
				Min	Max	
Input Frequency Ranges (2)						
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333	MHz
Input Clock Ji tter Tolerance (3)						
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	F_{CLKFX} d150 MHz	–	±300	ps
CLKIN_CYC_JITT_FX_HF			F_{CLKFX} ! 150 MHz	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 35.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Table 38: Switching Characteristics for the DFS

Symbol	Description		Device	Speed Grade: -4		Units
				Min	Max	
Output Frequency Ranges						
CLKOUT_FREQ_FX(2)	Frequency for the CLKFX and CLKFX180 outputs		All	5	320	MHz
Output Clock Jitter (3,4)						
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	CLKIN d20 MHz	All	Typ	Max	ps
				Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip		
		CLKIN ! 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle (5,6)						
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	ps
Phase Alignment (6)						
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	ps

Table 38: Switching Characteristics for the DFS ***(Cont'd)***

Symbol	Description		Device	Speed Grade: -4		Units
				Min	Max	
Lock Time						
LOCK_FX[2,3]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz dF$_{CLKIN}$ d15 MHz	All	–	5	ms
		F$_{CLKIN}$! 15 MHz		–	450	ps

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 37.
2. DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Maximum output jitter is characterized within a reasonable noise environment (40 SSOs and 25% CLB switching) on an FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of "±[1% of CLKFX period + 200]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Phase Shifter

Table 39: Recommended Operating Conditions for the PS in Variable Phase Mode

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Operating Frequency Ranges				
PSCLK_FREQ (F$_{PSCLK}$)	Frequency for the PSCLK input	1	167	MHz
Input Pulse Requirements				
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	–

Table 40: Switching Characteristics for the PS in Variable Phase Mode

Symbol	Description		Phase Shift Amount	Units
Phase Shifting Range				
MAX_STEPS[2]	Maximum allowed number of DCM_DELAY_STEP[3] steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	CLKIN 60 MHz	r[INTEGER(10 x(T$_{CLKIN}$ – 3 ns))]	steps
		CLKIN t 60 MHz	r[INTEGER(15 x(T$_{CLKIN}$ – 3 ns))]	
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting		r[MAX_STEPS x DCM_DELAY_STEP_MIN]	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting		r[MAX_STEPS x DCM_DELAY_STEP_MAX]	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 39.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 36.

Suspend Mode Timing

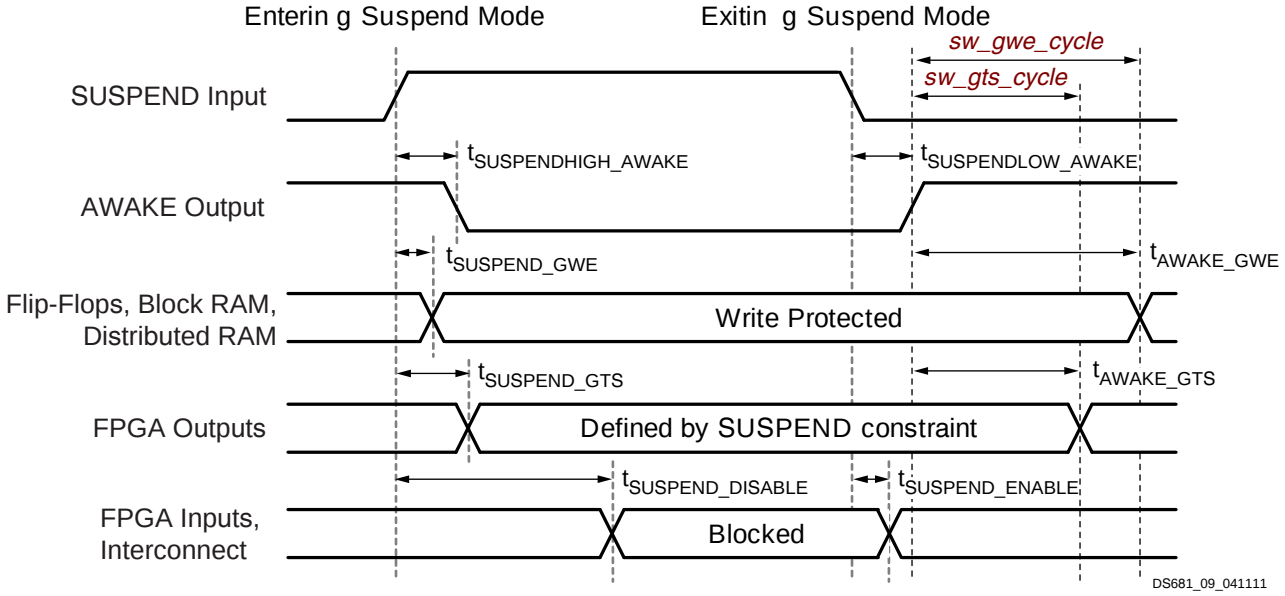


Figure 10: Suspend Mode Timing

Table 43: Suspend Mode Timing Parameters

Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{SUSPENDHIGH_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***)	–	7	–	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***)	+160	+300	+600	ns
$T_{SUSPEND_GTS}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–	ns
$T_{SUSPEND_GWE}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	<5	–	ns
$T_{SUSPEND_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–	ns
Exiting Suspend Mode					
$T_{SUSPENDLOW_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.	–	4 to 108	–	µs
$T_{SUSPEND_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1***.	–	67	–	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512***.	–	14	–	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1***.	–	57	–	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512***.	–	14	–	µs

Notes:
1. These parameters based on characterization.
2. For information on using the Spartan-3A Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

Table 54: Configuration Timing Requirements for Attached Parallel NOR Flash

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	T_{CE} d $T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	T_{OE} d $T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	T_{ACC} d 50%$T_{CCLKn\ min} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time[(3)]	T_{BYTE} d $T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.