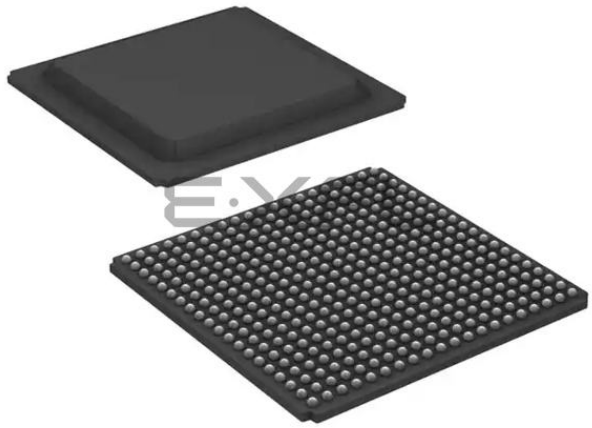

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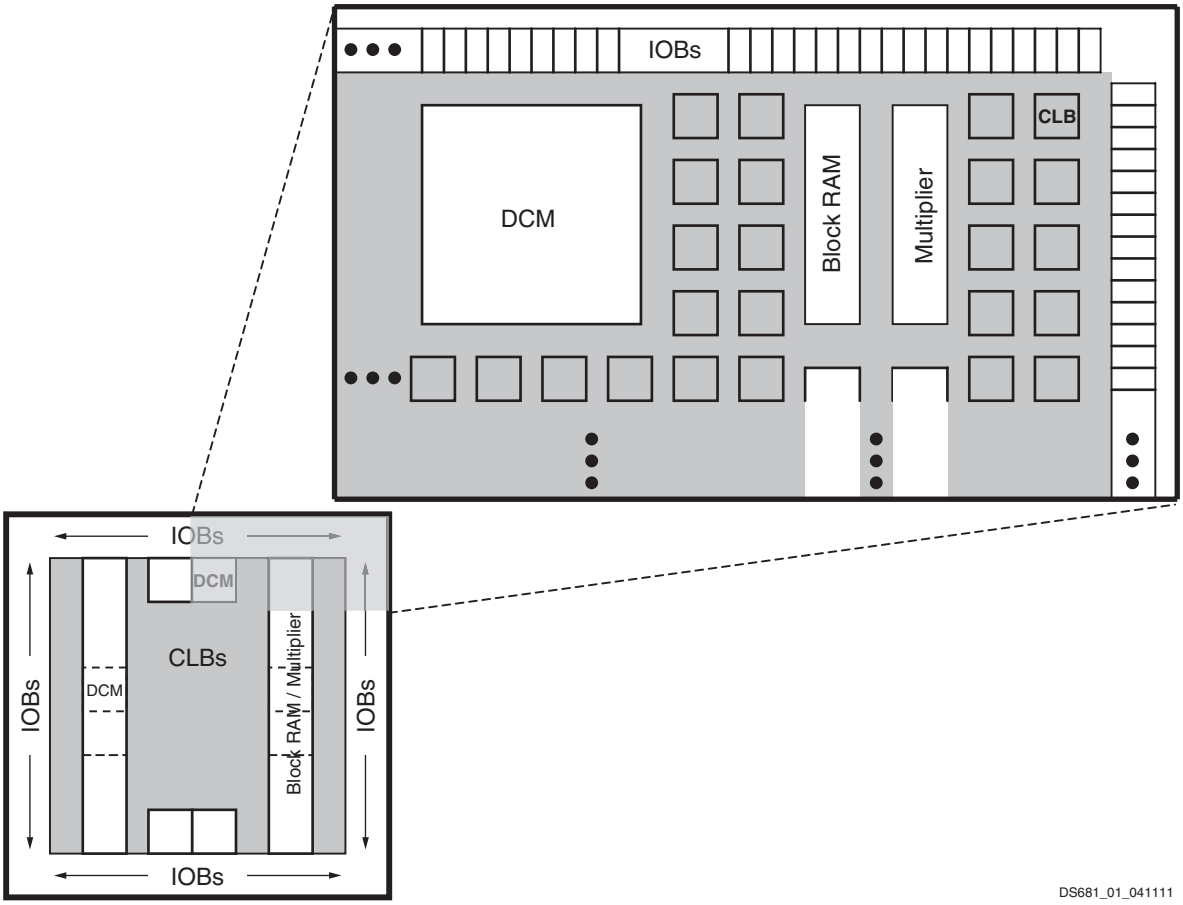
Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	368640
Number of I/O	311
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 125°C (TJ)
Package / Case	400-BGA
Supplier Device Package	400-FBGA (21x21)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3s400a-4fgg400q



Notes:

1. The XA3S700A and XA3S1400A have two additional DCMs on both the left and right sides as indicated by the dashed lines.

Figure 1: **XA Spartan-3A Family Architecture**

Configuration

XA Spartan-3A FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a SPI serial Flash or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes:

- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Additionally, each XA Spartan-3A FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

Quiescent Current Requirements

Table 10: **Quiescent Supply Current Characteristics**

Symbol	Description	Device	Typical[2]	I-Grade Maximum[2]	Q-Grade Maximum[2]	Units
I_{CCINTQ}	Quiescent V_{CCINT} supply current	XA3S200A	7	70	110	mA
		XA3S400A	10	125	230	mA
		XA3S700A	13	185	330	mA
		XA3S1400A	24	310	580	mA
I_{CCOQ}	Quiescent V_{CCO} supply current	XA3S200A	0.2	3	4	mA
		XA3S400A	0.3	4	5	mA
		XA3S700A	0.3	4	5	mA
		XA3S1400A	0.3	4	5	mA
I_{CCAUXQ}	Quiescent V_{CCAUX} supply current	XA3S200A	5	15	20	mA
		XA3S400A	5	24	40	mA
		XA3S700A	6	34	60	mA
		XA3S1400A	10	58	95	mA

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8.
2. Quiescent supply current is measured with all I/O drivers in a high-impedance state and with all pull-up/pull-down resistors at the I/O pads disabled. Typical values are characterized using typical devices at room temperature (T_J of 25°C at V_{CCINT} = 1.2V, V_{CCO} = 3.3V, and V_{CCAUX} = 2.5V). The maximum limits are tested for each device at the respective maximum specified junction temperature and at maximum voltage limits with V_{CCINT} = 1.26V, V_{CCO} = 3.6V, and V_{CCAUX} = 3.6V. The FPGA is programmed with a "blank" configuration data file (that is, a design with no functional elements instantiated). For conditions other than those described above (for example, a design including functional elements), measured quiescent current levels will be different than the values in the table.
3. There are two recommended ways to estimate the total power consumption (quiescent plus dynamic) for a specific design: a) The Spartan-3A FPGA XPower Estimator provides quick, approximate, typical estimates, and does not require a netlist of the design. b) XPower Analyzer uses a netlist as input to provide maximum estimates as well as more accurate typical estimates.
4. The maximum numbers in this table indicate the minimum current each power rail requires in order for the FPGA to power-on successfully.
5. For information on the power-saving Suspend mode, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*. Suspend mode typically saves 40% total power consumption compared to quiescent current.

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL[3]	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24[6]	–24		
LVCMOS33[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16[6]		
	24[4]	24	–24[6]		
LVCMOS25[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16[4]	16	–16[6]		
	24[4]	24[6]	–24[6]		
LVCMOS18[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6[6]		
	8	8	–8		
	12[4]	12	–12[6]		
	16[4]	16	–16		
LVCMOS15[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8[4]	8	–8		
	12[4]	12	–12		
LVCMOS12[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4[4]	4	–4		
	6[4]	6	–6		
PCI33_3[5]		1.5	–0.5	10% V_{CCO}	90% V_{CCO}

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
HSTL_I(4)	8	–8	0.4	V_{CCO} – 0.4
HSTL_III(4)	24(7)	–8	0.4	V_{CCO} – 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} – 0.4
HSTL_II_18(4)	16	–16(7)	0.4	V_{CCO} – 0.4
HSTL_III_18	24(7)	–8	0.4	V_{CCO} – 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II(4)	13.4	–13.4	V_{TT} – 0.475	V_{TT} + 0.475
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II(4)	16.2	–16.2	V_{TT} – 0.80	V_{TT} + 0.80
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 11.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} — the output current condition under which V_{OL} is tested
   I_{OH} — the output current condition under which V_{OH} is tested
   V_{OL} — the output voltage that indicates a Low logic level
   V_{OH} — the output voltage that indicates a High logic level
   V_{IL} — the input voltage that indicates a Low logic level
   V_{IH} — the input voltage that indicates a High logic level
   V_{CCO} — the supply voltage for output drivers
   V_{REF} — the reference voltage for setting the input switching threshold
   V_{TT} — the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
4. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
5. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see http://www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics, but no PCI-X IP is supported.
6. DE-RATE by 20% for T_J above 100°C
7. DE-RATE by 5% for T_J above 100°C

Differential I/O Standards

Differential Input Pairs

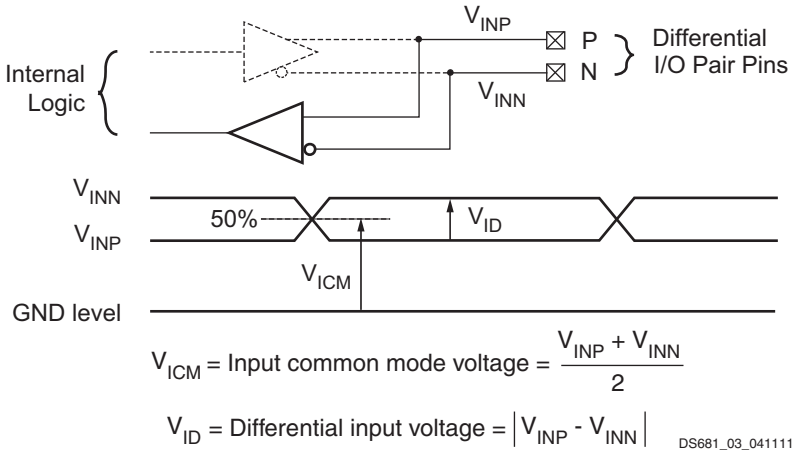


Figure 4: **Differential Input Voltages**

Differential Output Pairs

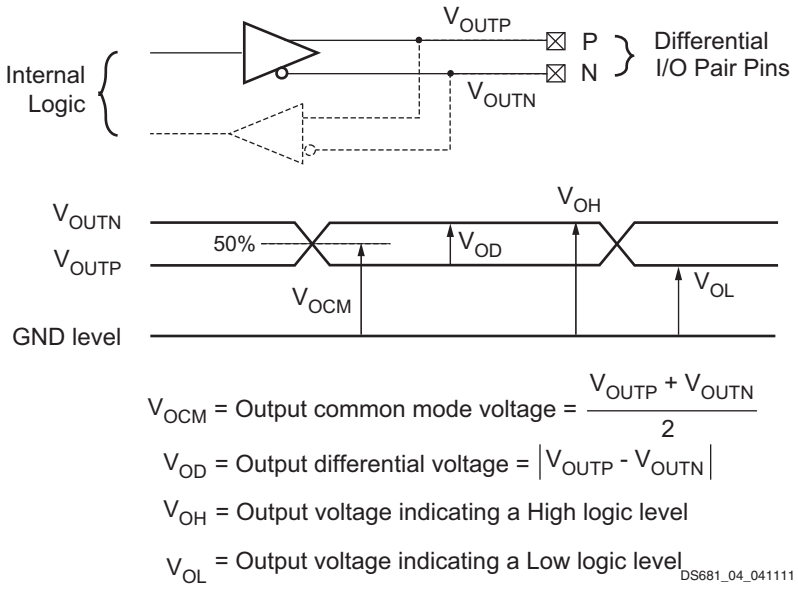


Figure 5: **Differential Output Voltages**

Table 14: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	–	1.375	–	–
LVDS_33	247	350	454	1.125	–	1.375	–	–
BLVDS_25	240	350	460	–	1.30	–	–	–
MINI_LVDS_25	300	–	600	1.0	–	1.4	–	–
MINI_LVDS_33	300	–	600	1.0	–	1.4	–	–
RSDS_25	100	–	400	1.0	–	1.4	–	–
RSDS_33	100	–	400	1.0	–	1.4	–	–
TMDS_33	400	–	800	V_{CCO} – 0.405	–	V_{CCO} – 0.190	–	–
PPDS_25	100	–	400	0.5	0.8	1.4	–	–
PPDS_33	100	–	400	0.5	0.8	1.4	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL18_II	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL2_I	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	–	–	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL3_I	–	–	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL3_II	–	–	–	–	–	–	V_{TT} + 0.8	V_{TT} – 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 13.
2. See External Termination Requirements for Differential I/O, page 16.
3. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when V_{CCO}=2.5V, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when V_{CCO} = 3.3V

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

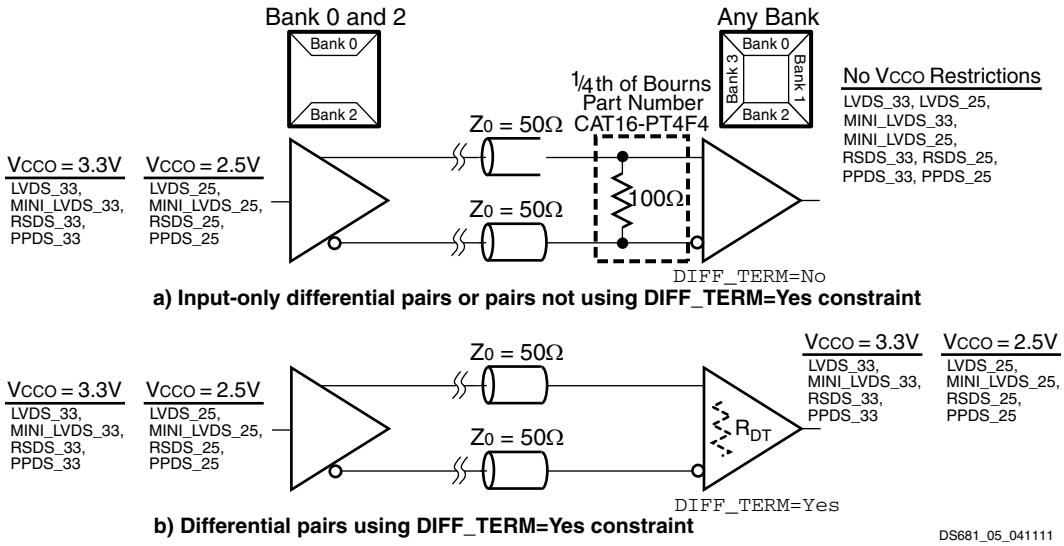


Figure 6: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

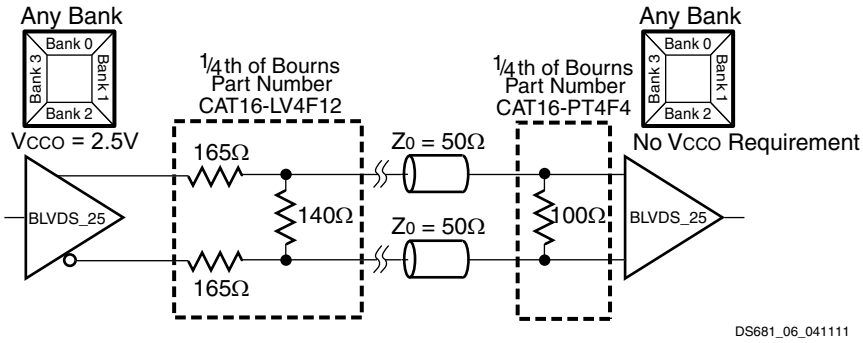


Figure 7: **External Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

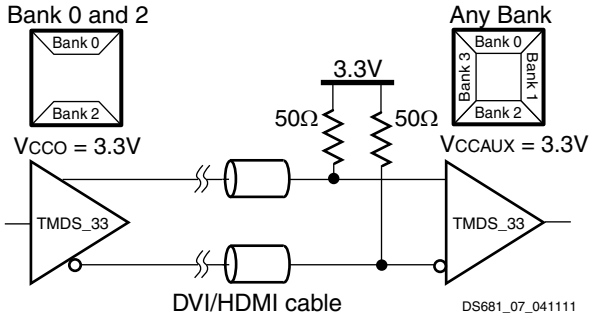


Figure 8: **External Input Resistors Required for TMDS_33 I/O Standard**

Device DNA Data Retention, Read Endurance

Table 15: **Device DNA Identifier Memory Characteristics**

Symbol	Description	Minimum	Units
DNA_CYCLES	Number of READ operations or JTAG ISC_DNA read operations. Unaffected by HOLD or SHIFT operations.	30,000,000	Read cycles

Switching Characteristics

All XA Spartan-3A FPGAs ship in the -4 speed grade. Switching characteristics in this document are designated as Production as shown in Table 16.

Production: These specifications are approved once enough production silicon of a particular device family member has been characterized to provide full correlation between speed files and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes.

Software Version Requirements

Production-quality systems must use FPGA designs compiled using a speed file designated as PRODUCTION status. FPGA designs using a less mature speed file designation should only be used during system prototyping or pre-production qualification. FPGA designs with speed files designated as Preview, Advance, or Preliminary should not be used in a production-quality system.

Whenever a speed file designation changes, as a device matures toward Production status, rerun the latest Xilinx ISE software on the FPGA design to ensure that the FPGA design incorporates the latest timing information and software updates.

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the published parameter values apply to all XA Spartan-3A devices, and AC and DC characteristics are specified using the same numbers for both I-Grade and Q-Grade.

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Timing parameters and their representative values are selected for inclusion below either because they are important as general design requirements or they indicate fundamental device performance characteristics. The XA Spartan-3A FPGA speed files (v1.41), part of the Xilinx Development Software, are the original source for many but not all of the values. The speed grade designations for these files are shown in Table 16. For more complete, more precise, and worst-case data, use the values reported by the Xilinx static timing analyzer (TRACE in the Xilinx development software) and back-annotated to the simulation netlist.

Table 16: **XA Spartan-3A FPGA v1.41 Speed Grade Designations**

Device	Production
XA3S200A	-4
XA3S400A	-4
XA3S700A	-4
XA3S1400A	-4

Table 17 provides the recent history of the XA Spartan-3A FPGA speed files.

Table 17: **XA Spartan-3A FPGA Speed File Version History**

Version	ISE Release	Description
1.39	10.1.01i	Initial release.
1.40	10.1.02i	Updated input timing adjustments.
1.41	10.1.03i	Updated output timing adjustments.

Table 20: **Setup and Hold Times for the IOB Input Path *(Cont'd)***

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade: -4	Units
					Min	
$T_{IOPICKD}$	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). The Input Delay is programmed.	LVCMOS25(2)	1	XA3S200A	2.20	ns
			2		2.93	ns
			3		3.78	ns
			4		4.37	ns
			5		4.20	ns
			6		5.23	ns
			7		6.11	ns
			8		6.71	ns
			1	XA3S400A	2.02	ns
			2		2.67	ns
			3		3.43	ns
			4		3.96	ns
			5		3.95	ns
			6		4.81	ns
			7		5.66	ns
			8		6.19	ns
			1	XA3S700A	1.95	ns
			2		2.83	ns
			3		3.72	ns
			4		4.31	ns
			5		4.14	ns
			6		5.19	ns
			7		6.10	ns
			8		6.73	ns
			1	XA3S1400A	2.17	ns
			2		2.92	ns
			3		3.76	ns
			4		4.32	ns
			5		4.19	ns
			6		5.09	ns
			7		5.98	ns
			8		6.57	ns
Hold Times						
T_{IOICKP}	Time from the active transition at the ICLK input of the Input Flip-Flop (IFF) to the point where data must be held at the Input pin. No Input Delay is programmed.	LVCMOS25(3)	0	XA3S200A	–0.65	ns
				XA3S400A	–0.42	ns
				XA3S700A	–0.67	ns
				XA3S1400A	–0.71	ns

Input Propagation Times

Table 21: **Propagation Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_DELAY_VALUE	Device	Speed Grade: -4	Units
					Max	
Propagation Times						
T_{IOPLI}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with no input delay programmed	LVCMOS25(2)	0	XA3S200A	2.04	ns
				XA3S400A	1.74	ns
				XA3S700A	1.74	ns
				XA3S1400A	1.97	ns
T_{IOPLID}	The time it takes for data to travel from the Input pin through the IFF latch to the I output with the input delay programmed	LVCMOS25(2)	1	XA3S200A	2.43	ns
			2		3.16	ns
			3		4.01	ns
			4		4.60	ns
			5		4.43	ns
			6		5.46	ns
			7		6.33	ns
			8		6.94	ns
			1	XA3S400A	2.25	ns
			2		2.90	ns
			3		3.66	ns
			4		4.19	ns
			5		4.18	ns
			6		5.03	ns
			7		5.88	ns
			8		6.42	ns
			1	XA3S700A	2.18	ns
			2		3.06	ns
			3		3.95	ns
			4		4.54	ns
			5		4.37	ns
			6		5.42	ns
			7		6.33	ns
			8		6.96	ns
			1	XA3S1400A	2.40	ns
			2		3.15	ns
			3		3.99	ns
			4		4.55	ns
			5		4.42	ns
			6		5.32	ns
			7		6.21	ns
			8		6.80	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This propagation time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the data Input. When this is true, *add* the appropriate Input adjustment from Table 22.

Output Timing Adjustments

Table 25: **Output Timing Adjustments for IOB**

Convert Output Time from LVCMOS25 with 12mA Drive and Fast Slew Rate to the Following Signal Standard (IOSTANDARD)			Add the Adjustment Below	Units
			Speed Grade: -4	
Single-Ended Standards				
LVTTL	Slow	2 mA	5.58	ns
		4 mA	3.45	ns
		6 mA	3.45	ns
		8 mA	2.26	ns
		12 mA	1.66	ns
		16 mA	1.29	ns
		24 mA	2.97	ns
	Fast	2 mA	3.37	ns
		4 mA	2.27	ns
		6 mA	2.27	ns
		8 mA	0.63	ns
		12 mA	0.61	ns
		16 mA	0.59	ns
		24 mA	0.60	ns
	QuietIO	2 mA	27.67	ns
		4 mA	27.67	ns
		6 mA	27.67	ns
		8 mA	16.71	ns
		12 mA	16.67	ns
		16 mA	16.22	ns
		24 mA	12.11	ns
LVCMOS33	Slow	2 mA	5.58	ns
		4 mA	3.30	ns
		6 mA	3.30	ns
		8 mA	2.26	ns
		12 mA	1.29	ns
		16 mA	1.22	ns
		24 mA	2.79	ns
	Fast	2 mA	3.72	ns
		4 mA	2.05	ns
		6 mA	2.08	ns
		8 mA	0.53	ns
		12 mA	0.59	ns
		16 mA	0.59	ns
		24 mA	0.51	ns
	QuietIO	2 mA	27.67	ns
		4 mA	27.67	ns
		6 mA	27.67	ns
		8 mA	16.71	ns
		12 mA	16.29	ns
		16 mA	16.18	ns
		24 mA	12.11	ns

Table 26: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		–	0	3.3	1M	0	1.4
LVCMOS33		–	0	3.3	1M	0	1.65
LVCMOS25		–	0	2.5	1M	0	1.25
LVCMOS18		–	0	1.8	1M	0	0.9
LVCMOS15		–	0	1.5	1M	0	0.75
LVCMOS12		–	0	1.2	1M	0	0.6
PCI33_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}
Differential							
LVDS_25		–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_33		–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25		–	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25		–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
MINI_LVDS_33		–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25		–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
LVPECL_33		–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
RSDS_25		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
RSDS_33		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
TMDS_33		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	3.3	V_{ICM}
PPDS_25		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
PPDS_33		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
DIFF_HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
DIFF_HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
DIFF_HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
DIFF_SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}

Table 28: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX}=3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type: FTG256, FGG400, FGG484	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
LVCMOS25	Slow	2	76	76
		4	46	46
		6	33	33
		8	24	24
		12	18	18
		16	–	11
		24	–	7
	Fast	2	18	18
		4	14	14
		6	6	6
		8	6	6
		12	3	3
		16	–	3
		24	–	2
	QuietIO	2	76	76
		4	60	60
		6	48	48
		8	36	36
		12	36	36
		16	–	36
		24	–	8
LVCMOS18	Slow	2	64	64
		4	34	34
		6	22	22
		8	18	18
		12	–	13
		16	–	10
	Fast	2	18	18
		4	9	9
		6	7	7
		8	4	4
		12	–	4
		16	–	3
	QuietIO	2	64	64
		4	64	64
		6	48	48
		8	36	36
		12	–	36
		16	–	24

Table 28: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX}=3.3V) *(Cont'd)***

Signal Standard (IOSTANDARD)			Package Type: FTG256, FGG400, FGG484	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
LVCMOS15	Slow	2	55	55
		4	31	31
		6	18	18
		8	–	15
		12	–	10
	Fast	2	25	25
		4	10	10
		6	6	6
		8	–	4
		12	–	3
	QuietIO	2	70	70
		4	40	40
		6	31	31
		8	–	31
		12	–	20
LVCMOS12	Slow	2	40	40
		4	–	25
		6	–	18
	Fast	2	31	31
		4	–	13
		6	–	9
	QuietIO	2	55	55
		4	–	36
		6	–	36
PCI33_3			16	16
HSTL_I			–	20
HSTL_III			–	8
HSTL_I_18			17	17
HSTL_II_18			–	5
HSTL_III_18			10	8
SSTL18_I			7	15
SSTL18_II			–	9
SSTL2_I			18	18
SSTL2_II			–	9
SSTL3_I			8	10
SSTL3_II			6	7

Digital Frequency Synthesizer

Table 37: **Recommended Operating Conditions for the DFS**

Symbol		Description		Speed Grade: -4		Units
				Min	Max	
Input Frequency Ranges(2)						
F_{CLKIN}	CLKIN_FREQ_FX	Frequency for the CLKIN input		0.200	333	MHz
Input Clock Jitter Tolerance(3)						
CLKIN_CYC_JITT_FX_LF		Cycle-to-cycle jitter at the CLKIN input, based on CLKFX output frequency	$F_{CLKFX} \leq 150$ MHz	–	±300	ps
CLKIN_CYC_JITT_FX_HF			$F_{CLKFX} > 150$ MHz	–	±150	ps
CLKIN_PER_JITT_FX		Period jitter at the CLKIN input		–	±1	ns

Notes:

1. DFS specifications apply when either of the DFS outputs (CLKFX or CLKFX180) is used.
2. If both DFS and DLL outputs are used on the same DCM, follow the more restrictive CLKIN_FREQ_DLL specifications in Table 35.
3. CLKIN input jitter beyond these limits may cause the DCM to lose lock.

Table 38: **Switching Characteristics for the DFS**

Symbol	Description		Device	Speed Grade: -4		Units
				Min	Max	
Output Frequency Ranges						
CLKOUT_FREQ_FX(2)	Frequency for the CLKFX and CLKFX180 outputs		All	5	320	MHz
Output Clock Jitter(3,4)						
CLKOUT_PER_JITT_FX	Period jitter at the CLKFX and CLKFX180 outputs.	CLKIN ≤ 20 MHz	All	**Typ**	**Max**	ps
				Use the Spartan-3A Jitter Calculator: www.xilinx.com/support/documentation/data_sheets/s3a_jitter_calc.zip		
		CLKIN > 20 MHz		±[1% of CLKFX period + 100]	±[1% of CLKFX period + 200]	ps
Duty Cycle(5,6)						
CLKOUT_DUTY_CYCLE_FX	Duty cycle precision for the CLKFX and CLKFX180 outputs, including the BUFGMUX and clock tree duty-cycle distortion		All	–	±[1% of CLKFX period + 350]	ps
Phase Alignment(6)						
CLKOUT_PHASE_FX	Phase offset between the DFS CLKFX output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±200	ps
CLKOUT_PHASE_FX180	Phase offset between the DFS CLKFX180 output and the DLL CLK0 output when both the DFS and DLL are used		All	–	±[1% of CLKFX period + 200]	ps

Table 38: **Switching Characteristics for the DFS *(Cont'd)***

Symbol	Description		Device	Speed Grade: -4		Units
				Min	Max	
Lock Time						
LOCK_FX[2,3]	The time from deassertion at the DCM's Reset input to the rising transition at its LOCKED output. The DFS asserts LOCKED when the CLKFX and CLKFX180 signals are valid. If using both the DLL and the DFS, use the longer locking time.	5 MHz ≤ F_{CLKIN} ≤ 15 MHz	All	–	5	ms
		F_{CLKIN} > 15 MHz		–	450	µs

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 37.
2. DFS performance requires the additional logic automatically added by ISE 9.1i and later software revisions.
3. For optimal jitter tolerance and faster lock time, use the CLKIN_PERIOD attribute.
4. Maximum output jitter is characterized within a reasonable noise environment (40 SSOs and 25% CLB switching) on an FPGA. Output jitter strongly depends on the environment, including the number of SSOs, the output drive strength, CLB utilization, CLB switching activities, switching frequency, power supply and PCB design. The actual maximum output jitter depends on the system application.
5. The CLKFX and CLKFX180 outputs always have an approximate 50% duty cycle.
6. Some duty-cycle and alignment specifications include a percentage of the CLKFX output period. For example, the data sheet specifies a maximum CLKFX jitter of "±[1% of CLKFX period + 200]". Assume the CLKFX output frequency is 100 MHz. The equivalent CLKFX period is 10 ns and 1% of 10 ns is 0.1 ns or 100 ps. According to the data sheet, the maximum jitter is ±[100 ps + 200 ps] = ±300 ps.

Phase Shifter

Table 39: **Recommended Operating Conditions for the PS in Variable Phase Mode**

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Operating Frequency Ranges				
PSCLK_FREQ (F_{PSCLK})	Frequency for the PSCLK input	1	167	MHz
Input Pulse Requirements				
PSCLK_PULSE	PSCLK pulse width as a percentage of the PSCLK period	40%	60%	–

Table 40: **Switching Characteristics for the PS in Variable Phase Mode**

Symbol	Description		Phase Shift Amount	Units
Phase Shifting Range				
MAX_STEPS[2]	Maximum allowed number of DCM_DELAY_STEP[3] steps for a given CLKIN clock period, where T = CLKIN clock period in ns. If using CLKIN_DIVIDE_BY_2 = TRUE, double the clock effective clock period.	CLKIN < 60 MHz	±[INTEGER(10 • (T_{CLKIN} – 3 ns))]	steps
		CLKIN ≥ 60 MHz	±[INTEGER(15 • (T_{CLKIN} – 3 ns))]	
FINE_SHIFT_RANGE_MIN	Minimum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MIN]	ns
FINE_SHIFT_RANGE_MAX	Maximum guaranteed delay for variable phase shifting		±[MAX_STEPS • DCM_DELAY_STEP_MAX]	ns

Notes:
1. The numbers in this table are based on the operating conditions set forth in Table 8 and Table 39.
2. The maximum variable phase shift range, MAX_STEPS, is only valid when the DCM is has no initial fixed phase shifting, that is, the PHASE_SHIFT attribute is set to 0.
3. The DCM_DELAY_STEP values are provided at the bottom of Table 36.

Suspend Mode Timing

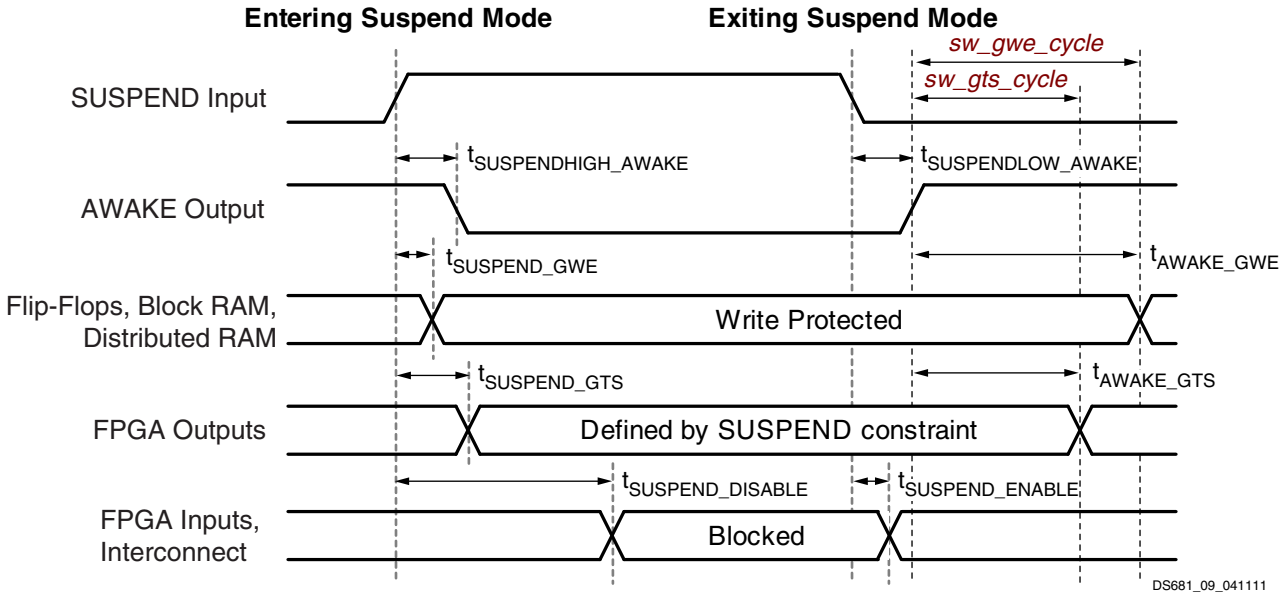


Figure 10: **Suspend Mode Timing**

Table 43: **Suspend Mode Timing Parameters**

Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***)	–	7	–	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***)	+160	+300	+600	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	<5	–	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–	ns
Exiting Suspend Mode					
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.	–	4 to 108	–	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1***.	–	67	–	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512***.	–	14	–	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1***.	–	57	–	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512***.	–	14	–	µs

Notes:

1. These parameters based on characterization.
2. For information on using the Spartan-3A Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

Table 46: **Master Mode CCLK Output Frequency by *ConfigRate* Option Setting**

Symbol	Description	*ConfigRate* Setting	Temperature Range	Minimum	Maximum	Units
F_{CCLK1}	Equivalent CCLK clock frequency by *ConfigRate* setting	1 *(power-on value)*	I-Grade/ Q-Grade	0.40	0.95	MHz
F_{CCLK3}		3	I-Grade/ Q-Grade	1.20	2.85	MHz
F_{CCLK6}		6	I-Grade/ Q-Grade	2.40	5.74	MHz
F_{CCLK7}		7	I-Grade/ Q-Grade	2.80	6.74	MHz
F_{CCLK8}		8	I-Grade/ Q-Grade	3.20	7.58	MHz
F_{CCLK10}		10	I-Grade/ Q-Grade	4.00	9.65	MHz
F_{CCLK12}		12	I-Grade/ Q-Grade	4.80	11.48	MHz
F_{CCLK13}		13	I-Grade/ Q-Grade	5.20	12.49	MHz
F_{CCLK17}		17	I-Grade/ Q-Grade	6.80	16.33	MHz
F_{CCLK22}		22	I-Grade/ Q-Grade	8.80	21.23	MHz
F_{CCLK25}		25	I-Grade/ Q-Grade	10.00	23.59	MHz
F_{CCLK27}		27	I-Grade/ Q-Grade	10.80	28.31	MHz
F_{CCLK33}		33	I-Grade/ Q-Grade	13.20	32.67	MHz
F_{CCLK44}		44	I-Grade/ Q-Grade	17.60	42.47	MHz
F_{CCLK50}		50	I-Grade/ Q-Grade	20.00	53.08	MHz
$F_{CCLK100}$		100	I-Grade/ Q-Grade	40.00	106.16	MHz

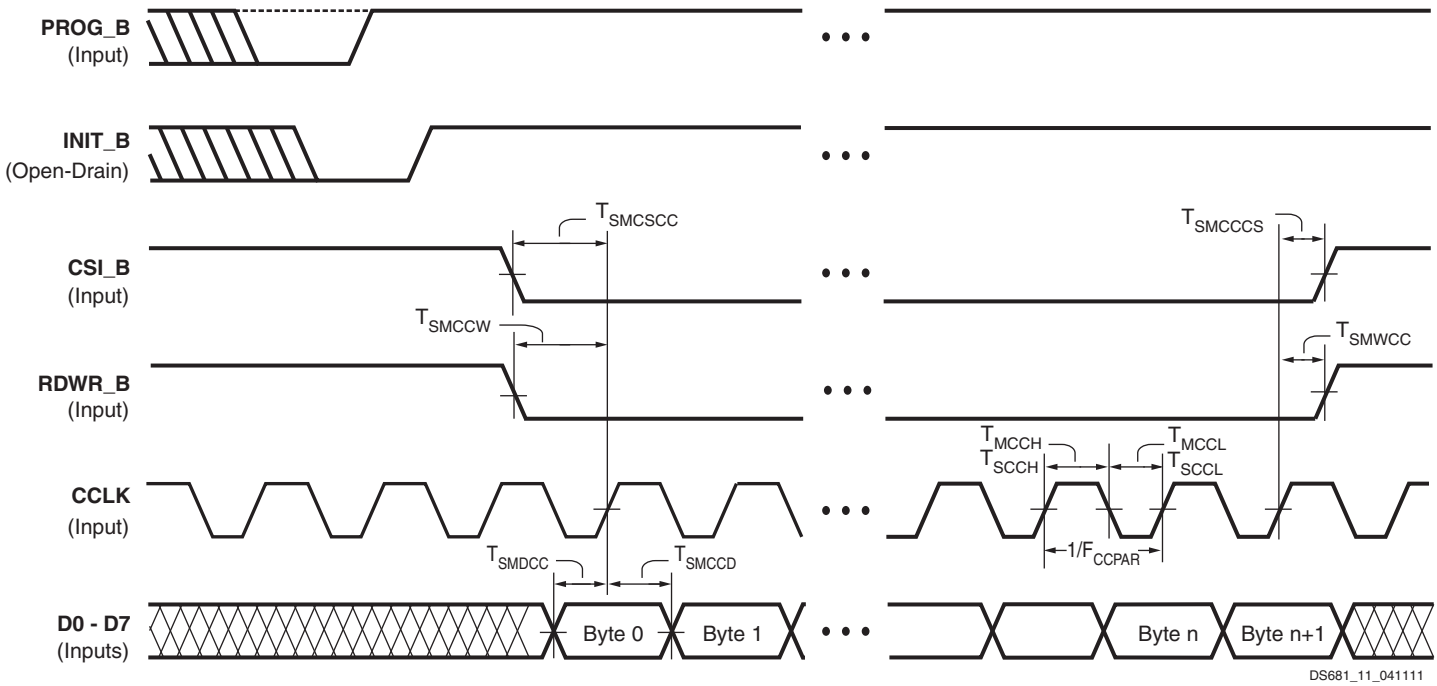
Table 47: **Master Mode CCLK Output Minimum Low and High Time**

Symbol	Description		*ConfigRate* Setting															Units
			1	3	6	7	8	10	12	13	17	22	25	27	33	44	50	100	
T_{MCCL}, T_{MCCH}	Master Mode CCLK Minimum Low and High Time	I-Grade/ Q-Grade	474	158	78.4	66.8	59.3	46.6	39.2	36.0	27.6	21.2	19.1	15.9	13.8	10.6	8.5	4.2	ns

Table 48: **Slave Mode CCLK Input Low and High Time**

Symbol	Description	Min	Max	Units
T_{SCCL}, T_{SCCH}	CCLK Low and High time	5	∞	ns

Slave Parallel Mode Timing



Notes:

1. It is possible to abort configuration by pulling CSI_B Low in a given CCLK cycle, then switching RDWR_B Low or High in any subsequent cycle for which CSI_B remains Low. The RDWR_B pin asynchronously controls the driver impedance of the D0–D7 bus. When RDWR_B switches High, be careful to avoid contention on the D0–D7 bus.

Figure 13: **Waveforms for Slave Parallel Configuration**

Table 50: **Timing for the Slave Parallel Configuration Mode**

Symbol	Description		Speed Grade: -4		Units
			Min	Max	
Setup Times					
T_{SMDCC} (2)	The time from the setup of data at the D0-D7 pins to the rising transition at the CCLK pin		7	–	ns
T_{SMCSCC}	Setup time on the CSI_B pin before the rising transition at the CCLK pin		7	–	ns
T_{SMCCW}	Setup time on the RDWR_B pin before the rising transition at the CCLK pin		15	–	ns
Hold Times					
T_{SMCCD}	The time from the rising transition at the CCLK pin to the point when data is last held at the D0-D7 pins		1.0	–	ns
T_{SMCCCS}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the CSO_B pin		0	–	ns
T_{SMWCC}	The time from the rising transition at the CCLK pin to the point when a logic level is last held at the RDWR_B pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the CCLK input pin		5	–	ns
T_{CCL}	The Low pulse width at the CCLK input pin		5	–	ns
F_{CCPAR}	Frequency of the clock signal at the CCLK input pin	No bitstream compression	0	80	MHz
		With bitstream compression	0	80	MHz

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.
2. Some Xilinx documents refer to Parallel modes as “SelectMAP” modes.

Table 54: **Configuration Timing Requirements for Attached Parallel NOR Flash**

Symbol	Description	Requirement	Units
T_{CE} (t_{ELQV})	Parallel NOR Flash PROM chip-select time	$T_{CE} \leq T_{INITADDR}$	ns
T_{OE} (t_{GLQV})	Parallel NOR Flash PROM output-enable time	$T_{OE} \leq T_{INITADDR}$	ns
T_{ACC} (t_{AVQV})	Parallel NOR Flash PROM read access time	$T_{ACC} \leq 50\% T_{CCLKn(min)} - T_{CCO} - T_{DCC} - PCB$	ns
T_{BYTE} (t_{FLQV}, t_{FHQV})	For x8/x16 PROMs only: BYTE# to output valid time(3)	$T_{BYTE} \leq T_{INITADDR}$	ns

Notes:

1. These requirements are for successful FPGA configuration in BPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.
3. The initial BYTE# timing can be extended using an external, appropriately sized pull-down resistor on the FPGA's LDC2 pin. The resistor value also depends on whether the FPGA's PUDC_B pin is High or Low.

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
04/30/08	1.0	Initial release.
05/07/08	1.0.1	Updated Figure 14, minor edits under Features and Package Marking, Table 20 and 21.
02/03/09	1.1	Updated Key Feature Differences from Commercial XC Devices, page 2. Removed MultiBoot description from Configuration, page 3. Updated to v1.41 in Table 3 and Table 16. Removed -5 high performance (commercial only) speed grade from Ordering Information, page 5. Replaced V_{ICM} with V_{CCAUX} in Note 7 of Table 13. Added versions 1.40 and 1.41 to Table 17. Updated Note 2 in Figure 11. Removed T_{IOOLP} from Table 23. Updated T_{IOCKHZ} and T_{IOCKON} in Table 24. Updated Table 22 and Table 25. Updated SSO number for left and right I/O banks of DIFF_SSTL18_II standard in Table 28. Updated T_{ACC} requirement in Table 54.
04/22/11	2.0	This revision goes along with XCN11019: *Data Sheet Revisions for Xilinx Automotive (XA) Spartan-3A/-3A DSP FPGA Devices*. Added I_{IK} to Table 4. Updated description for V_{IN} in Table 8 including adding Note 4. Also, added Note 2 to I_L in Table 9 to note potential leakage between pins of a differential pair. Updated Notes 5 and 6 in Table 13. Table 20: Updated tags to Note 3. In Table 42, corrected symbols for $T_{DNACLKH}$ and $T_{DNACLKL}$. Corrected symbols for $T_{SUSPEND\_GTS}$ and $T_{SUSPEND\_GWE}$ in Table 43. Revised standard title to: IEEE 1149.1/1532 JTAG Test Access Port Timing. Updated Notice of Disclaimer.

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