AMD Xilinx - XA3S400A-4FTG256I Datasheet

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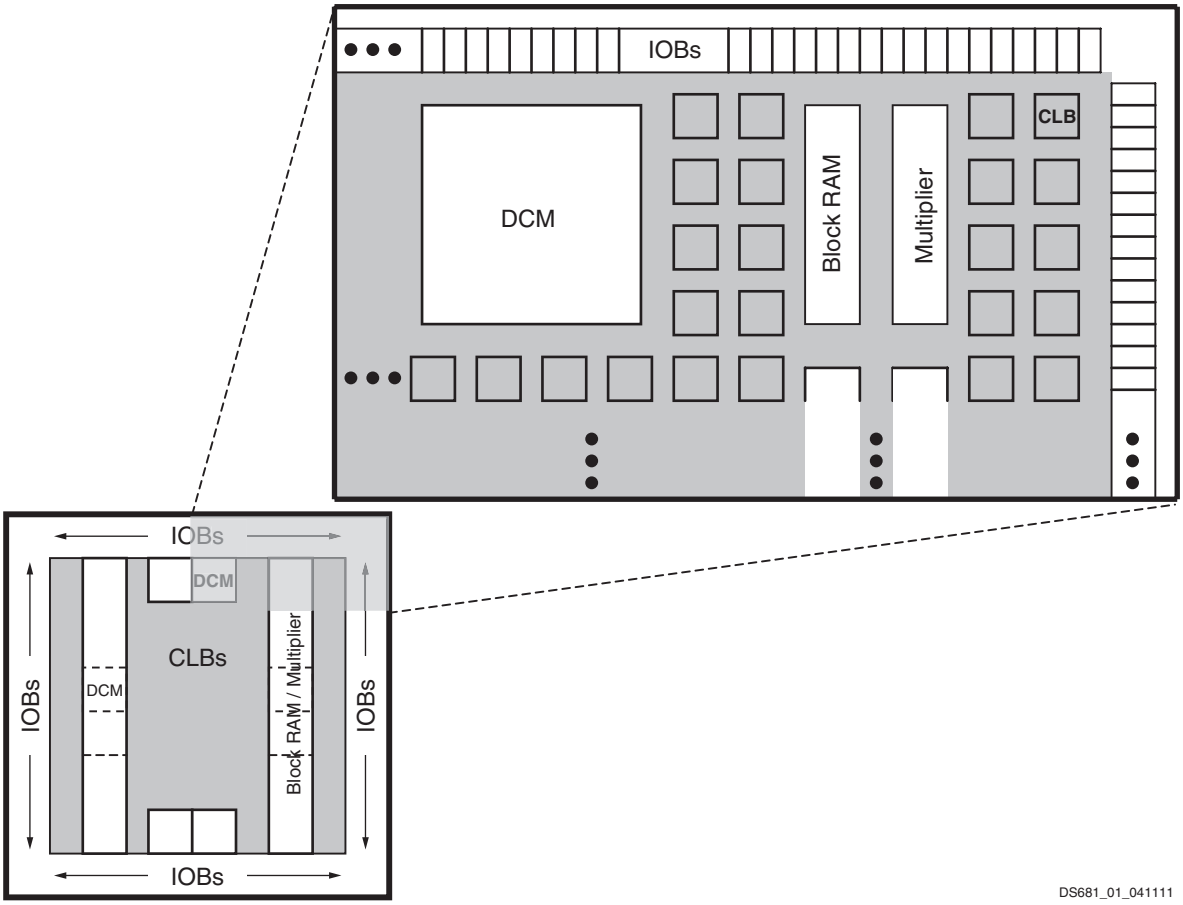
Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	896
Number of Logic Elements/Cells	8064
Total RAM Bits	368640
Number of I/O	195
Number of Gates	400000
Voltage - Supply	1.14V ~ 1.26V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FTBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xa3s400a-4ftg256i



Notes:

1. The XA3S700A and XA3S1400A have two additional DCMs on both the left and right sides as indicated by the dashed lines.

Figure 1: **XA Spartan-3A Family Architecture**

Configuration

XA Spartan-3A FPGAs are programmed by loading configuration data into robust, reprogrammable, static CMOS configuration latches (CCLs) that collectively control all functional elements and routing resources. The FPGA's configuration data is stored externally in a SPI serial Flash or some other non-volatile medium, either on or off the board. After applying power, the configuration data is written to the FPGA using any of five different modes:

- Serial Peripheral Interface (SPI) from an industry-standard SPI serial Flash
- Byte Peripheral Interface (BPI) Up from an industry-standard x8 or x8/x16 parallel NOR Flash
- Slave Serial, typically downloaded from a processor
- Slave Parallel, typically downloaded from a processor
- Boundary Scan (JTAG), typically downloaded from a processor or system tester

Additionally, each XA Spartan-3A FPGA contains a unique, factory-programmed Device DNA identifier useful for tracking purposes, anti-cloning designs, or IP protection.

I/O Capabilities

The XA Spartan-3A FPGA SelectIO interface supports many popular single-ended and differential standards. Table 2 shows the number of user I/Os as well as the number of differential I/O pairs available for each device/package combination. Some of the user I/Os are unidirectional input-only pins as indicated in Table 2.

XA Spartan-3A FPGAs support the following single-ended standards:

- 3.3V low-voltage TTL (LVTTL)
- Low-voltage CMOS (LVCMOS) at 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V
- 3.3V PCI at 33 MHz
- HSTL I, II, and III at 1.5V and 1.8V, commonly used in memory applications
- SSTL I and II at 1.8V, 2.5V, and 3.3V, commonly used for memory applications

XA Spartan-3A FPGAs support the following differential standards:

- LVDS, mini-LVDS, RSDS, and PPDS I/O at 2.5V or 3.3V
- Bus LVDS I/O at 2.5V
- TMDS I/O at 3.3V
- Differential HSTL and SSTL I/O
- LVPECL inputs at 2.5V or 3.3V

Table 2: **Available User I/Os and Differential I/O Pairs**

Device	FTG256		FGG400		FGG484	
	User	Differential	User	Differential	User	Differential
XA3S200A	**195** *(35)*	**90** *(50)*	–	–	–	–
XA3S400A	**195** *(35)*	**90** *(50)*	**311** *(63)*	**142** *(78)*	–	–
XA3S700A	–	–	**311** *(63)*	**142** *(78)*	**372** *(84)*	**165** *(93)*
XA3S1400A	–	–	–	–	**375** *(87)*	**165** *(93)*

Notes:

1. The number shown in **bold** indicates the maximum number of I/O and input-only pins. The number shown in (italics) indicates the number of input-only pins. The differential input-only pin count includes both differential pairs on input-only pins and differential pairs on I/O pins within I/O banks that are restricted to differential inputs.

Production Status

Table 3 indicates the production status of each XA Spartan-3A FPGA by temperature range and speed grade. The table also lists the earliest speed file version required for creating a production configuration bitstream. Later versions are also supported.

Table 3: **XA Spartan-3A FPGA Family Production Status (Production Speed File)**

Temperature Range		I-Grade	Q-Grade
Speed Grade		Standard (-4)	Standard (-4)
Part Number	XA3S200A	Production (v1.41)	Production (v1.41)
	XA3S400A	Production (v1.41)	Production (v1.41)
	XA3S700A	Production (v1.41)	Production (v1.41)
	XA3S1400A	Production (v1.41)	Production (v1.41)

Package Marking

Figure 2 shows the top marking for Spartan-3A FPGAs in BGA packages. The markings for the BGA packages are nearly identical to those for the quad-flat packages, except that the marking is rotated with respect to the ball A1 indicator.

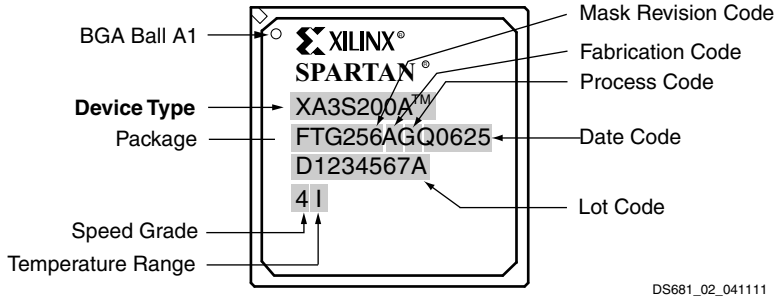


Figure 2: **XA Spartan-3A FPGA BGA Package Marking Example**

Ordering Information

XA Spartan-3A FPGAs are available in Pb-free packaging only for all device/package combinations.

Pb-Free Packaging

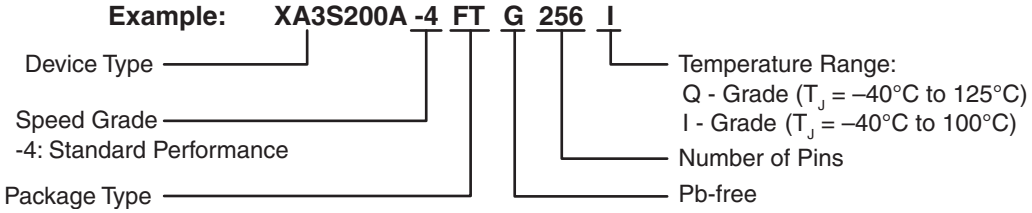


Figure 3: **Ordering Information**

Device	Speed Grade		Package Type / Number of Pins		Temperature Range (T_J)	
XA3S200A	-4	Standard Performance	FTG256	256-ball Fine-Pitch Thin Ball Grid Array (FTBGA)	I	I-Grade (–40°C to 100°C)
XA3S400A			FGG400	400-ball Fine-Pitch Ball Grid Array (FBGA)	Q	Q-Grade (–40°C to 125°C)
XA3S700A			FGG484	484-ball Fine-Pitch Ball Grid Array (FBGA)		
XA3S1400A						

Notes:

1. The XA Spartan-3A FPGA product line is available in -4 Speed Grade only.

DC Electrical Characteristics

All parameter limits are representative of worst-case supply voltage and junction temperature conditions. Unless otherwise noted, the published parameter values apply to all XA Spartan-3A devices, and AC and DC characteristics are specified using the same numbers for both I-Grade and Q-Grade.

Absolute Maximum Ratings

Stresses beyond those listed under Table 4: Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions is not implied. Exposure to absolute maximum conditions for extended periods of time adversely affects device reliability.

Table 4: **Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Max	Units
V_{CCINT}	Internal supply voltage		–0.5	1.32	V
V_{CCAUX}	Auxiliary supply voltage		–0.5	3.75	V
V_{CCO}	Output driver supply voltage		–0.5	3.75	V
V_{REF}	Input reference voltage		–0.5	V_{CCO} + 0.5	V
V_{IN}	Voltage applied to all User I/O pins and dual-purpose pins	Driver in a high-impedance state	–0.95	4.6	V
	Voltage applied to all Dedicated pins		–0.5	4.6	V
I_{IK}	Input clamp current per I/O pin	$-0.5V < V_{IN} < (V_{CCO} + 0.5V)$ (1)	–	±100	mA
V_{ESD}	Electrostatic Discharge Voltage	Human body model	–	±2000	V
		Charged device model	–	±500	V
		Machine model	–	±200	V
T_J	Junction temperature		–	125	°C
T_{STG}	Storage temperature		–65	150	°C

Notes:

1. Upper clamp applies only when using PCI IOSTANDARDs.
2. For soldering guidelines, see UG112: *Device Packaging and Thermal Characteristics* and XAPP427: *Implementation and Solder Reflow Guidelines for Pb-Free Packages*.

Single-Ended I/O Standards

Table 11: **Recommended Operating Conditions for User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[2]			V_{REF}			V_{IL}	V_{IH}
	Min (V)	Nom (V)	Max (V)	Min (V)	Nom (V)	Max (V)	Max (V)	Min (V)
LVTTL	3.0	3.3	3.6	V_{REF} is not used for these I/O standards			0.8	2.0
LVCMOS33[4]	3.0	3.3	3.6				0.8	2.0
LVCMOS25[4,5]	2.3	2.5	2.7				0.7	1.7
LVCMOS18	1.65	1.8	1.95				0.4	0.8
LVCMOS15	1.4	1.5	1.6				0.4	0.8
LVCMOS12	1.1	1.2	1.3				0.4	0.7
PCI33_3[6]	3.0	3.3	3.6				$0.3 \bullet V_{CCO}$	$0.5 \bullet V_{CCO}$
HSTL_I	1.4	1.5	1.6	0.68	0.75	0.9	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III	1.4	1.5	1.6	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_I_18	1.7	1.8	1.9	0.8	0.9	1.1	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_II_18	1.7	1.8	1.9	–	0.9	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
HSTL_III_18	1.7	1.8	1.9	–	1.1	–	$V_{REF} - 0.1$	$V_{REF} + 0.1$
SSTL18_I	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL18_II	1.7	1.8	1.9	0.833	0.900	0.969	$V_{REF} - 0.125$	$V_{REF} + 0.125$
SSTL2_I	2.3	2.5	2.7	1.15	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL2_II	2.3	2.5	2.7	1.15	1.25	1.38	$V_{REF} - 0.150$	$V_{REF} + 0.150$
SSTL3_I	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$
SSTL3_II	3.0	3.3	3.6	1.3	1.5	1.7	$V_{REF} - 0.2$	$V_{REF} + 0.2$

Notes:

1. Descriptions of the symbols used in this table are as follows:
   V_{CCO} – the supply voltage for output drivers
   V_{REF} – the reference voltage for setting the input switching threshold
   V_{IL} – the input voltage that indicates a Low logic level
   V_{IH} – the input voltage that indicates a High logic level
2. In general, the V_{CCO} rails supply only output drivers, not input circuits. The exceptions are for LVCMOS25 inputs when V_{CCAUX} = 3.3V range and for PCI I/O standards.
3. For device operation, the maximum signal voltage (V_{IH} max) can be as high as V_{IN} max. See Table 8.
4. There is approximately 100 mV of hysteresis on inputs using LVCMOS33 and LVCMOS25 I/O standards.
5. All Dedicated pins (PROG_B, DONE, SUSPEND, TCK, TDI, TDO, and TMS) draw power from the V_{CCAUX} rail and use the LVCMOS25 or LVCMOS33 standard depending on V_{CCAUX}. The Dual-Purpose configuration pins use the LVCMOS25 standard before the User mode. When using these pins as part of a standard 2.5V configuration interface, apply 2.5V to the V_{CCO} lines of Banks 0, 1, and 2 at power-on as well as throughout configuration.
6. For information on PCI IP solutions, see http://www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics, but no PCI-X IP is supported.

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards**

IOSTANDARD Attribute		Test Conditions		Logic Level Characteristics	
		I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
LVTTL[3]	2	2	–2	0.4	2.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16		
	24	24[6]	–24		
LVCMOS33[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16	16	–16[6]		
	24[4]	24	–24[6]		
LVCMOS25[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8	8	–8		
	12	12	–12		
	16[4]	16	–16[6]		
	24[4]	24[6]	–24[6]		
LVCMOS18[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6[6]		
	8	8	–8		
	12[4]	12	–12[6]		
	16[4]	16	–16		
LVCMOS15[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4	4	–4		
	6	6	–6		
	8[4]	8	–8		
	12[4]	12	–12		
LVCMOS12[3]	2	2	–2	0.4	V_{CCO} – 0.4
	4[4]	4	–4		
	6[4]	6	–6		
PCI33_3[5]		1.5	–0.5	10% V_{CCO}	90% V_{CCO}

Table 12: **DC Characteristics of User I/Os Using Single-Ended Standards *(Cont'd)***

IOSTANDARD Attribute	Test Conditions		Logic Level Characteristics	
	I_{OL} (mA)	I_{OH} (mA)	V_{OL} Max (V)	V_{OH} Min (V)
HSTL_I(4)	8	–8	0.4	V_{CCO} – 0.4
HSTL_III(4)	24(7)	–8	0.4	V_{CCO} – 0.4
HSTL_I_18	8	–8	0.4	V_{CCO} – 0.4
HSTL_II_18(4)	16	–16(7)	0.4	V_{CCO} – 0.4
HSTL_III_18	24(7)	–8	0.4	V_{CCO} – 0.4
SSTL18_I	6.7	–6.7	V_{TT} – 0.475	V_{TT} + 0.475
SSTL18_II(4)	13.4	–13.4	V_{TT} – 0.475	V_{TT} + 0.475
SSTL2_I	8.1	–8.1	V_{TT} – 0.61	V_{TT} + 0.61
SSTL2_II(4)	16.2	–16.2	V_{TT} – 0.80	V_{TT} + 0.80
SSTL3_I	8	–8	V_{TT} – 0.6	V_{TT} + 0.6
SSTL3_II	16	–16	V_{TT} – 0.8	V_{TT} + 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 11.
2. Descriptions of the symbols used in this table are as follows:
   I_{OL} — the output current condition under which V_{OL} is tested
   I_{OH} — the output current condition under which V_{OH} is tested
   V_{OL} — the output voltage that indicates a Low logic level
   V_{OH} — the output voltage that indicates a High logic level
   V_{IL} — the input voltage that indicates a Low logic level
   V_{IH} — the input voltage that indicates a High logic level
   V_{CCO} — the supply voltage for output drivers
   V_{REF} — the reference voltage for setting the input switching threshold
   V_{TT} — the voltage applied to a resistor termination
3. For the LVCMOS and LVTTL standards: the same V_{OL} and V_{OH} limits apply for both the Fast and Slow slew attributes.
4. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
5. Tested according to the relevant PCI specifications. For information on PCI IP solutions, see http://www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm. The PCI IOSTANDARD is not supported on input-only pins. The PCIX IOSTANDARD is available and has equivalent characteristics, but no PCI-X IP is supported.
6. DE-RATE by 20% for T_J above 100°C
7. DE-RATE by 5% for T_J above 100°C

Differential I/O Standards

Differential Input Pairs

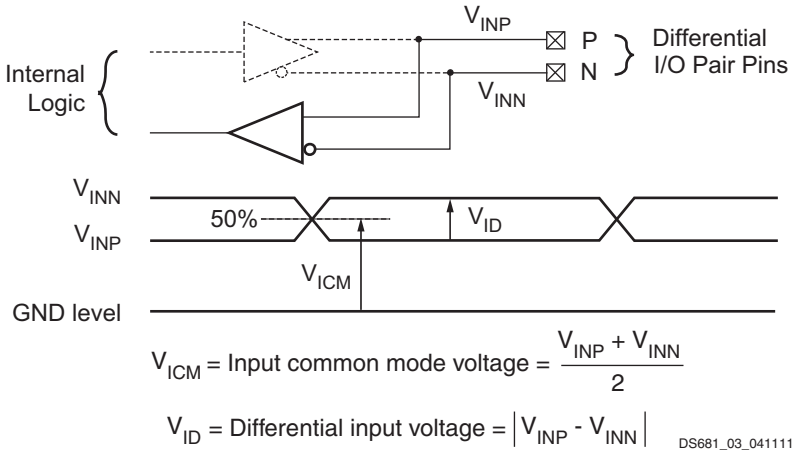


Figure 4: **Differential Input Voltages**

Table 13: **Recommended Operating Conditions for User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{CCO} for Drivers[1]			V_{ID}			V_{ICM}[2]		
	Min (V)	Nom (V)	Max (V)	Min (mV)	Nom (mV)	Max (mV)	Min (V)	Nom (V)	Max (V)
LVDS_25[3]	2.25	2.5	2.75	100	350	600	0.3	1.25	2.35
LVDS_33[3]	3.0	3.3	3.6	100	350	600	0.3	1.25	2.35
BLVDS_25[4]	2.25	2.5	2.75	100	300	–	0.3	1.3	2.35
MINI_LVDS_25[3]	2.25	2.5	2.75	200	–	600	0.3	1.2	1.95
MINI_LVDS_33[3]	3.0	3.3	3.6	200	–	600	0.3	1.2	1.95
LVPECL_25[5]	Inputs Only			100	800	1000	0.3	1.2	1.95
LVPECL_33[5]	Inputs Only			100	800	1000	0.3	1.2	2.8[6]
RSDS_25[3]	2.25	2.5	2.75	100	200	–	0.3	1.2	1.5
RSDS_33[3]	3.0	3.3	3.6	100	200	–	0.3	1.2	1.5
TMDS_33[3,4,7]	3.14	3.3	3.47	150	–	1200	2.7	–	3.23
PPDS_25[3]	2.25	2.5	2.75	100	–	400	0.2	–	2.3
PPDS_33[3]	3.0	3.3	3.6	100	–	400	0.2	–	2.3
DIFF_HSTL_I_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_II_18[8]	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_III_18	1.7	1.8	1.9	100	–	–	0.8	–	1.1
DIFF_HSTL_I	1.4	1.5	1.6	100	–	–	0.68		0.9
DIFF_HSTL_III	1.4	1.5	1.6	100	–	–	–	0.9	–
DIFF_SSTL18_I	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL18_II[8]	1.7	1.8	1.9	100	–	–	0.7	–	1.1
DIFF_SSTL2_I	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL2_II[8]	2.3	2.5	2.7	100	–	–	1.0	–	1.5
DIFF_SSTL3_I	3.0	3.3	3.6	100	–	–	1.1	–	1.9
DIFF_SSTL3_II	3.0	3.3	3.6	100	–	–	1.1	–	1.9

Notes:

1. The V_{CCO} rails supply only differential output drivers, not input circuits.
2. V_{ICM} must be less than V_{CCAUX}.
3. These true differential output standards are supported only on FPGA banks 0 and 2. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
4. See External Termination Requirements for Differential I/O, page 16.
5. LVPECL is supported on inputs only, not outputs. LVPECL_33 requires V_{CCAUX}=3.3V ± 10%.
6. LVPECL_33 maximum V_{ICM} = the lower of 2.8V or $V_{CCAUX} – (V_{ID} / 2)$
7. Requires V_{CCAUX} = 3.3V ± 10% for inputs. $(V_{CCAUX} – 300\ mV) \leq V_{ICM} \leq (V_{CCAUX} – 37\ mV)$
8. These higher-drive output standards are supported only on FPGA banks 1 and 3. Inputs are unrestricted. See the chapter "Using I/O Resources" in UG331.
9. V_{REF} inputs are used for the DIFF_SSTL and DIFF_HSTL standards. The V_{REF} settings are the same as for the single-ended versions in Table 11. Other differential standards do not use V_{REF}.

Differential Output Pairs

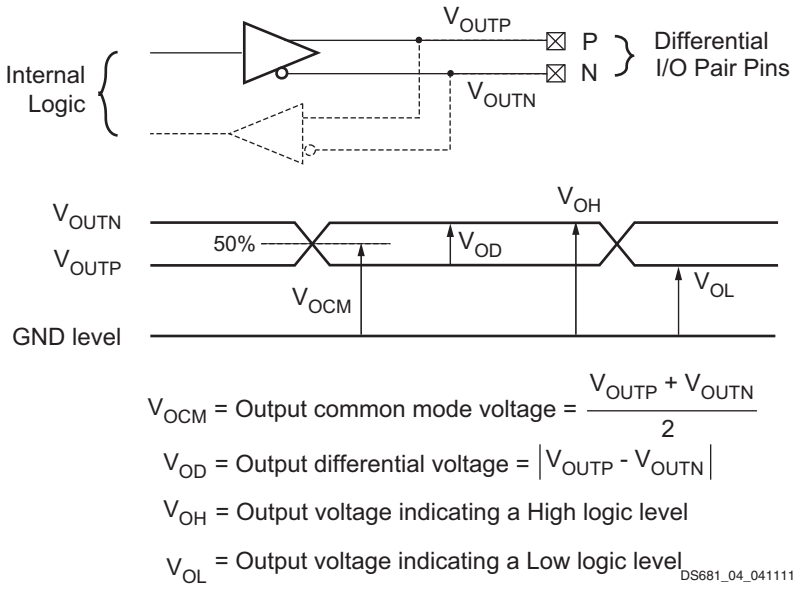


Figure 5: **Differential Output Voltages**

Table 14: **DC Characteristics of User I/Os Using Differential Signal Standards**

IOSTANDARD Attribute	V_{OD}			V_{OCM}			V_{OH}	V_{OL}
	Min (mV)	Typ (mV)	Max (mV)	Min (V)	Typ (V)	Max (V)	Min (V)	Max (V)
LVDS_25	247	350	454	1.125	–	1.375	–	–
LVDS_33	247	350	454	1.125	–	1.375	–	–
BLVDS_25	240	350	460	–	1.30	–	–	–
MINI_LVDS_25	300	–	600	1.0	–	1.4	–	–
MINI_LVDS_33	300	–	600	1.0	–	1.4	–	–
RSDS_25	100	–	400	1.0	–	1.4	–	–
RSDS_33	100	–	400	1.0	–	1.4	–	–
TMDS_33	400	–	800	V_{CCO} – 0.405	–	V_{CCO} – 0.190	–	–
PPDS_25	100	–	400	0.5	0.8	1.4	–	–
PPDS_33	100	–	400	0.5	0.8	1.4	–	–
DIFF_HSTL_I_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_II_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III_18	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_I	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_HSTL_III	–	–	–	–	–	–	V_{CCO} – 0.4	0.4
DIFF_SSTL18_I	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL18_II	–	–	–	–	–	–	V_{TT} + 0.475	V_{TT} – 0.475
DIFF_SSTL2_I	–	–	–	–	–	–	V_{TT} + 0.61	V_{TT} – 0.61
DIFF_SSTL2_II	–	–	–	–	–	–	V_{TT} + 0.81	V_{TT} – 0.81
DIFF_SSTL3_I	–	–	–	–	–	–	V_{TT} + 0.6	V_{TT} – 0.6
DIFF_SSTL3_II	–	–	–	–	–	–	V_{TT} + 0.8	V_{TT} – 0.8

Notes:

1. The numbers in this table are based on the conditions set forth in Table 8 and Table 13.
2. See External Termination Requirements for Differential I/O, page 16.
3. Output voltage measurements for all differential standards are made with a termination resistor (R_T) of 100Ω across the N and P pins of the differential signal pair.
4. At any given time, no more than two of the following differential output standards can be assigned to an I/O bank: LVDS_25, RSDS_25, MINI_LVDS_25, PPDS_25 when V_{CCO}=2.5V, or LVDS_33, RSDS_33, MINI_LVDS_33, TMDS_33, PPDS_33 when V_{CCO} = 3.3V

External Termination Requirements for Differential I/O

LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards

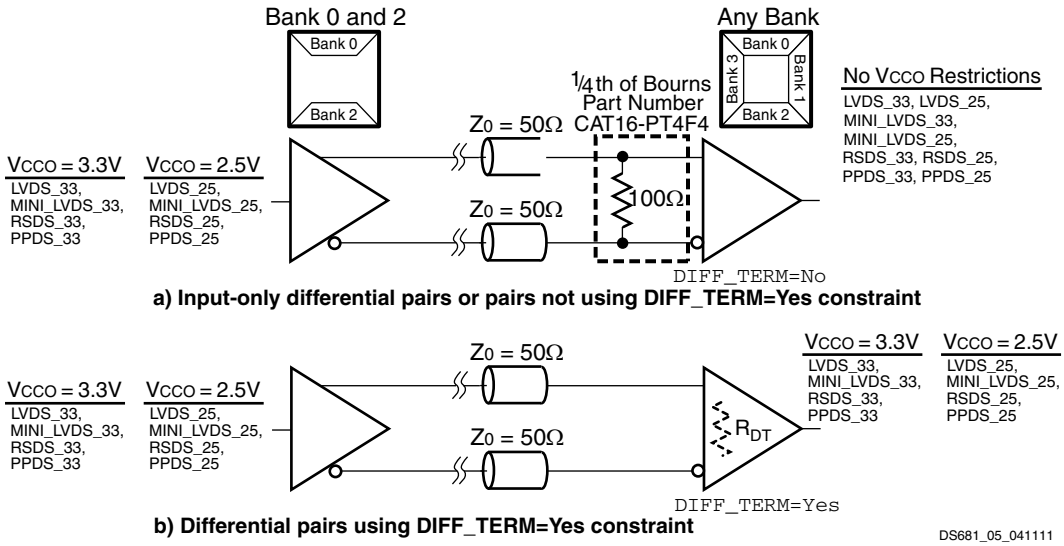


Figure 6: **External Input Termination for LVDS, RSDS, MINI_LVDS, and PPDS I/O Standards**

BLVDS_25 I/O Standard

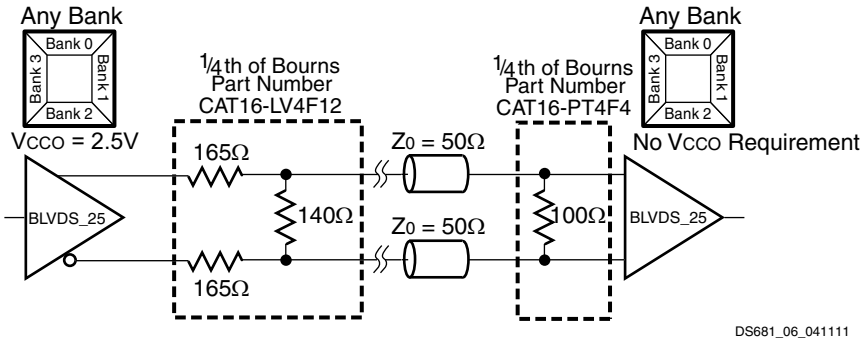


Figure 7: **External Termination Resistors for BLVDS_25 I/O Standard**

TMDS_33 I/O Standard

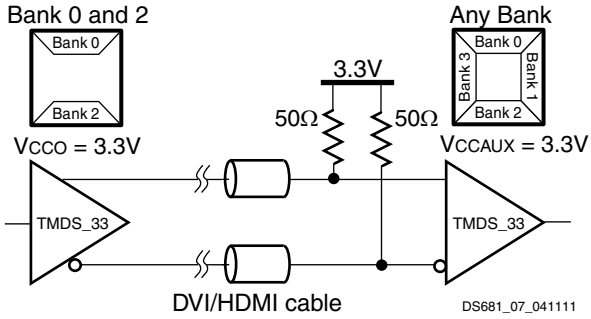


Figure 8: **External Input Resistors Required for TMDS_33 I/O Standard**

Pin-to-Pin Setup and Hold Times

Table 19: **Pin-to-Pin Setup and Hold Times for the IOB Input Path (System Synchronous)**

Symbol	Description	Conditions	Device	Speed Grade: -4	Units
				Min	
Setup Times					
T_{PSDCM}	When writing to the Input Flip-Flop (IFF), the time from the setup of data at the Input pin to the active transition at a Global Clock pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(2), IFD_DELAY_VALUE = 0, with DCM(4)	XA3S200A	2.84	ns
			XA3S400A	2.68	ns
			XA3S700A	2.57	ns
			XA3S1400A	2.17	ns
T_{PSFD}	When writing to IFF, the time from the setup of data at the Input pin to an active transition at the Global Clock pin. The DCM is not in use. The Input Delay is progr ammed.	LVCMOS25(2), IFD_DELAY_VALUE = 5, without DCM	XA3S200A	2.76	ns
			XA3S400A	2.60	ns
			XA3S700A	2.63	ns
			XA3S1400A	2.41	ns
Hold Times					
T_{PHDCM}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is in use. No Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 0, with DCM(4)	XA3S200A	–0.52	ns
			XA3S400A	–0.29	ns
			XA3S700A	–0.12	ns
			XA3S1400A	0.00	ns
T_{PHFD}	When writing to IFF, the time from the active transition at the Global Clock pin to the point when data must be held at the Input pin. The DCM is not in use. The Input Delay is programmed.	LVCMOS25(3), IFD_DELAY_VALUE = 5, without DCM	XA3S200A	–0.56	ns
			XA3S400A	–0.42	ns
			XA3S700A	–0.75	ns
			XA3S1400A	–0.69	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 8 and Table 11.
2. This setup time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, subtract the appropriate adjustment from Table 22. If this is true of the data Input, add the appropriate Input adjustment from the same table.
3. This hold time requires adjustment whenever a signal standard other than LVCMOS25 is assigned to the Global Clock Input or the data Input. If this is true of the Global Clock Input, add the appropriate Input adjustment from Table 22. If this is true of the data Input, subtract the appropriate Input adjustment from the same table. When the hold time is negative, it is possible to change the data before the clock's active edge.
4. DCM output jitter is included in all measurements.

Input Setup and Hold Times

Table 20: **Setup and Hold Times for the IOB Input Path**

Symbol	Description	Conditions	IFD_ DELAY_ VALUE	Device	Speed Grade: -4	Units
					Min	
Setup Times						
T_{IOPICK}	Time from the setup of data at the Input pin to the active transition at the ICLK input of the Input Flip-Flop (IFF). No Input Delay is programmed.	LVCMOS25(2)	0	XA3S200A	1.81	ns
				XA3S400A	1.51	ns
				XA3S700A	1.51	ns
				XA3S1400A	1.74	ns

Input Timing Adjustments

Table 22: **Input Timing Adjustments by IOSTANDARD**

Convert Input Time from LVCMOS25 to the Following Signal Standard (IOSTANDARD)	Add the Adjustment Below	Units
	Speed Grade: -4	
Single-Ended Standards		
LVTTL	0.62	ns
LVCMOS33	0.54	ns
LVCMOS25	0	ns
LVCMOS18	0.83	ns
LVCMOS15	0.60	ns
LVCMOS12	0.31	ns
PCI33_3	0.45	ns
HSTL_I	0.72	ns
HSTL_III	0.85	ns
HSTL_I_18	0.69	ns
HSTL_II_18	0.83	ns
HSTL_III_18	0.79	ns
SSTL18_I	0.71	ns
SSTL18_II	0.71	ns
SSTL2_I	0.71	ns
SSTL2_II	0.71	ns
SSTL3_I	0.78	ns
SSTL3_II	0.78	ns
Differential Standards		
LVDS_25	0.79	ns
LVDS_33	0.79	ns
BLVDS_25	0.79	ns
MINI_LVDS_25	0.84	ns
MINI_LVDS_33	0.84	ns
LVPECL_25	0.80	ns
LVPECL_33	0.80	ns
RSDS_25	0.83	ns
RSDS_33	0.83	ns
TMDS_33	0.80	ns
PPDS_25	0.81	ns
PPDS_33	0.81	ns
DIFF_HSTL_I_18	0.80	ns
DIFF_HSTL_II_18	0.98	ns
DIFF_HSTL_III_18	1.05	ns
DIFF_HSTL_I	0.77	ns
DIFF_HSTL_III	1.05	ns
DIFF_SSTL18_I	0.76	ns
DIFF_SSTL18_II	0.76	ns
DIFF_SSTL2_I	0.77	ns
DIFF_SSTL2_II	0.77	ns
DIFF_SSTL3_I	1.06	ns
DIFF_SSTL3_II	1.06	ns

Notes:

1. The numbers in this table are tested using the methodology presented in Table 26 and are based on the operating conditions set forth in Table 8, Table 11, and Table 13.
2. These adjustments are used to convert input path times originally specified for the LVCMOS25 standard to times that correspond to other signal standards.

Table 26: **Test Methods for Timing Measurement at I/Os**

Signal Standard (IOSTANDARD)		Inputs			Outputs		Inputs and Outputs
		V_{REF} (V)	V_L (V)	V_H (V)	R_T (Ω)	V_T (V)	V_M (V)
Single-Ended							
LVTTL		–	0	3.3	1M	0	1.4
LVCMOS33		–	0	3.3	1M	0	1.65
LVCMOS25		–	0	2.5	1M	0	1.25
LVCMOS18		–	0	1.8	1M	0	0.9
LVCMOS15		–	0	1.5	1M	0	0.75
LVCMOS12		–	0	1.2	1M	0	0.6
PCI33_3	Rising	–	Note 3	Note 3	25	0	0.94
	Falling				25	3.3	2.03
HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
SSTL18_II		0.9	V_{REF} – 0.5	V_{REF} + 0.5	25	0.9	V_{REF}
SSTL2_I		1.25	V_{REF} – 0.75	V_{REF} + 0.75	50	1.25	V_{REF}
SSTL2_II		1.25	V_{REF} – 0.75	V_{REF} + 0.75	25	1.25	V_{REF}
SSTL3_I		1.5	V_{REF} – 0.75	V_{REF} + 0.75	50	1.5	V_{REF}
SSTL3_II		1.5	V_{REF} – 0.75	V_{REF} + 0.75	25	1.5	V_{REF}
Differential							
LVDS_25		–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVDS_33		–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
BLVDS_25		–	V_{ICM} – 0.125	V_{ICM} + 0.125	1M	0	V_{ICM}
MINI_LVDS_25		–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
MINI_LVDS_33		–	V_{ICM} – 0.125	V_{ICM} + 0.125	50	1.2	V_{ICM}
LVPECL_25		–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
LVPECL_33		–	V_{ICM} – 0.3	V_{ICM} + 0.3	N/A	N/A	V_{ICM}
RSDS_25		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
RSDS_33		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	1.2	V_{ICM}
TMDS_33		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	3.3	V_{ICM}
PPDS_25		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
PPDS_33		–	V_{ICM} – 0.1	V_{ICM} + 0.1	50	0.8	V_{ICM}
DIFF_HSTL_I		0.75	V_{REF} – 0.5	V_{REF} + 0.5	50	0.75	V_{REF}
DIFF_HSTL_III		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	1.5	V_{REF}
DIFF_HSTL_I_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_HSTL_II_18		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}
DIFF_HSTL_III_18		1.1	V_{REF} – 0.5	V_{REF} + 0.5	50	1.8	V_{REF}
DIFF_SSTL18_I		0.9	V_{REF} – 0.5	V_{REF} + 0.5	50	0.9	V_{REF}

Simultaneously Switching Output Guidelines

This section provides guidelines for the recommended maximum allowable number of Simultaneous Switching Outputs (SSOs). These guidelines describe the maximum number of user I/O pins of a given output signal standard that should simultaneously switch in the same direction, while maintaining a safe level of switching noise. Meeting these guidelines for the stated test conditions ensures that the FPGA operates free from the adverse effects of ground and power bounce.

Ground or power bounce occurs when a large number of outputs simultaneously switch in the same direction. The output drive transistors all conduct current to a common voltage rail. Low-to-High transitions conduct to the V_{CCO} rail; High-to-Low transitions conduct to the GND rail. The resulting cumulative current transient induces a voltage difference across the inductance that exists between the die pad and the power supply or ground return. The inductance is associated with bonding wires, the package lead frame, and any other signal routing inside the package. Other variables contribute to SSO noise levels, including stray inductance on the PCB as well as capacitive loading at receivers. Any SSO-induced voltage consequently affects internal switching noise margins and ultimately signal quality.

Table 27 and Table 28 provide the essential SSO guidelines. For each device/package combination, Table 27 provides the number of equivalent V_{CCO}/GND pairs. For each output signal standard and drive strength, Table 28 recommends the maximum number of SSOs, switching in the same direction, allowed per V_{CCO}/GND pair within an I/O bank. The guidelines in Table 28 are categorized by package style, slew rate, and output drive current. Furthermore, the number of SSOs is specified by I/O bank. Generally, the left and right I/O banks (Banks 1 and 3) support higher output drive current.

Multiply the appropriate numbers from Table 27 and Table 28 to calculate the maximum number of SSOs allowed within an I/O bank. Exceeding these SSO guidelines might result in increased power or ground bounce, degraded signal integrity, or increased system jitter.

SSO_{MAX}/IO Bank = Table 27 x Table 28

The recommended maximum SSO values assumes that the FPGA is soldered on the printed circuit board and that the board uses sound design practices. The SSO values do not apply for FPGAs mounted in sockets, due to the lead inductance introduced by the socket.

Ball grid array packages are recommended for applications with a large number of simultaneously switching outputs.

Table 27: **Equivalent V_{CCO}/GND Pairs per Bank**

Device	Package Style *(Pb-free)*		
	FTG256	FGG400	FGG484
XA3S200A	4	–	–
XA3S400A	4	5	–
XA3S700A	–	5	5
XA3S1400A	–	–	6

Table 28: **Recommended Number of Simultaneously Switching Outputs per V_{CCO}/GND Pair (V_{CCAUX}=3.3V)**

Signal Standard (IOSTANDARD)			Package Type: FTG256, FGG400, FGG484	
			Top, Bottom (Banks 0,2)	Left, Right (Banks 1,3)
Single-Ended Standards				
LVTTL	Slow	2	60	60
		4	41	41
		6	29	29
		8	22	22
		12	13	13
		16	11	11
		24	9	9
	Fast	2	10	10
		4	6	6
		6	5	5
		8	3	3
		12	3	3
		16	3	3
		24	2	2
	QuietIO	2	80	80
		4	48	48
		6	36	36
		8	27	27
		12	16	16
		16	13	13
		24	12	12
LVCMOS33	Slow	2	76	76
		4	46	46
		6	27	27
		8	20	20
		12	13	13
		16	10	10
		24	–	9
	Fast	2	10	10
		4	8	8
		6	5	5
		8	4	4
		12	4	4
		16	2	2
		24	–	2
	QuietIO	2	76	76
		4	46	46
		6	32	32
		8	26	26
		12	18	18
		16	14	14
		24	–	10

Configurable Logic Block (CLB) Timing

Table 29: **CLB (SLICEM) Timing**

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Clock-to-Output Times				
T_{CKO}	When reading from the FFX (FFY) Flip-Flop, the time from the active transition at the CLK input to data appearing at the XQ (YQ) output	–	0.68	ns
Setup Times				
T_{AS}	Time from the setup of data at the F or G input to the active transition at the CLK input of the CLB	0.36	–	ns
T_{DICK}	Time from the setup of data at the BX or BY input to the active transition at the CLK input of the CLB	1.88	–	ns
Hold Times				
T_{AH}	Time from the active transition at the CLK input to the point where data is last held at the F or G input	0	–	ns
T_{CKDI}	Time from the active transition at the CLK input to the point where data is last held at the BX or BY input	0	–	ns
Clock Timing				
T_{CH}	The High pulse width of the CLB's CLK signal	0.75	–	ns
T_{CL}	The Low pulse width of the CLK signal	0.75	–	ns
F_{TOG}	Toggle frequency (for export control)	0	667	MHz
Propagation Times				
T_{ILO}	The time it takes for data to travel from the CLB's F (G) input to the X (Y) output	–	0.71	ns
Set/Reset Pulse Width				
T_{RPW_CLB}	The minimum allowable pulse width, High or Low, to the CLB's SR input	1.61	–	ns

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.

Table 30: **CLB Distributed RAM Switching Characteristics**

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Clock-to-Output Times				
T_{SHCKO}	Time from the active edge at the CLK input to data appearing on the distributed RAM output	–	2.01	ns
Setup Times				
T_{DS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the distributed RAM	–0.02	–	ns
T_{AS}	Setup time of the F/G address inputs before the active transition at the CLK input of the distributed RAM	0.36	–	ns
T_{WS}	Setup time of the write enable input before the active transition at the CLK input of the distributed RAM	0.59	–	ns
Hold Times				
T_{DH}	Hold time of the BX and BY data inputs after the active transition at the CLK input of the distributed RAM	0.13	–	ns
T_{AH}, T_{WH}	Hold time of the F/G address inputs or the write enable input after the active transition at the CLK input of the distributed RAM	0.01	–	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	–	ns

Table 31: **CLB Shift Register Switching Characteristics**

Symbol	Description	Speed Grade: -4		Units
		Min	Max	
Clock-to-Output Times				
T_{REG}	Time from the active edge at the CLK input to data appearing on the shift register output	–	4.82	ns
Setup Times				
T_{SRLDS}	Setup time of data at the BX or BY input before the active transition at the CLK input of the shift register	0.18	–	ns
Hold Times				
T_{SRLDH}	Hold time of the BX or BY data input after the active transition at the CLK input of the shift register	0.16	–	ns
Clock Pulse Width				
T_{WPH}, T_{WPL}	Minimum High or Low pulse width at CLK input	1.01	–	ns

Suspend Mode Timing

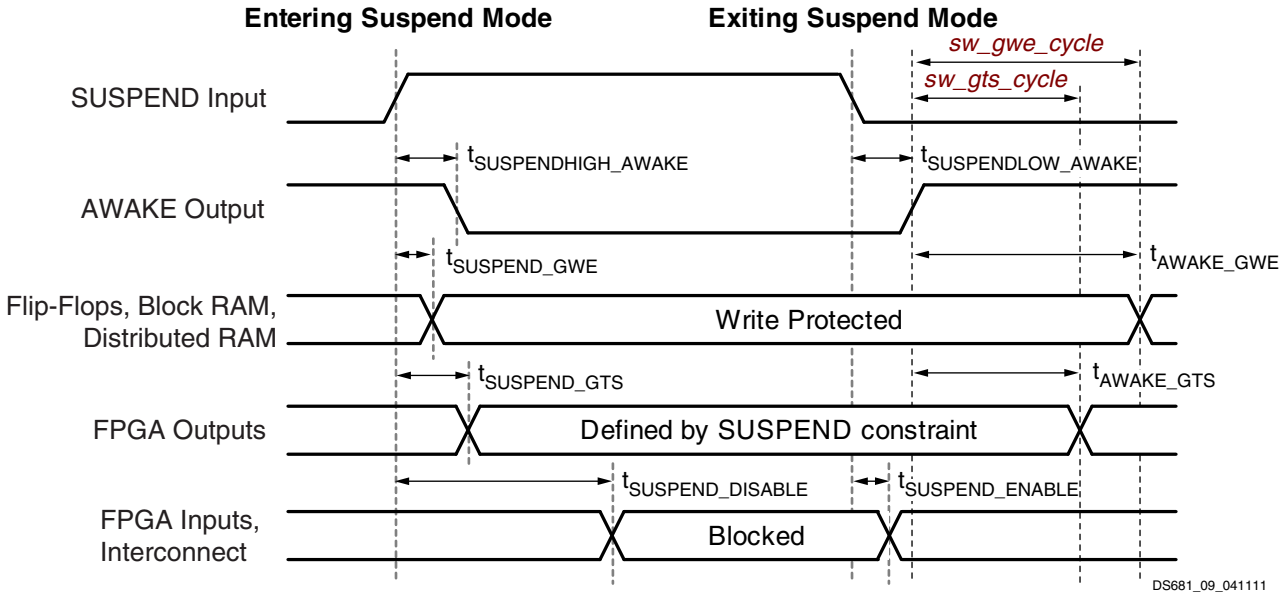


Figure 10: **Suspend Mode Timing**

Table 43: **Suspend Mode Timing Parameters**

Symbol	Description	Min	Typ	Max	Units
Entering Suspend Mode					
$T_{SUSPENDHIGH\_AWAKE}$	Rising edge of SUSPEND pin to falling edge of AWAKE pin without glitch filter (***suspend_filter:No***)	–	7	–	ns
$T_{SUSPENDFILTER}$	Adjustment to SUSPEND pin rising edge parameters when glitch filter enabled (***suspend_filter:Yes***)	+160	+300	+600	ns
$T_{SUSPEND\_GTS}$	Rising edge of SUSPEND pin until FPGA output pins drive their defined SUSPEND constraint behavior	–	10	–	ns
$T_{SUSPEND\_GWE}$	Rising edge of SUSPEND pin to write-protect lock on all writable clocked elements	–	<5	–	ns
$T_{SUSPEND\_DISABLE}$	Rising edge of the SUSPEND pin to FPGA input pins and interconnect disabled	–	340	–	ns
Exiting Suspend Mode					
$T_{SUSPENDLOW\_AWAKE}$	Falling edge of the SUSPEND pin to rising edge of the AWAKE pin. Does not include DCM lock time.	–	4 to 108	–	µs
$T_{SUSPEND\_ENABLE}$	Falling edge of the SUSPEND pin to FPGA input pins and interconnect re-enabled	–	3.7 to 109	–	µs
T_{AWAKE_GWE1}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:1***.	–	67	–	ns
T_{AWAKE_GWE512}	Rising edge of the AWAKE pin until write-protect lock released on all writable clocked elements, using ***sw_clk:InternalClock*** and ***sw_gwe_cycle:512***.	–	14	–	µs
T_{AWAKE_GTS1}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:1***.	–	57	–	ns
T_{AWAKE_GTS512}	Rising edge of the AWAKE pin until outputs return to the behavior described in the FPGA application, using ***sw_clk:InternalClock*** and ***sw_gts_cycle:512***.	–	14	–	µs

Notes:

1. These parameters based on characterization.
2. For information on using the Spartan-3A Suspend feature, see XAPP480: *Using Suspend Mode in Spartan-3 Generation FPGAs*.

Table 52: **Configuration Timing Requirements for Attached SPI Serial Flash**

Symbol	Description	Requirement	Units
T_{CCS}	SPI serial Flash PROM chip-select time	$T_{CCS} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DSU}	SPI serial Flash PROM data input setup time	$T_{DSU} \leq T_{MCCL1} - T_{CCO}$	ns
T_{DH}	SPI serial Flash PROM data input hold time	$T_{DH} \leq T_{MCCH1}$	ns
T_V	SPI serial Flash PROM data clock-to-output time	$T_V \leq T_{MCCLn} - T_{DCC}$	ns
f_C or f_R	Maximum SPI serial Flash PROM clock frequency (also depends on specific read command used)	$f_C \geq \frac{1}{T_{CCLKn(min)}}$	MHz

Notes:

1. These requirements are for successful FPGA configuration in SPI mode, where the FPGA generates the CCLK signal. The post-configuration timing can be different to support the specific needs of the application loaded into the FPGA.
2. Subtract additional printed circuit board routing delay as required by the application.

IEEE 1149.1/1532 JTAG Test Access Port Timing

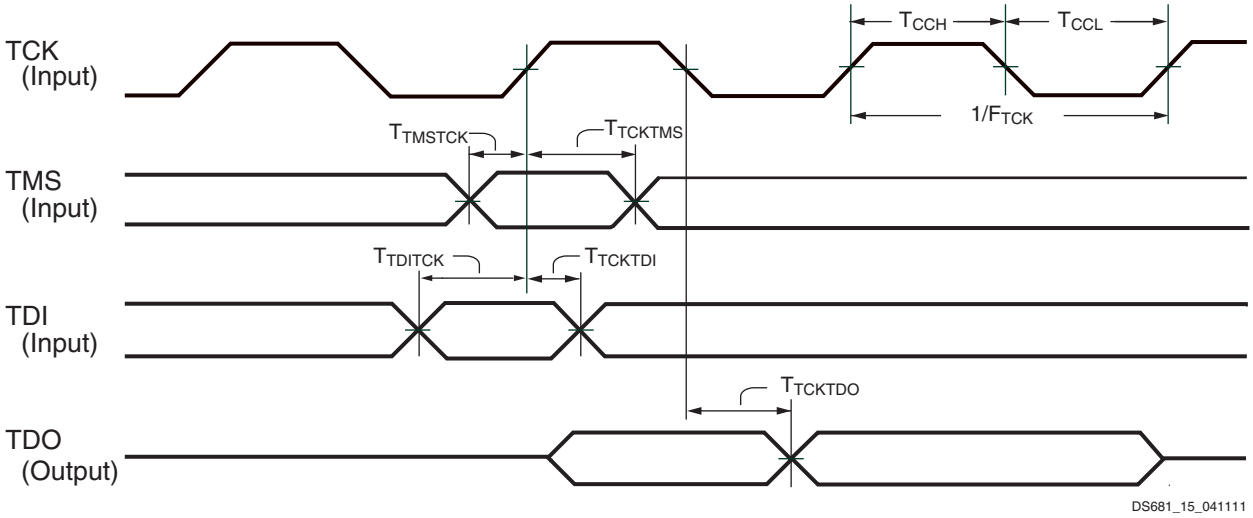


Figure 16: **JTAG Waveforms**

Table 55: **Timing for the JTAG Test Access Port**

Symbol	Description		Speed Grade: -4		Units
			Min	Max	
Clock-to-Output Times					
T_{TCKTDO}	The time from the falling transition on the TCK pin to data appearing at the TDO pin		1.0	11.0	ns
Setup Times					
T_{TDITCK}	The time from the setup of data at the TDI pin to the rising transition at the TCK pin	All devices and functions except those shown below	7.0	–	ns
		Boundary scan commands (INTEST, EXTEST, SAMPLE) on XA3S700A and XA3S1400A FPGAs	11.0		
T_{TMSTCK}	The time from the setup of a logic level at the TMS pin to the rising transition at the TCK pin		7.0	–	ns
Hold Times					
T_{TCKTDI}	The time from the rising transition at the TCK pin to the point when data is last held at the TDI pin	All functions except those shown below	0	–	ns
		Configuration commands (CFG_IN, ISC_PROGRAM)	2.0		
T_{TCKTMS}	The time from the rising transition at the TCK pin to the point when a logic level is last held at the TMS pin		0	–	ns
Clock Timing					
T_{CCH}	The High pulse width at the TCK pin	All functions except ISC_DNA command	5	–	ns
T_{CCL}	The Low pulse width at the TCK pin		5	–	ns
T_{CCHDNA}	The High pulse width at the TCK pin	During ISC_DNA command	10	10,000	ns
T_{CCLDNA}	The Low pulse width at the TCK pin		10	10,000	ns
F_{TCK}	Frequency of the TCK signal	All operations on XA3S200A and XA3S400A FPGAs and for BYPASS or HIGHZ instructions on all FPGAs	0	33	MHz
		All operations on XA3S700A and XA3S1400A FPGAs, except for BYPASS or HIGHZ instructions		20	

Notes:

1. The numbers in this table are based on the operating conditions set forth in Table 8.