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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	EBI/EMI, I <sup>2</sup> C, IrDA, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT
Number of I/O	79
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.6V
Data Converters	A/D 15x10/12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TFBGA
Supplier Device Package	100-TFBGA (9x9)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/atmel/atsam3sd8ca-cu">https://www.e-xfl.com/product-detail/atmel/atsam3sd8ca-cu</a>

**Table 9-1. Peripheral Identifiers (Continued)**

Instance ID	Instance Name	NVIC Interrupt	PMC Clock Control	Instance Description
31	PWM	X	X	Pulse Width Modulation
32	CRCCU	X	X	CRC Calculation Unit
33	ACC	X	X	Analog Comparator
34	UDP	X	X	USB Device Port

## 9.2 APB/AHB Bridge

The SAM3S8/SD8 embeds One Peripheral Bridge. The peripherals of the bridge are clocked by MCK.

## 9.3 Peripheral Signal Multiplexing on I/O Lines

The SAM3S8/SD8 features two PIO controllers on 64-pin versions (PIOA and PIOB) or three PIO controllers on the 100-pin version (PIOA, PIOB and PIOC), that multiplex the I/O lines of the peripheral set.

The SAM3S8/SD8 64-pin and 100-pin PIO Controllers control up to 32 lines. Each line can be assigned to one of three peripheral functions: A, B or C. The multiplexing tables in the following tables define how the I/O lines of the peripherals A, B and C are multiplexed on the PIO Controllers.

Note that some peripheral functions which are output only, might be duplicated within the tables.

- **PRIMASK**

0 = no effect

1 = prevents the activation of all exceptions with configurable priority.

### 10.3.3.13 Fault Mask Register

The FAULTMASK register prevents activation of all exceptions. See the register summary in Table 10-2 on page 41 for its attributes. The bit assignments are:

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							FAULTMASK

- **FAULTMASK**

0 = no effect

1 = prevents the activation of all exceptions.

The processor clears the FAULTMASK bit to 0 on exit from any exception handler except the NMI handler.

- **WKUPDBC: Wake Up Inputs Debouncer Period**

Value	Name	Description
0	IMMEDIATE	Immediate, no debouncing, detected active at least on one Slow Clock edge.
1	3_SCLK	WKUPx shall be in its active state for at least 3 SCLK periods
2	32_SCLK	WKUPx shall be in its active state for at least 32 SCLK periods
3	512_SCLK	WKUPx shall be in its active state for at least 512 SCLK periods
4	4096_SCLK	WKUPx shall be in its active state for at least 4,096 SCLK periods
5	32768_SCLK	WKUPx shall be in its active state for at least 32,768 SCLK periods
6	Reserved	Reserved
7	Reserved	Reserved

- **LPDBC: Low Power DeBouncer Period**

Value	Name	Description
0	DISABLE	Disable the low power debouncer.
1	2_RTCOUT0	WKUP0/1 in its active state for at least 2 RTCOUT0 periods
2	3_RTCOUT0	WKUP0/1 in its active state for at least 3 RTCOUT0 periods
3	4_RTCOUT0	WKUP0/1 in its active state for at least 4 RTCOUT0 periods
4	5_RTCOUT0	WKUP0/1 in its active state for at least 5 RTCOUT0 periods
5	6_RTCOUT0	WKUP0/1 in its active state for at least 6 RTCOUT0 periods
6	7_RTCOUT0	WKUP0/1 in its active state for at least 7 RTCOUT0 periods
7	8_RTCOUT0	WKUP0/1 in its active state for at least 8 RTCOUT0 periods

## 23.11 Data Float Wait States

Some memory devices are slow to release the external bus. For such devices, it is necessary to add wait states (data float wait states) after a read access:

- before starting a read access to a different external memory
- before starting a write access to the same device or to a different external one.

The Data Float Output Time ( $t_{DF}$ ) for each external memory device is programmed in the TDF\_CYCLES field of the SMC\_MODE register for the corresponding chip select. The value of TDF\_CYCLES indicates the number of data float wait cycles (between 0 and 15) before the external device releases the bus, and represents the time allowed for the data output to go to high impedance after the memory is disabled.

Data float wait states do not delay internal memory accesses. Hence, a single access to an external memory with long  $t_{DF}$  will not slow down the execution of a program from internal memory.

The data float wait states management depends on the READ\_MODE and the TDF\_MODE fields of the SMC\_MODE register for the corresponding chip select.

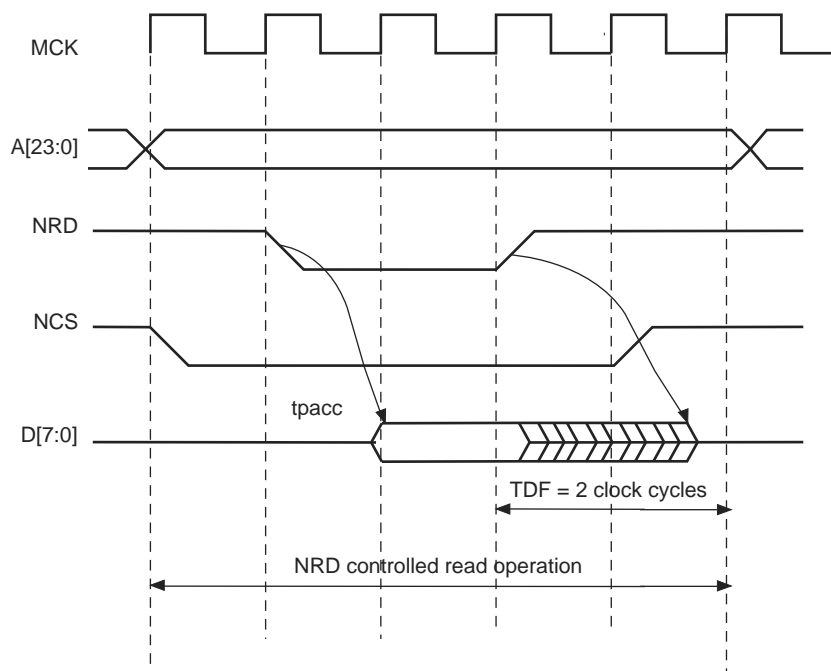
### 23.11.1 READ\_MODE

Setting the READ\_MODE to 1 indicates to the SMC that the NRD signal is responsible for turning off the tri-state buffers of the external memory device. The Data Float Period then begins after the rising edge of the NRD signal and lasts TDF\_CYCLES MCK cycles.

When the read operation is controlled by the NCS signal (READ\_MODE = 0), the TDF field gives the number of MCK cycles during which the data bus remains busy after the rising edge of NCS.

Figure 23-17 illustrates the Data Float Period in NRD-controlled mode (READ\_MODE = 1), assuming a data float period of 2 cycles (TDF\_CYCLES = 2). Figure 23-18 shows the read operation when controlled by NCS (READ\_MODE = 0) and the TDF\_CYCLES parameter equals 3.

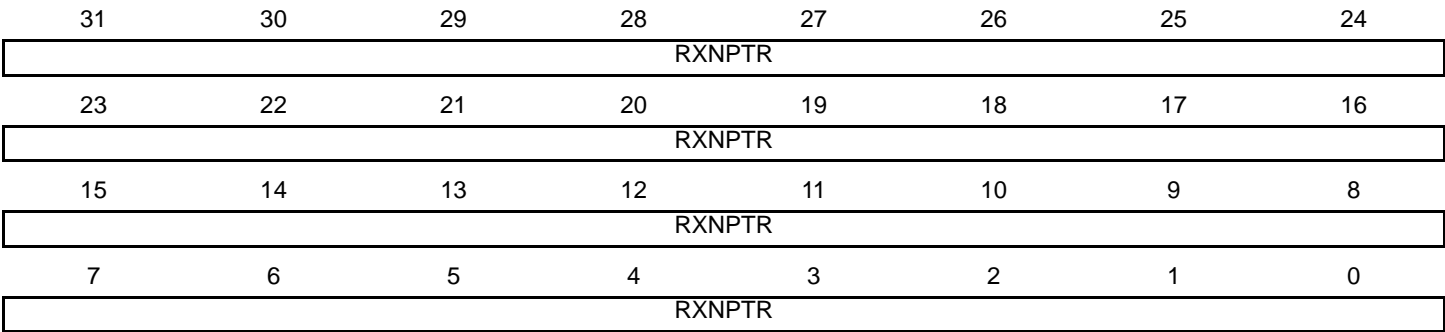
Figure 23-17. TDF Period in NRD Controlled Read Access (TDF = 2)



24.5.5 Receive Next Pointer Register

Name: PERIPH\_RNPR

Access: Read-write



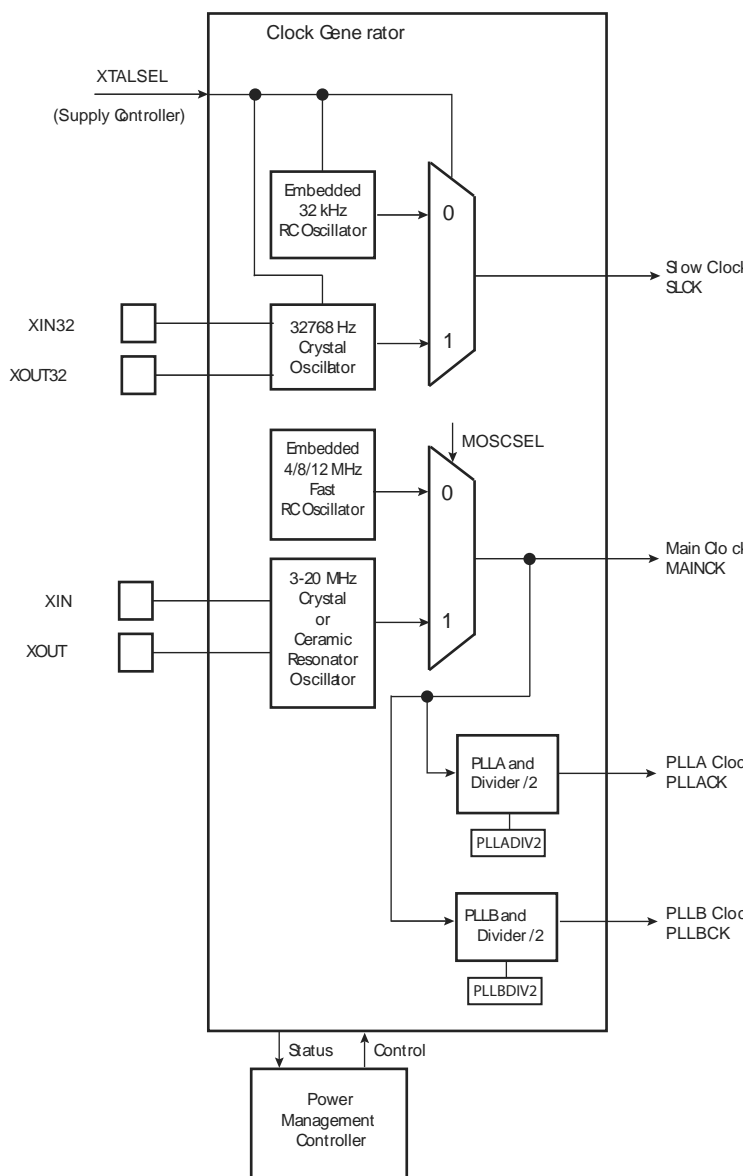
• RXNPTR: Receive Next Pointer

RXNPTR contains next receive buffer address.

When a half duplex peripheral is connected to the PDC, RXNPTR = TXNPTR.

## 25.3 Block Diagram

Figure 25-1. Clock Generator Block Diagram



## 25.4 Slow Clock

The Supply Controller embeds a slow clock generator that is supplied with the VDDIO power supply. As soon as the VDDIO is supplied, both the crystal oscillator and the embedded RC oscillator are powered up, but only the embedded RC oscillator is enabled. This allows the slow clock to be valid in a short time (about 100  $\mu$ s).

The Slow Clock is generated either by the Slow Clock Crystal Oscillator or by the Slow Clock RC Oscillator.

The selection between the RC or the crystal oscillator is made by writing the XTALSEL bit in the Supply Controller Control Register (SUPC\_CR).

- **CFDEV: Clock Failure Detector Event**

0 = No clock failure detection of the main on-chip RC oscillator clock has occurred since the last read of PMC\_SR.

1 = At least one clock failure detection of the main on-chip RC oscillator clock has occurred since the last read of PMC\_SR.

- **CFDS: Clock Failure Detector Status**

0 = A clock failure of the main on-chip RC oscillator clock is not detected.

1 = A clock failure of the main on-chip RC oscillator clock is detected.

- **FOS: Clock Failure Detector Fault Output Status**

0 = The fault output of the clock failure detector is inactive.

1 = The fault output of the clock failure detector is active.



### 28.7.19 PIO Multi-driver Disable Register

**Name:** PIO\_MDDR

**Address:** 0x400E0E54 (PIOA), 0x400E1054 (PIOB), 0x400E1254 (PIOC)

**Access:** Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

This register can only be written if the WPEN bit is cleared in “PIO Write Protect Mode Register” .

- **P0-P31: Multi Drive Disable.**

0: No effect.

1: Disables Multi Drive on the I/O line.

## 28.7.26 PIO Input Filter Slow Clock Disable Register

**Name:** PIO\_IFSCDR

**Address:** 0x400E0E80 (PIOA), 0x400E1080 (PIOB), 0x400E1280 (PIOC)

**Access:** Write-only

31	30	29	28	27	26	25	24
P31	P30	P29	P28	P27	P26	P25	P24
23	22	21	20	19	18	17	16
P23	P22	P21	P20	P19	P18	P17	P16
15	14	13	12	11	10	9	8
P15	P14	P13	P12	P11	P10	P9	P8
7	6	5	4	3	2	1	0
P7	P6	P5	P4	P3	P2	P1	P0

- **P0-P31: PIO Clock Glitch Filtering Select.**

0: No Effect.

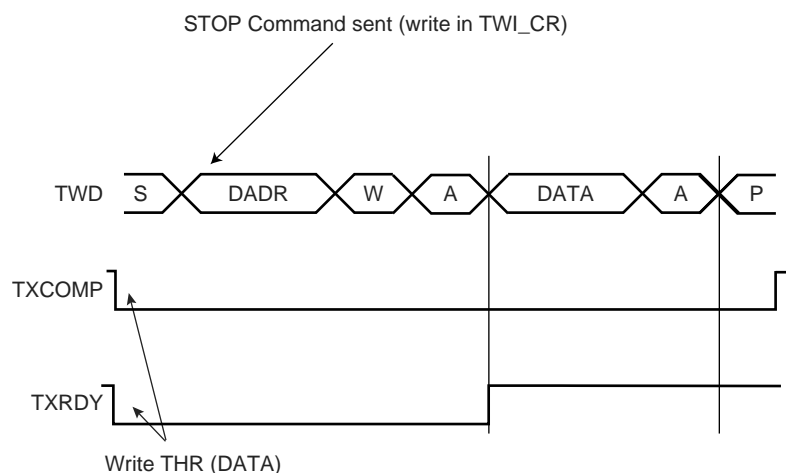
1: The Glitch Filter is able to filter glitches with a duration  $< T_{mck}/2$ .

While no new data is written in the TWI\_THR, the Serial Clock Line is tied low. When new data is written in the TWI\_THR, the SCL is released and the data is sent. To generate a STOP event, the STOP command must be performed by writing in the STOP field of TWI\_CR.

After a Master Write transfer, the Serial Clock line is stretched (tied low) while no new data is written in the TWI\_THR or until a STOP command is performed.

See Figure 30-6, Figure 30-7, and Figure 30-8.

**Figure 30-6. Master Write with One Data Byte**



**Figure 30-7. Master Write with Multiple Data Bytes**

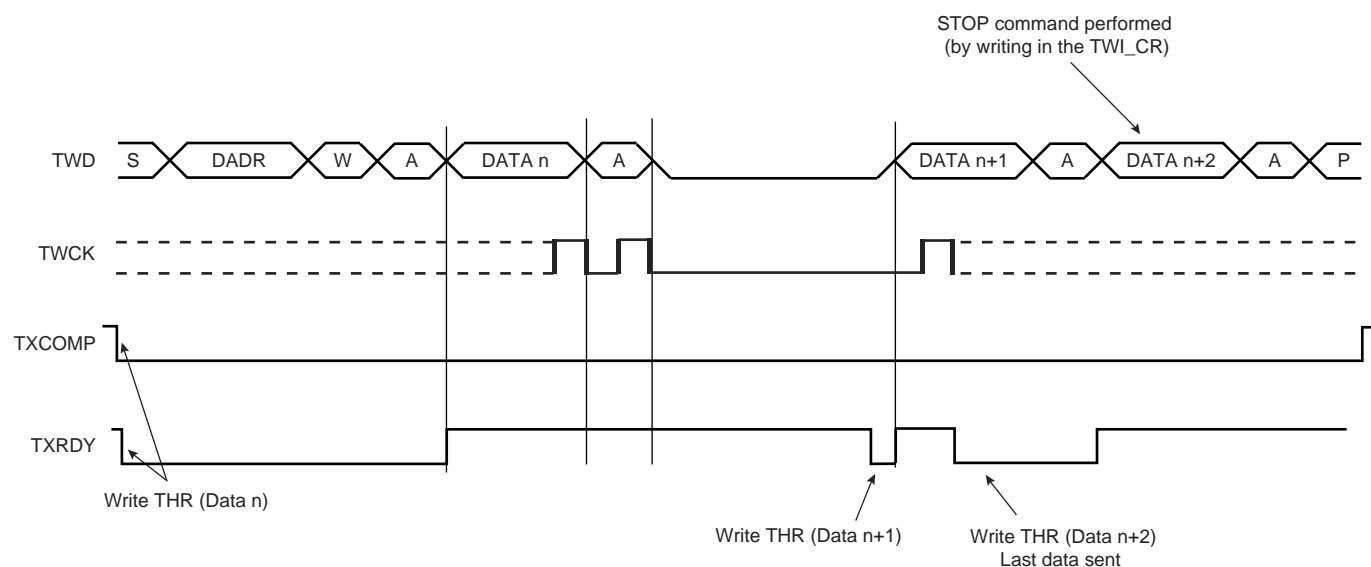
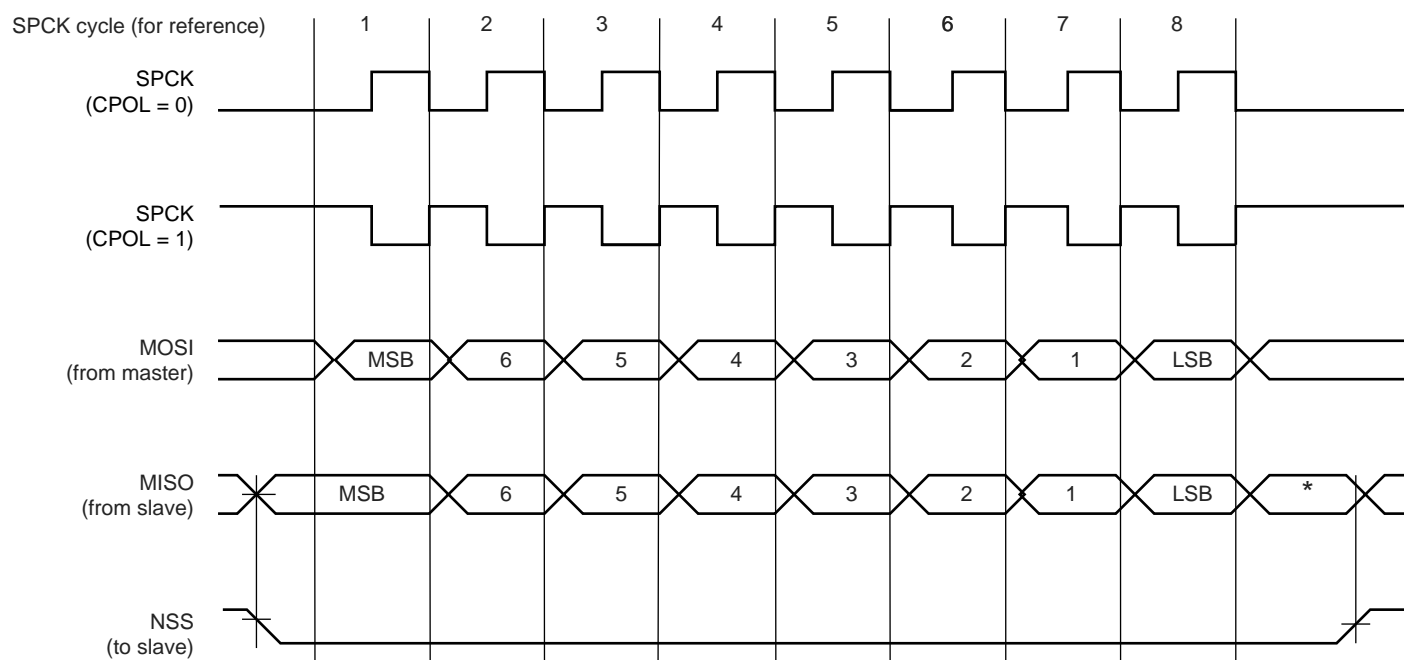


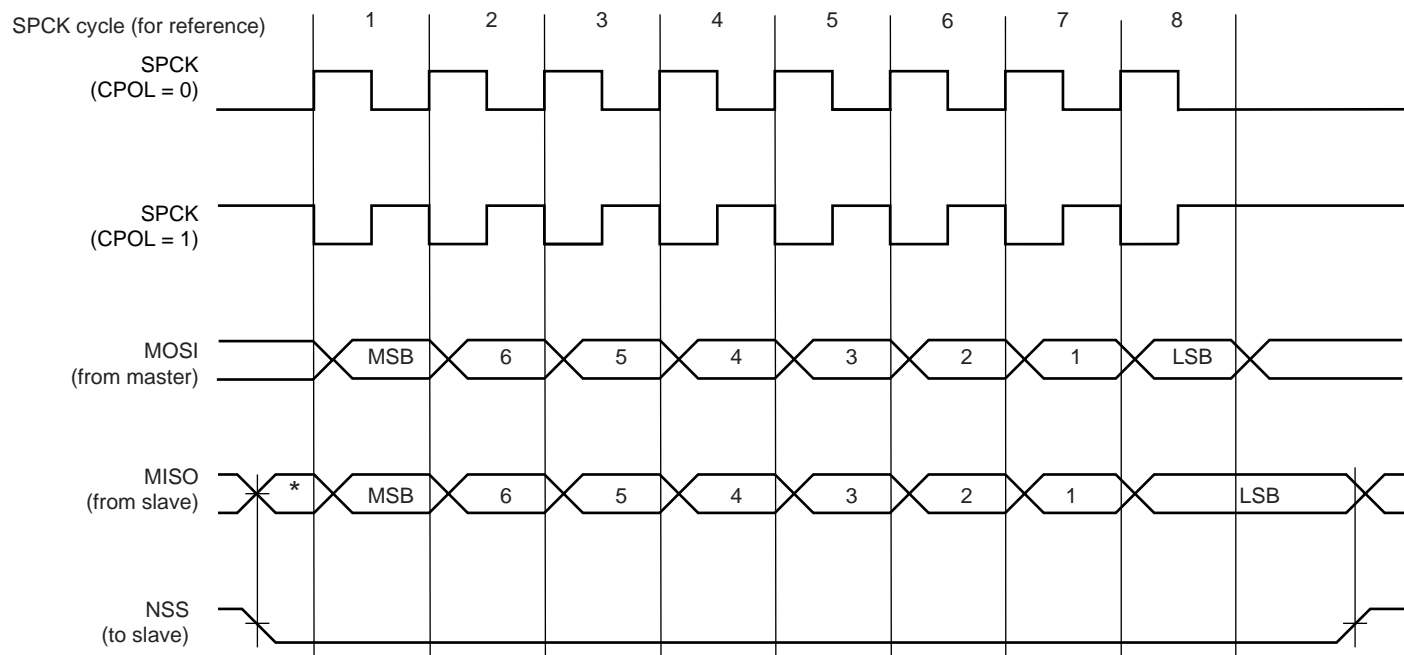
Figure 31-3 and Figure 31-4 show examples of data transfers.

**Figure 31-3. SPI Transfer Format (NCPHA = 1, 8 bits per transfer)**



\* Not defined, but normally MSB of previous character received.

**Figure 31-4. SPI Transfer Format (NCPHA = 0, 8 bits per transfer)**

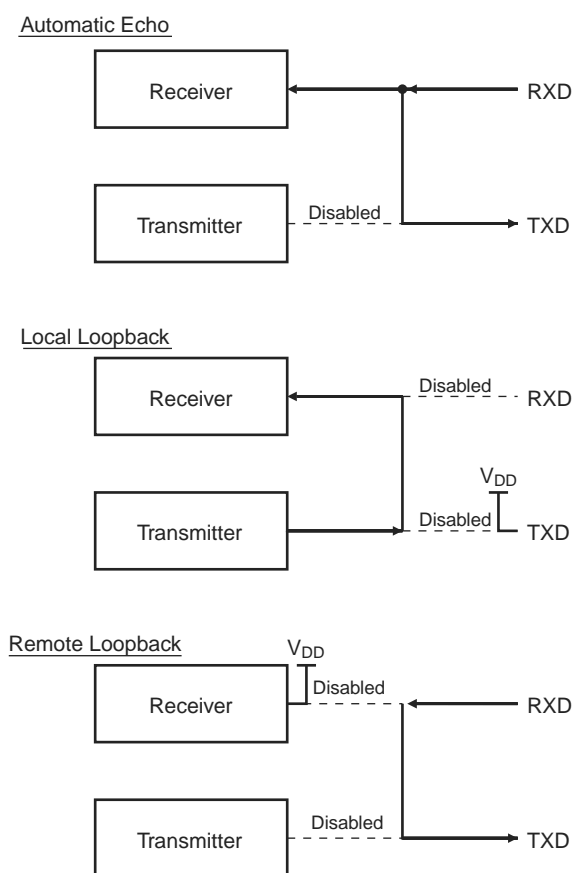


\* Not defined but normally LSB of previous character transmitted.

The Local Loopback mode allows the transmitted characters to be received. UTXD and URXD pins are not used and the output of the transmitter is internally connected to the input of the receiver. The URXD pin level has no effect and the UTXD line is held high, as in idle state.

The Remote Loopback mode directly connects the URXD pin to the UTXD line. The transmitter and the receiver are disabled and have no effect. This mode allows a bit-by-bit retransmission.

**Figure 32-11. Test Modes**

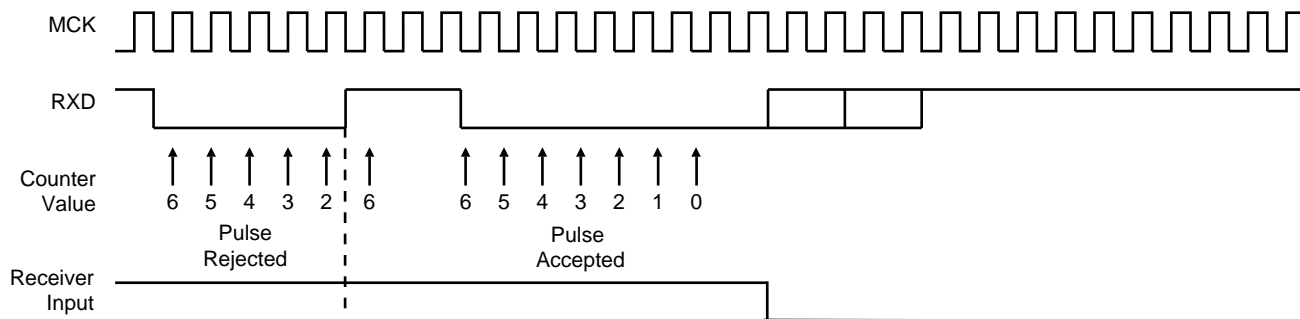


### 33.7.5.3 IrDA Demodulator

The demodulator is based on the IrDA Receive filter comprised of an 8-bit down counter which is loaded with the value programmed in US\_IF. When a falling edge is detected on the RXD pin, the Filter Counter starts counting down at the Master Clock (MCK) speed. If a rising edge is detected on the RXD pin, the counter stops and is reloaded with US\_IF. If no rising edge is detected when the counter reaches 0, the input of the receiver is driven low during one bit time.

Figure 33-35 illustrates the operations of the IrDA demodulator.

**Figure 33-35. IrDA Demodulator Operations**



As the IrDA mode uses the same logic as the ISO7816, note that the FI\_DI\_RATIO field in US\_FIDI must be set to a value higher than 0 in order to assure IrDA communications operate correctly.

- **PARE: Parity Error**

0: No parity error has been detected since the last RSTSTA.

1: At least one parity error has been detected since the last RSTSTA.

- **TIMEOUT: Receiver Time-out**

0: There has not been a time-out since the last Start Time-out command (STTTO in US\_CR) or the Time-out Register is 0.

1: There has been a time-out since the last Start Time-out command (STTTO in US\_CR).

- **TXEMPTY: Transmitter Empty**

0: There are characters in either US\_THR or the Transmit Shift Register, or the transmitter is disabled.

1: There are no characters in US\_THR, nor in the Transmit Shift Register.

- **ITER: Max number of Repetitions Reached**

0: Maximum number of repetitions has not been reached since the last RSTSTA.

1: Maximum number of repetitions has been reached since the last RSTSTA.

- **UNRE: SPI Underrun Error**

– Applicable if USART operates in SPI Slave Mode (USART\_MODE = 0xF):

UNRE = 0: No SPI underrun error has occurred since the last RSTSTA.

UNRE = 1: At least one SPI underrun error has occurred since the last RSTSTA.

- **TXBUFE: Transmission Buffer Empty**

0: The signal Buffer Empty from the Transmit PDC channel is inactive.

1: The signal Buffer Empty from the Transmit PDC channel is active.

- **RXBUFF: Reception Buffer Full**

0: The signal Buffer Full from the Receive PDC channel is inactive.

1: The signal Buffer Full from the Receive PDC channel is active.

- **NACK: Non Acknowledge Interrupt**

0: Non Acknowledge has not been detected since the last RSTNACK.

1: At least one Non Acknowledge has been detected since the last RSTNACK.

- **RIIC: Ring Indicator Input Change Flag**

0: No input change has been detected on the RI pin since the last read of US\_CSR.

1: At least one input change has been detected on the RI pin since the last read of US\_CSR.

- **DSRIC: Data Set Ready Input Change Flag**

0: No input change has been detected on the DSR pin since the last read of US\_CSR.

1: At least one input change has been detected on the DSR pin since the last read of US\_CSR.

- **DCDIC: Data Carrier Detect Input Change Flag**

0: No input change has been detected on the DCD pin since the last read of US\_CSR.

1: At least one input change has been detected on the DCD pin since the last read of US\_CSR.

## 34.6 Functional Description

### 34.6.1 TC Description

The 6 channels of the Timer Counter are independent and identical in operation except when quadrature decoder is enabled. The registers for channel programming are listed in Table 34-5 on page 781.

### 34.6.2 16-bit Counter

Each channel is organized around a 16-bit counter. The value of the counter is incremented at each positive edge of the selected clock. When the counter has reached the value 0xFFFF and passes to 0x0000, an overflow occurs and the COVFS bit in TC\_SR (Status Register) is set.

The current value of the counter is accessible in real time by reading the Counter Value Register, TC\_CV. The counter can be reset by a trigger. In this case, the counter value passes to 0x0000 on the next valid edge of the selected clock.

### 34.6.3 Clock Selection

At block level, input clock signals of each channel can either be connected to the external inputs TCLK0, TCLK1 or TCLK2, or be connected to the internal I/O signals TIOA0, TIOA1 or TIOA2 for chaining by programming the TC\_BMR (Block Mode). See Figure 34-2 "Clock Chaining Selection".

Each channel can independently select an internal or external clock source for its counter:

- Internal clock signals: TIMER\_CLOCK1, TIMER\_CLOCK2, TIMER\_CLOCK3, TIMER\_CLOCK4, TIMER\_CLOCK5
- External clock signals: XC0, XC1 or XC2

This selection is made by the TCCLKS bits in the TC Channel Mode Register.

The selected clock can be inverted with the CLKI bit in TC\_CMR. This allows counting on the opposite edges of the clock.

The burst function allows the clock to be validated when an external signal is high. The BURST parameter in the Mode Register defines this signal (none, XC0, XC1, XC2). See Figure 34-3 "Clock Selection"

Note: In all cases, if an external clock is used, the duration of each of its levels must be longer than the master clock period. The external clock frequency must be at least 2.5 times lower than the master clock



The field UPDM (Update Mode) in the PWM\_SCM register allow to select one of the three methods to update the registers of the synchronous channels:

- Method 1 (UPDM = 0): the period value, the duty-cycle values and the dead-time values must be written by the CPU in their respective update registers (respectively PWM\_CPRDUPDx, PWM\_CDTYUPDx and PWM\_DTUPDx). The update is triggered at the next PWM period as soon as the bit UPDULOCK in the “PWM Sync Channels Update Control Register” (PWM\_SCUC) is set to 1 (see “Method 1: Manual write of duty-cycle values and manual trigger of the update” on page 869).
- Method 2 (UPDM = 1): the period value, the duty-cycle values, the dead-time values and the update period value must be written by the CPU in their respective update registers (respectively PWM\_CPRDUPDx, PWM\_CDTYUPDx and PWM\_DTUPD). The update of the period value and of the dead-time values is triggered at the next PWM period as soon as the bit UPDULOCK in the “PWM Sync Channels Update Control Register” (PWM\_SCUC) is set to 1. The update of the duty-cycle values and the update period value is triggered automatically after an update period defined by the field UPR in the “PWM Sync Channels Update Period Register” (PWM\_SCUP) (see “Method 2: Manual write of duty-cycle values and automatic trigger of the update” on page 870).
- Method 3 (UPDM = 2): same as Method 2 apart from the fact that the duty-cycle values of ALL synchronous channels are written by the Peripheral DMA Controller (PDC) (see “Method 3: Automatic write of duty-cycle values and automatic trigger of the update” on page 872). The user can choose to synchronize the PDC transfer request with a comparison match (see Section 36.6.3 “PWM Comparison Units”), by the fields PTRM and PTRCS in the PWM\_SCM register.

**Table 36-5. Summary of the Update of Registers of Synchronous Channels**

	UPDM=0	UPDM=1	UPDM=2
Period Value (PWM_CPRDUPDx)	Write by the CPU		
	Update is triggered at the next PWM period as soon as the bit UPDULOCK is set to 1		
Dead-Time Values (PWM_DTUPDx)	Write by the CPU		
	Update is triggered at the next PWM period as soon as the bit UPDULOCK is set to 1		
Duty-Cycle Values (PWM_CDTYUPDx)	Write by the CPU	Write by the CPU	Write by the PDC
	Update is triggered at the next PWM period as soon as the bit UPDULOCK is set to 1	Update is triggered at the next PWM period as soon as the update period counter has reached the value UPR	
Update Period Value (PWM_SCUPUPD)	Not applicable	Write by the CPU	
	Not applicable	Update is triggered at the next PWM period as soon as the update period counter has reached the value UPR	

### 36.7.1 PWM Clock Register

**Name:** PWM\_CLK

**Address:** 0x40020000

**Access:** Read-write

31	30	29	28	27	26	25	24
–	–	–	–	PREB			
23	22	21	20	19	18	17	16
DIVB							
15	14	13	12	11	10	9	8
–	–	–	–	PREA			
7	6	5	4	3	2	1	0
DIVA							

This register can only be written if the bits WPSWS0 and WPHWS0 are cleared in “PWM Write Protect Status Register” on page 919.

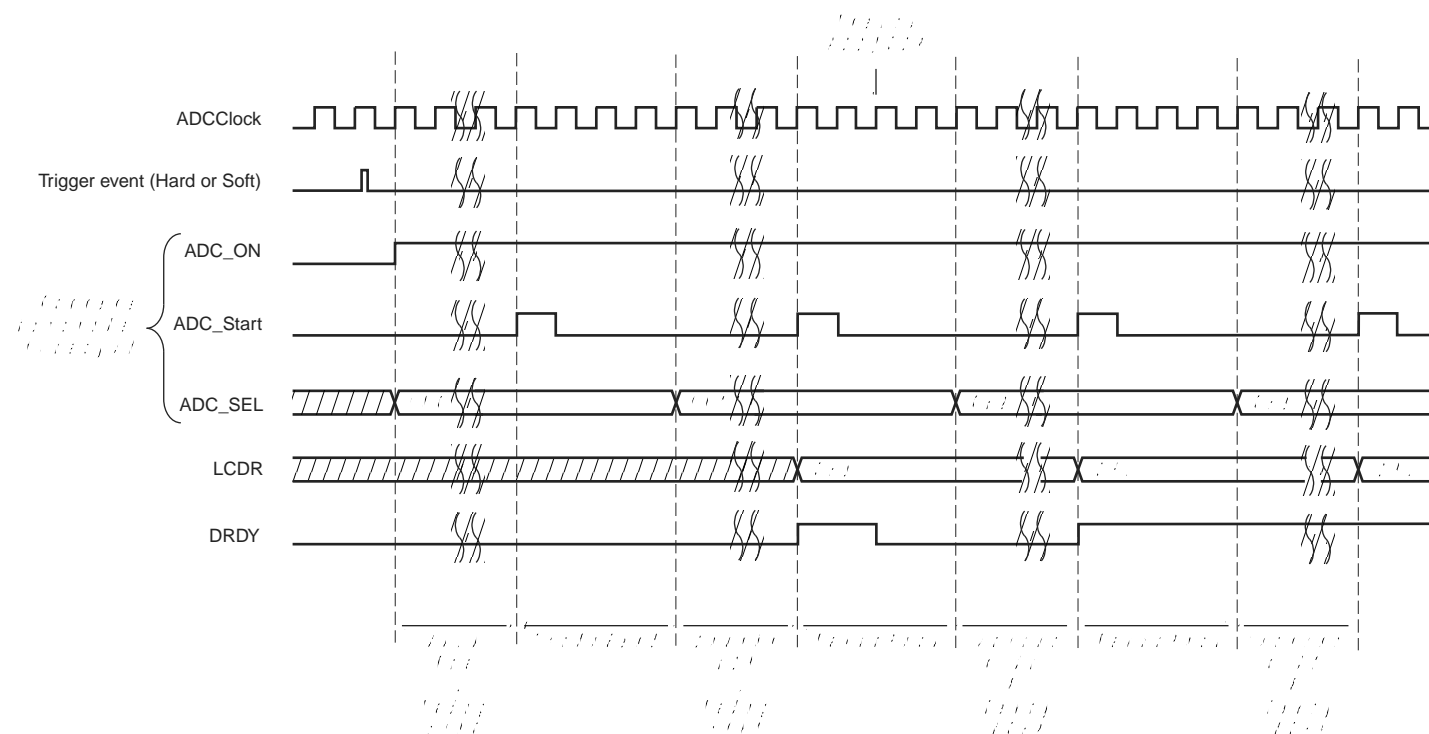
- DIVA, DIVB: CLKA, CLKB Divide Factor**

DIVA, DIVB	CLKA, CLKB
0	CLKA, CLKB clock is turned off
1	CLKA, CLKB clock is clock selected by PREA, PREB
2-255	CLKA, CLKB clock is clock selected by PREA, PREB divided by DIVA, DIVB factor.

- PREA, PREB: CLKA, CLKB Source Clock Selection**

PREA, PREB				Divider Input Clock
0	0	0	0	MCK
0	0	0	1	MCK/2
0	0	1	0	MCK/4
0	0	1	1	MCK/8
0	1	0	0	MCK/16
0	1	0	1	MCK/32
0	1	1	0	MCK/64
0	1	1	1	MCK/128
1	0	0	0	MCK/256
1	0	0	1	MCK/512
1	0	1	0	MCK/1024
Other				Reserved

**Figure 39-3. Sequence of ADC conversions when Tracking time < Conversion time**



### 39.6.2 Conversion Reference

The conversion is performed on a full range between 0V and the reference voltage pin ADVREF. Analog inputs between these voltages convert to values based on a linear conversion.

### 39.6.3 Conversion Resolution

The ADC supports 10-bit or 12-bit resolutions. The 10-bit selection is performed by setting the LOWRES bit in the ADC Mode Register (ADC\_MR). By default, after a reset, the resolution is the highest and the DATA field in the data registers is fully used. By setting the LOWRES bit, the ADC switches to the lowest resolution and the conversion results can be read in the lowest significant bits of the data registers. The two highest bits of the DATA field in the corresponding ADC\_CDR register and of the LDATA field in the ADC\_LCDR register read 0.

Moreover, when a PDC channel is connected to the ADC, 12-bit or 10-bit resolution sets the transfer request size to 16 bits.

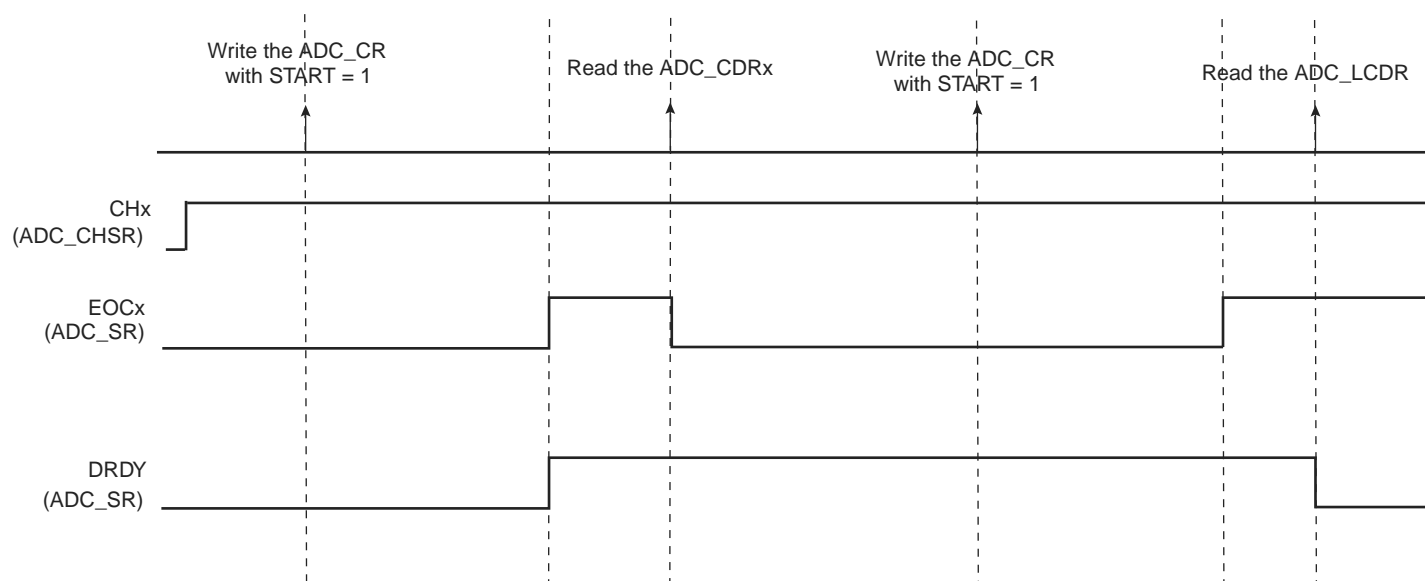
### 39.6.4 Conversion Results

When a conversion is completed, the resulting 12-bit digital value is stored in the Channel Data Register (ADC\_CDRx) of the current channel and in the ADC Last Converted Data Register (ADC\_LCDR). By setting the TAG option in the ADC\_EMR, the ADC\_LCDR presents the channel number associated to the last converted data in the CHNB field.

The channel EOC bit in the Status Register (ADC\_SR) is set and the DRDY is set. In the case of a connected PDC channel, DRDY rising triggers a data transfer request. In any case, either EOC and DRDY can trigger an interrupt.

Reading one of the ADC\_CDR registers clears the corresponding EOC bit. Reading ADC\_LCDR clears the DRDY bit and EOC bit corresponding to the last converted channel.

**Figure 39-4. EOCx and DRDY Flag Behavior**



If the ADC\_CDR is not read before further incoming data is converted, the corresponding Overrun Error (OVREx) flag is set in the Overrun Status Register (ADC\_OVER).

Likewise, new data converted when DRDY is high sets the GOVRE bit (General Overrun Error) in ADC\_SR.

The OVREx flag is automatically cleared when ADC\_OVER is read, and GOVRE flag is automatically cleared when ADC\_SR is read.

**Table 41-51. SMC Write NCS Controlled (WRITE\_MODE = 0)**

Symbol	Parameter	Min		Max		Unit
		1.8V Domain	3.3V Domain	1.8V Domain	3.3V Domain	
SMC <sub>22</sub>	Data Out Valid before NCS High	$\text{ncs wr pulse} \times t_{\text{CPMCK}} - 1$	$\text{ncs wr pulse} \times t_{\text{CPMCK}} - 1$			ns
SMC <sub>23</sub>	NCS Pulse Width	$\text{ncs wr pulse} \times t_{\text{CPMCK}} - 5$	$\text{ncs wr pulse} \times t_{\text{CPMCK}} - 5$			ns
SMC <sub>24</sub>	A0–A22 valid before NCS low	$\text{ncs wr setup} \times t_{\text{CPMCK}} - 2$	$\text{ncs wr setup} \times t_{\text{CPMCK}} - 1.5$			ns
SMC <sub>25</sub>	NWE low before NCS high	$(\text{ncs wr setup} - \text{nwe setup} + \text{ncs pulse}) \times t_{\text{CPMCK}} - 1$	$(\text{ncs wr setup} - \text{nwe setup} + \text{ncs pulse}) \times t_{\text{CPMCK}} - 1$			ns
SMC <sub>26</sub>	NCS High to Data Out, A0–A25, change	$\text{ncs wr hold} \times t_{\text{CPMCK}} - 6$	$\text{ncs wr hold} \times t_{\text{CPMCK}} - 5$			ns
SMC <sub>27</sub>	NCS High to NWE Inactive	$(\text{ncs wr hold} - \text{nwe hold}) \times t_{\text{CPMCK}} - 2$	$(\text{ncs wr hold} - \text{nwe hold}) \times t_{\text{CPMCK}} - 1.5$			ns

Notes: 1. hold length = total cycle duration - setup duration - pulse duration. “hold length” is for “ncs wr hold length” or “NWE hold length”.

**Figure 41-33. SMC Timings - NCS Controlled Read and Write**

