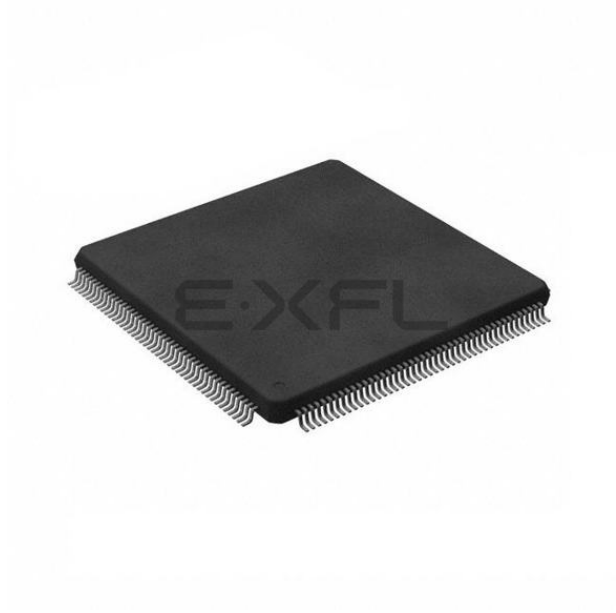

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What is "Embedded - Microcontrollers"?

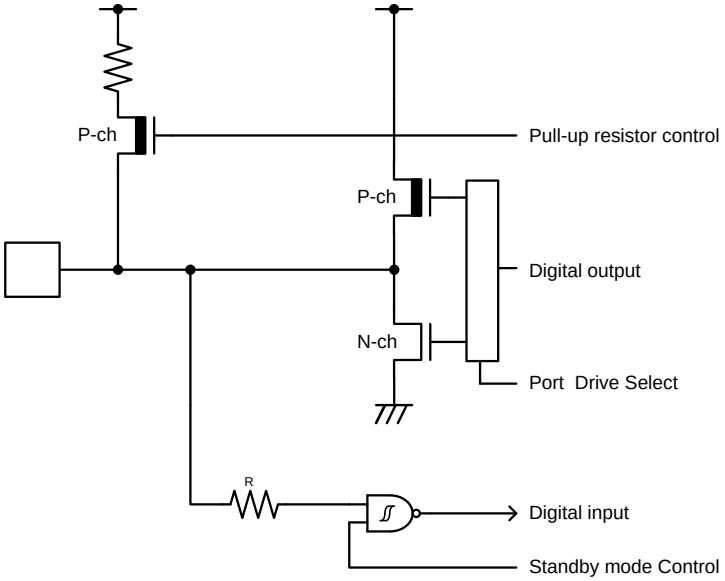
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c58j0agv2000a

Table of Contents

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
	INT20_1		89	74	-	M9
External Interrupt	INT21_0	External interrupt request 21 input pin	96	79	63	L10
	INT21_1		90	75	-	L9
	INT22_0	External interrupt request 22 input pin	99	82	66	N11
	INT22_1		78	63	-	K5
	INT23_0	External interrupt request 23 input pin	56	46	38	N2
	INT23_1		79	64	-	K6
	INT24_0	External interrupt request 24 input pin	147	121	97	F13
	INT24_1		131	107	87	H12
	INT25_0	External interrupt request 25 input pin	153	123	99	E11
	INT25_1		117	97	81	K14
	INT26_0	External interrupt request 26 input pin	156	126	102	D12
	INT26_1		142	116	92	G10
	INT27_0	External interrupt request 27 input pin	157	127	103	D13
	INT27_1		143	117	93	G9
	INT28_0	External interrupt request 28 input pin	190	158	128	A7
	INT28_1		207	167	-	E6
	INT29_0	External interrupt request 29 input pin	198	166	136	D6
	INT29_1		208	168	-	B5
	INT30_0	External interrupt request 30 input pin	209	169	137	C5
	INT30_1		195	163	133	F7
	INT31_0	External interrupt request 31 input pin	212	172	140	B3
	INT31_1		196	164	134	B6
	NMIX	Non-Maskable Interrupt input pin	158	128	104	C13

Type	Circuit	Remarks
S		・CMOS level output ・(It is possible to select by port drive capability. Select register [PDSR]) ・CMOS level hysteresis input ・Pull-up resistor control ・Standby mode control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -10 mA, I_{OL} = 10 mA (PDSR = 1) ・I_{OH} = -4 mA, I_{OL} = 4 mA (PDSR = 0) ・When this pin is used as an I^2C pin, the digital output P-ch transistor is always off.

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

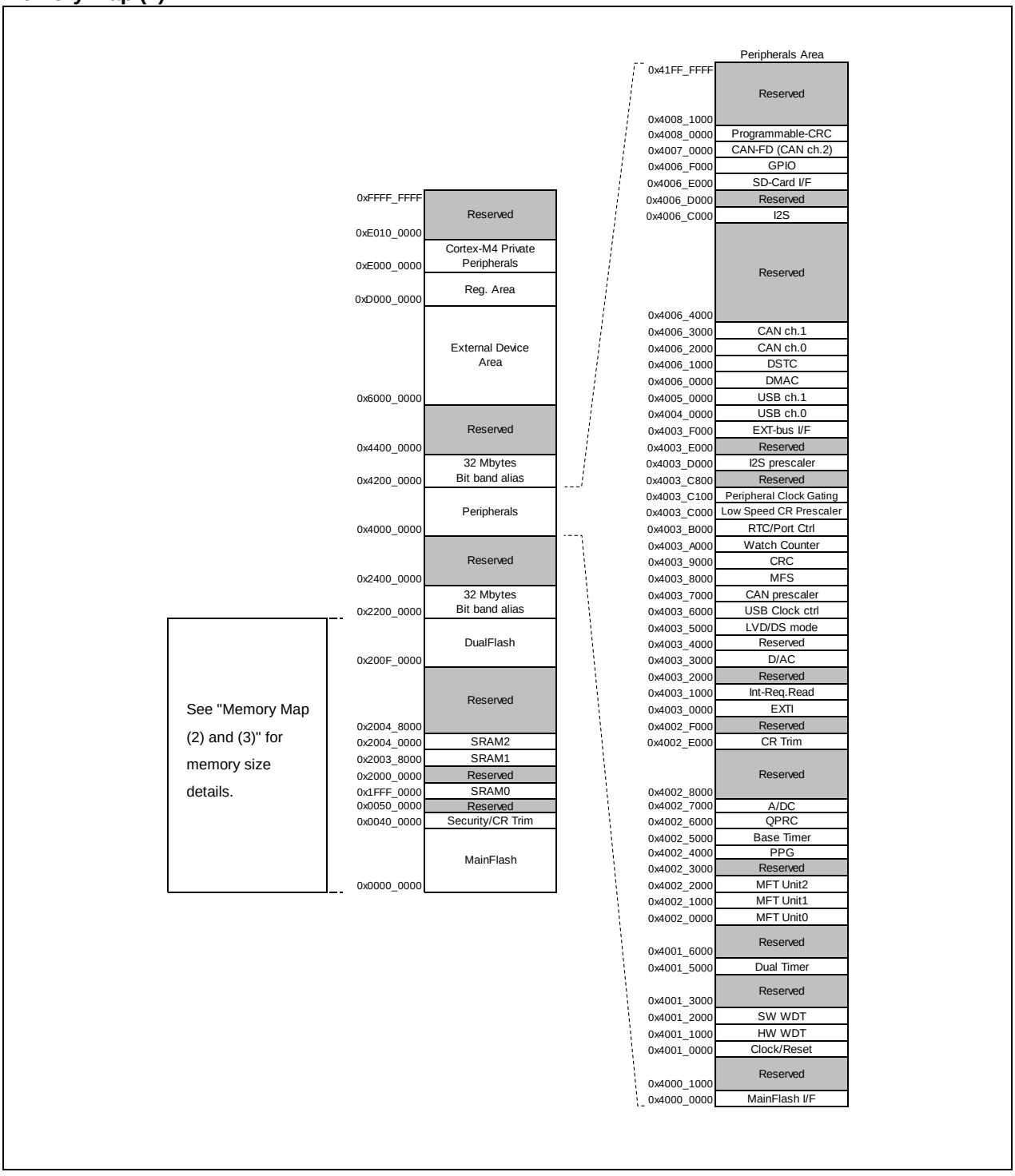
1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

9. Memory Size

See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

- INITX = 0

  This is the period when the INITX pin is at the L level.

- INITX = 1

  This is the period when the INITX pin is at the H level.

- SPL = 0

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

- SPL = 1

  This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

- Input enabled

  Indicates that the input function can be used.

- Internal input fixed at 0

  This is the status that the input function cannot be used. Internal input is fixed at L.

- Hi-Z

  Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

- Setting disabled

  Indicates that the setting is disabled.

- Maintain previous state

  Maintains the state that was immediately prior to entering the current mode.
  If a built-in peripheral function is operating, the output follows the peripheral function.
  If the pin is being used as a port, that output is maintained.

- Analog input is enabled

  Indicates that the analog input is enabled.

- Trace output

  Indicates that the trace function can be used.

- GPIO selected

  In Deep standby mode, pins switch to the general-purpose I/O port.

- Setting prohibition

  Prohibition of a setting by specification limitation

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return From Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
O	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected						Maintain previous state			
	Resource other than above selected						Hi-Z/internal input fixed at 0			
	GPIO selected									
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									

Current Explanation Diagram

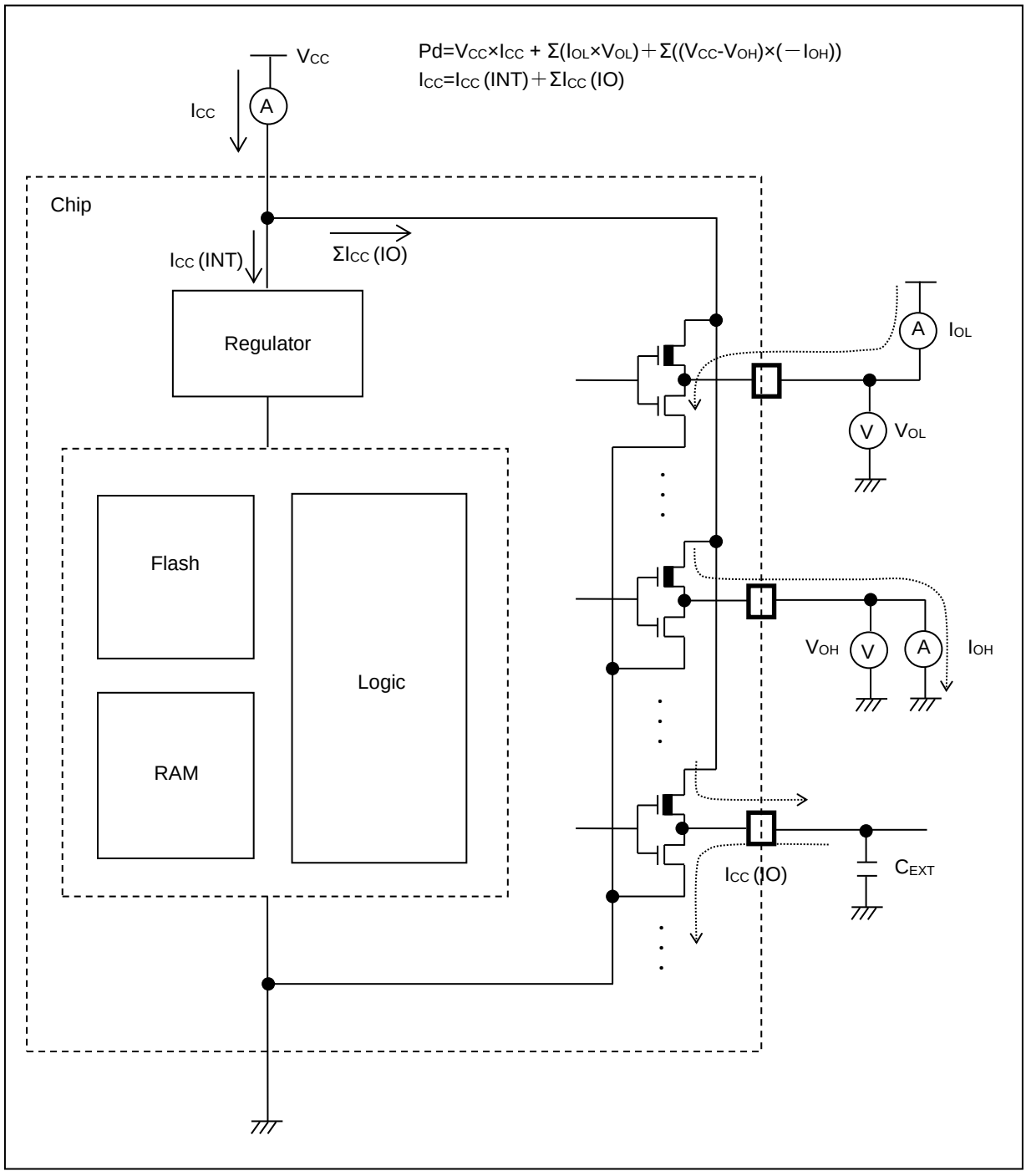


Table 12-10 Typical and Maximum Current Consumption in Low-voltage Detection Circuit, Main Flash Memory Write/erase

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Low-voltage detection circuit (LVD) power supply current	I_{CCLVD}	VCC	At operation	-	4	7	µA	For occurrence of interrupt
MainFlash memory write/erase current	$I_{CCFLASH}$		At write/erase	-	13.4	15.9	mA	*1

*1: When programming or erase in flash memory, Flash Memory Write/Erase current ($I_{CCFLASH}$) is added to the Power supply current (I_{CC}).

Peripheral Current Dissipation

Clock system	Peripheral	Unit	Frequency (MHz)			Unit	Remarks
			50	100	200		
HCLK	GPIO	All ports	0.39	0.81	1.56	mA	
	DMAC	-	0.99	1.97	3.82		
	DSTC	-	0.73	1.49	2.86		
	External bus I/F	-	0.25	0.48	0.97		
	SD card I/F	-	0.74	1.47	2.90		
	CAN	1 ch	0.06	0.08	0.16		
	CAN-FD	1 ch	0.77	1.50	2.95		
	USB	1 ch	0.48	0.95	1.89		
	I^2S	-	0.51	1.02	1.99		
	High-Speed Quad SPI	-	0.48	0.97	1.49		
	Programmable CRC	-	0.05	0.10	0.22		
PCLK1	Base timer	4 ch	0.21	0.42	0.83	mA	
	Multi-functional timer/PPG	1 unit/4 ch	0.83	1.65	3.25		
	Quadrature position/revolution counter	1 unit	0.07	0.13	0.27		
	A/D converter	1 unit	0.31	0.60	1.17		
PCLK2	Multi-function serial	1 ch	0.41	0.81	-	mA	

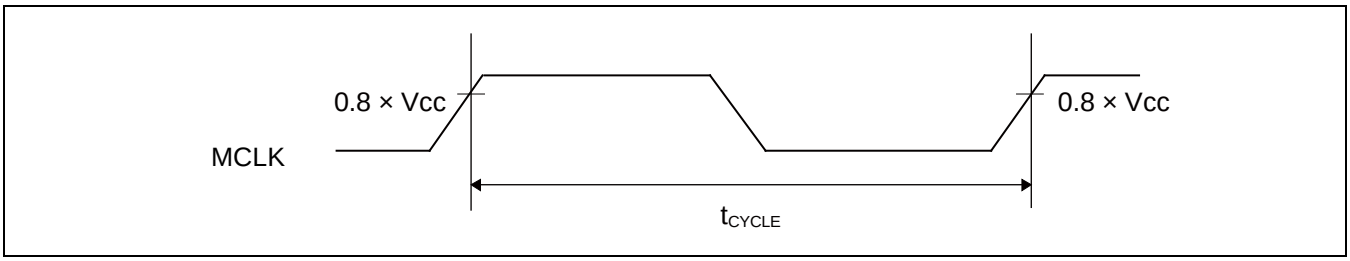
12.4.10 External Bus Timing

External Bus Clock Output Characteristics

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Output frequency	t_{CYCLE}	MCLKOUT *1		-	50 *2	MHz	

*1: The external bus clock (MCLKOUT) is a divided clock of HCLK.
For more information about setting of clock divider, see Chapter 14: External Bus Interface in FM4 Family Peripheral Manual Main Part (002-04856).

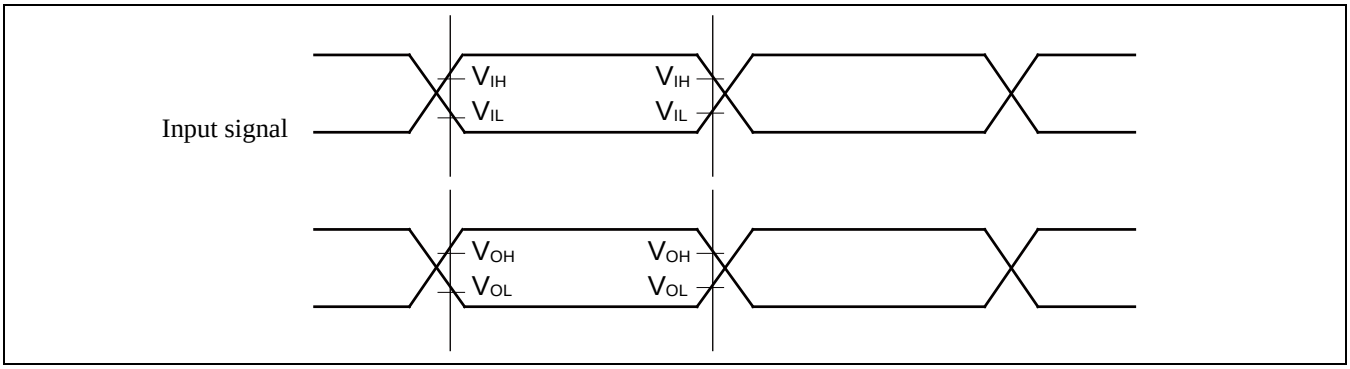
*2: Generate MCLKOUT at setting more than four divisions when the AHB bus clock exceeds 100 MHz.



External Bus Signal I/O characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value	Unit	Remarks
Signal input characteristics	V_{IH}	-	0.8 × V_{CC}	V	
	V_{IL}		0.2 × V_{CC}	V	
Signal output characteristics	V_{OH}		0.8 × V_{CC}	V	
	V_{OL}		0.2 × V_{CC}	V	



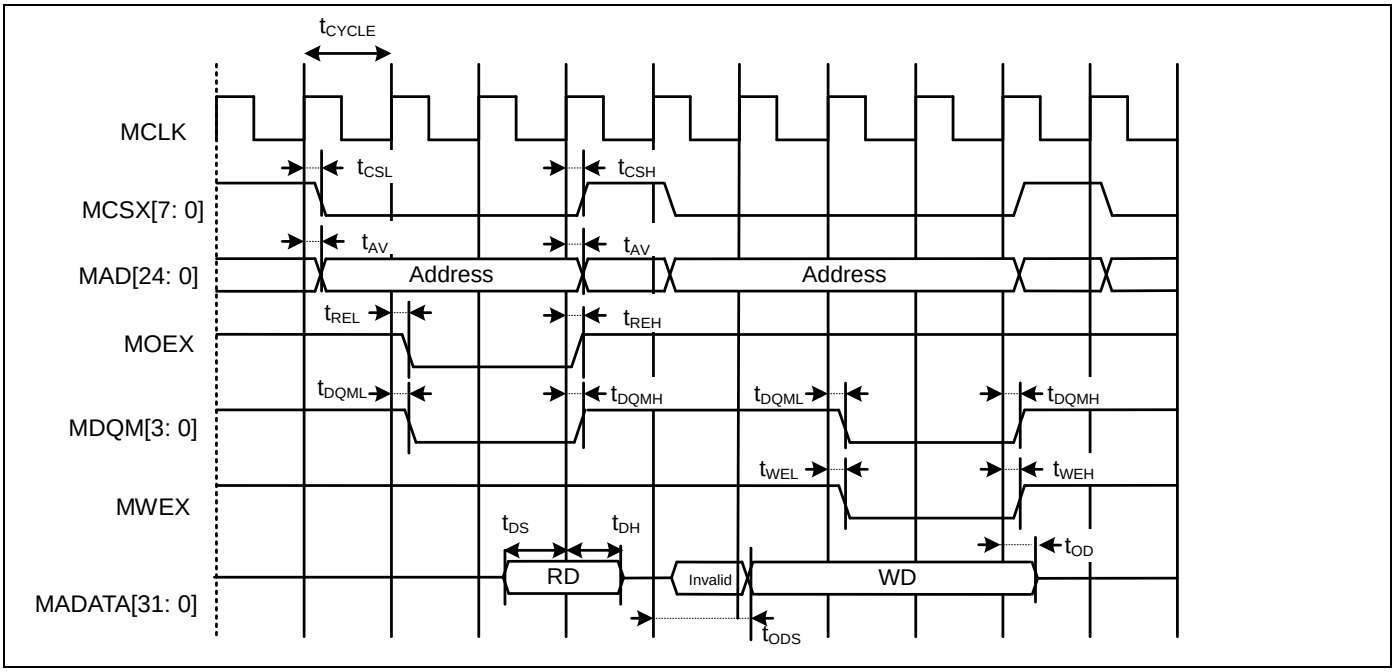
Separate Bus Access Synchronous SRAM Mode

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX[7: 0]	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up →MCLK ↑ time	t_{DS}	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1: 0] delay time	t_{DQML}	MCLK, MDQM[3: 0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[31: 0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[31: 0]	-	1	18	ns	

Note:

- *When the external load capacitance C_L = 30 pF*

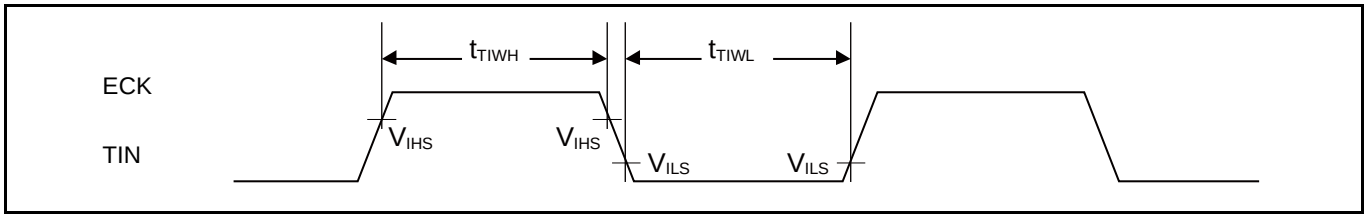


12.4.11 Base Timer Input Timing

Timer Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

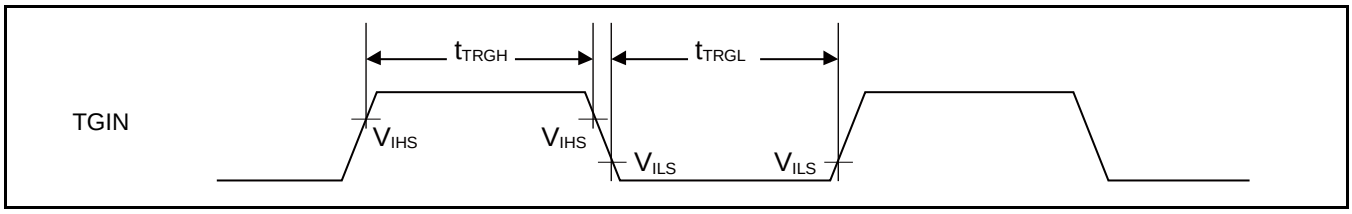
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIOAn/TIOBn (when using as ECK, TIN)	-	$2t_{CYCP}$	-	ns	



Trigger Input Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	TIOAn/TIOBn (when using as TGIN)	-	$2t_{CYCP}$	-	ns	



Note:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the base timer is connected, see 8. Block Diagram in this data sheet.*

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t_{CSDI}		(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	(*3)-50 +5t_{CYCP}	(*3)+50 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+30	-	3t_{CYCP}+30	-	ns
SCS ↓ →SOT delay time	t_{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)*

12.4.13 External Input Timing

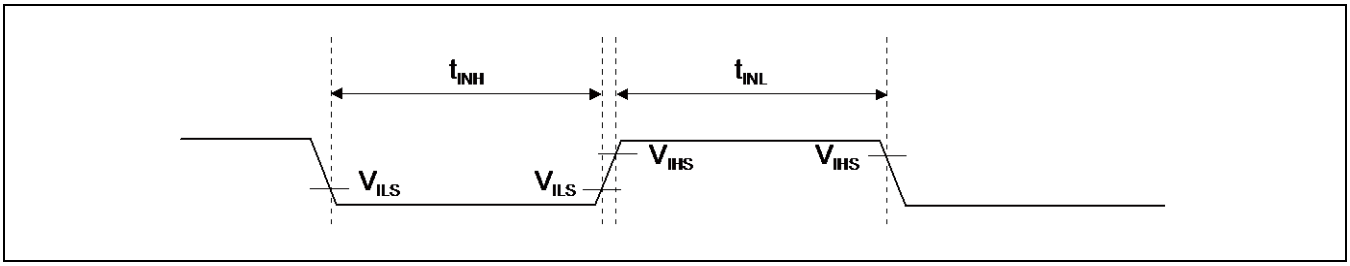
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{INH}, t_{INL}	ADTGx	-	$2t_{CYCP}$*1	-	ns	A/D converter trigger input
		FRCKx					Free-run timer input clock
		ICxx					Input capture
		DTTIxX	-	$2t_{CYCP}$*1	-	ns	Waveform generator
		INT00 to INT31, NMIX	-	$2t_{CYCP}$ + 100*1	-	ns	External interrupt, NMI
				500*2	-	ns	
		WKUPx	-	500*3	-	ns	Deep standby wake up

*1: t_{CYCP} indicates the APB bus clock cycle time except stop when in Stop mode, in Timer mode. For more information about the APB bus number to which the A/D converter, multi-function timer, and external interrupt are connected, see 8. Block Diagram in this data sheet.

*2: When in Stop mode, in Timer mode

*3: When in Deep Standby RTC mode, in Deep Standby Stop mode



12.4.19 I²S Timing

Master Mode Timing

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{MCYC}	I2SCK	-	-	12.288	MHz	
Output clock pulse width	t_{MHW}	I2SCK	-	45	55	%	
	t_{MLW}			45	55	%	
I2SCK→I2SWS delay time	t_{DFS}	I2SCK, I2SWS	-	0	24.0	ns	
I2SCK→I2SDO delay time*	t_{DDO}	I2SCK, I2SDO	-	0	24.0	ns	
I2SDI→I2SCK setup time	t_{HSDI}	I2SCK, I2SDI	-	25.0	-	ns	
I2SDI→I2SCK hold time	t_{HDI}		-	0	-	ns	
Input signal rise time	t_{FI}	I2SDI	-	-	5	ns	
Input signal fall time	t_{FI}		-	-	5	ns	

*: Except for the first bit of transmission frame

Notes:

- *When the external load capacitance C_L = 20 pF*
- *When I2SWS = 48 kHz, I2MCLK = 256 × I2SWS*
  Frame synchronization signal (I2SWS) is settable to 48 kHz, 32 kHz, 16 kHz.
  See Chapter7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details.

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH – 15	-	AVRH + 15	mV	
			AV_{CC} - 15	-	AV_{CC} + 15	mV	
Conversion time	-	-	0.5*1	-	-	µs	AV_{CC} ≥ 4.5 V
Sampling time *2	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-	1000		AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck ＜ 50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

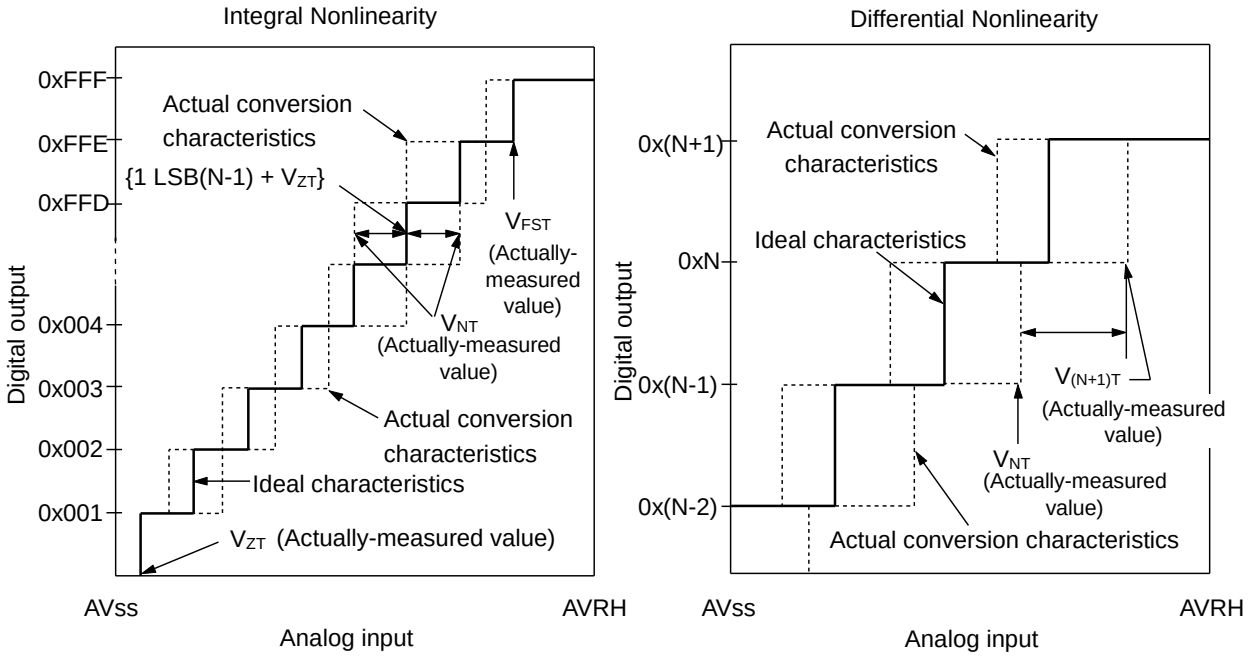
*1: The conversion time is the value of sampling time (T_S) + compare time (T_C).
The condition of the minimum conversion time is when the value of T_S = 150 ns and Tc = 350 ns (AV_{CC} ≥ 4.5V). Ensure that it satisfies the value of sampling time (T_S) and compare clock cycle (T_{CCK}). For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 8. Block Diagram in this data sheet.
The sampling and compare clock are set at base clock (HCLK).

*2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

*3: The compare time (T_C) is the value of (Equation 2).

Definition of 12-bit A/D Converter Terms

- **Resolution:** Analog variation that is recognized by an A/D converter.
- **Integral Nonlinearity:** Deviation of the line between the zero-transition point (0b000000000000 ⟷ 0b000000000001) and the full-scale transition point (0b111111111110 ⟷ 0b111111111111) from the actual conversion characteristics.
- **Differential Nonlinearity:** Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



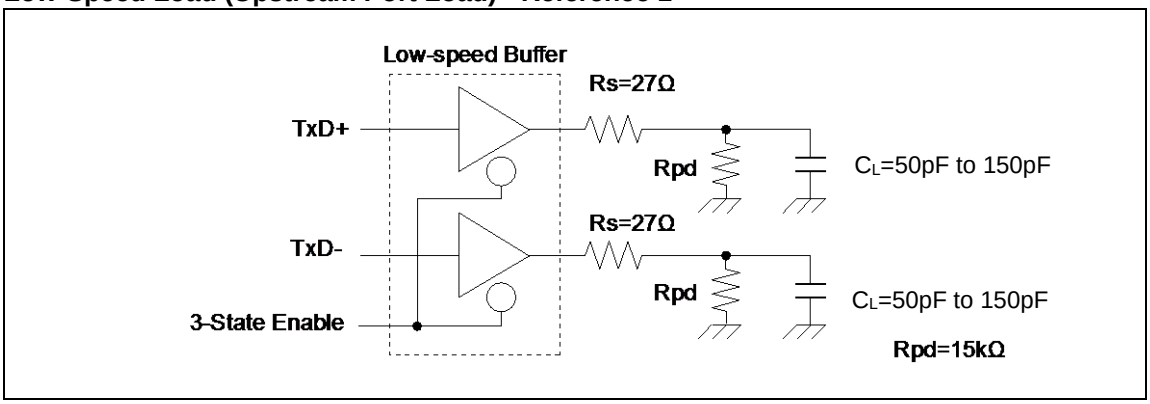
$$\text{Integral Nonlinearity of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{ZT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

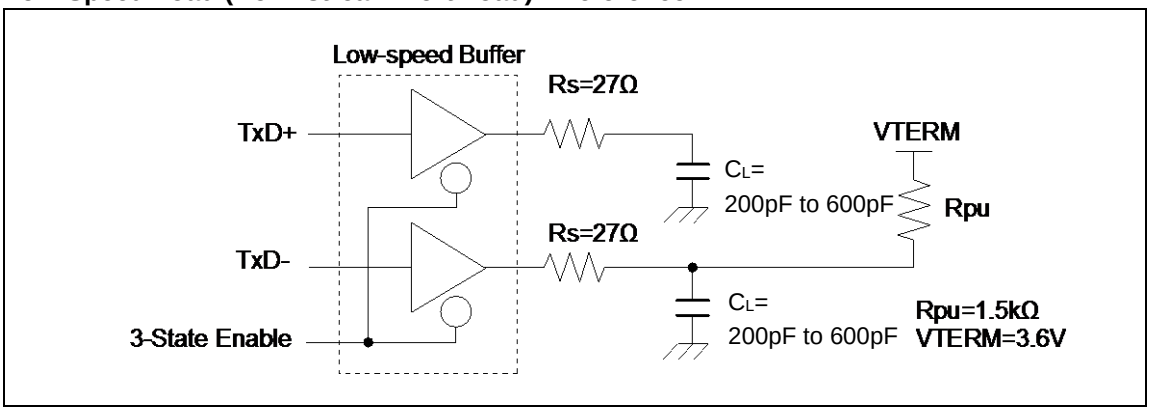
$$1LSB = \frac{V_{FST} - V_{ZT}}{4094}$$

N: A/D converter digital output value.
V_{ZT}: Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST}: Voltage at which the digital output changes from 0xFFE to 0xFFF.
V_{NT}: Voltage at which the digital output changes from 0x(N − 1) to 0xN.

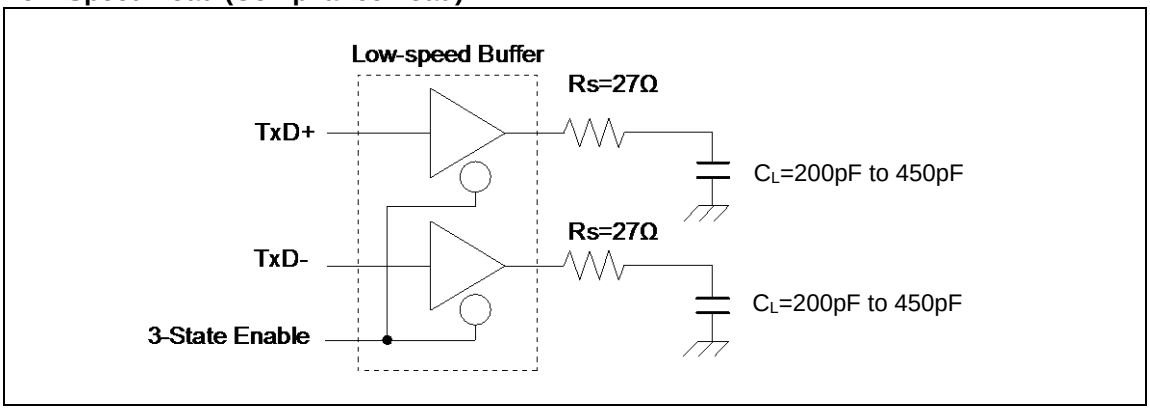
Low-Speed Load (Upstream Port Load) - Reference 1



Low-Speed Load (Downstream Port Load) - Reference 2



Low-Speed Load (Compliance Load)



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