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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

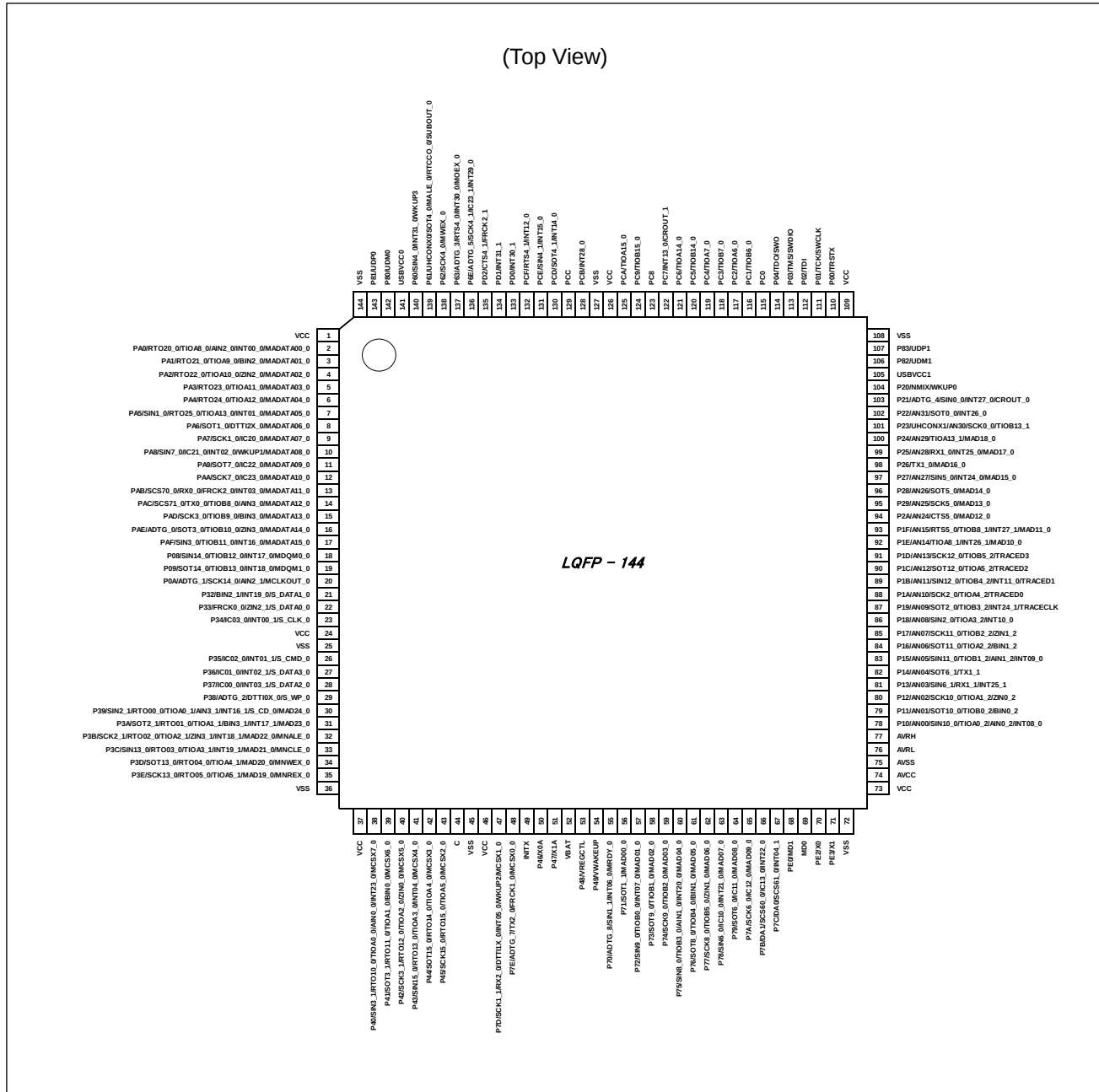
Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, I ² C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c59h0agv2000a

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3. Pin Assignments

LQS144



Note:

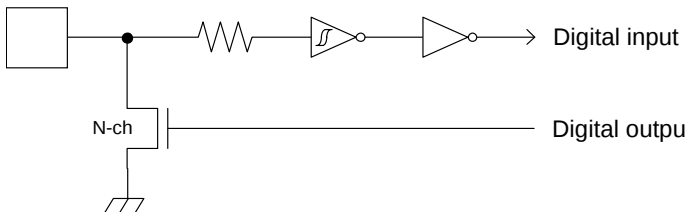
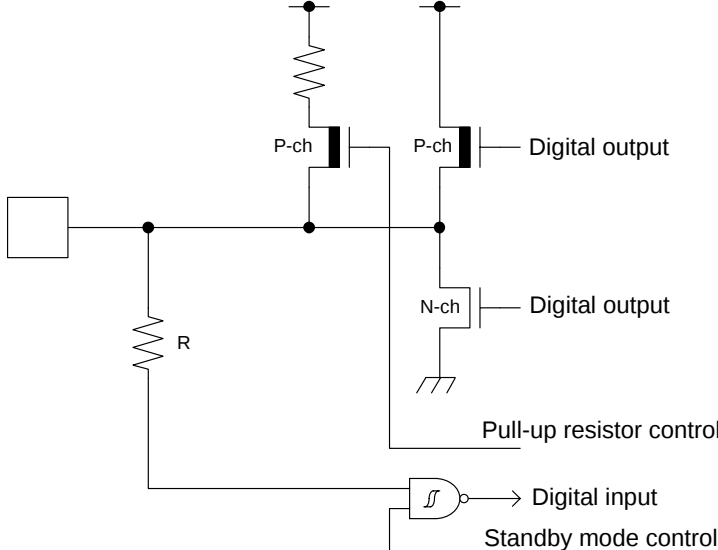
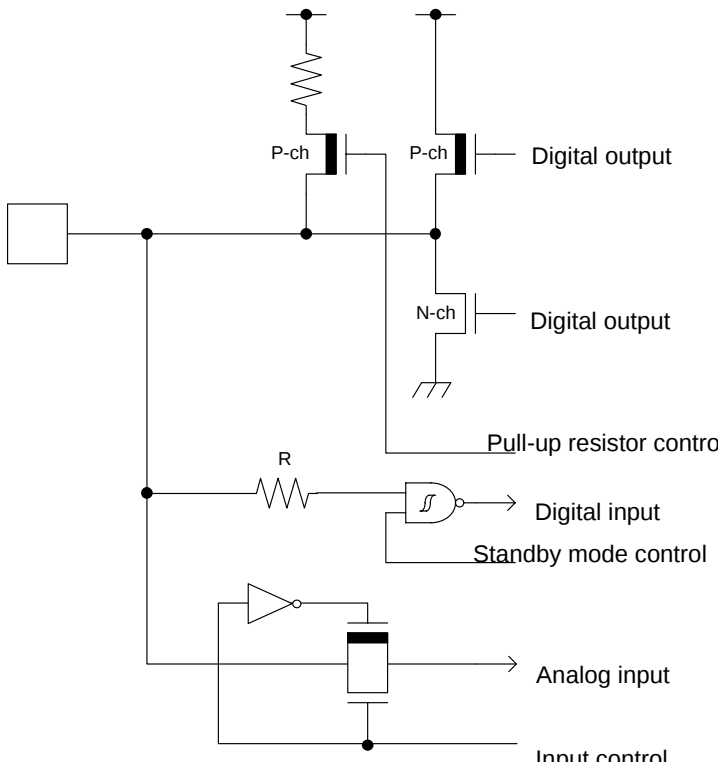
- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

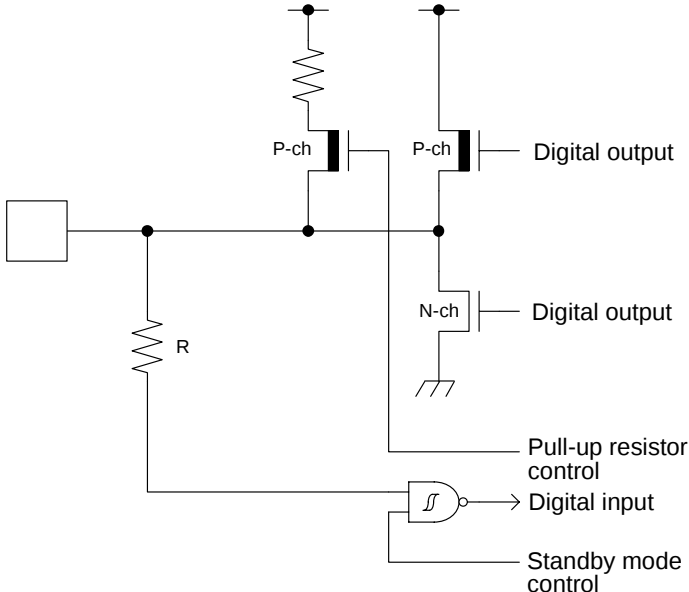
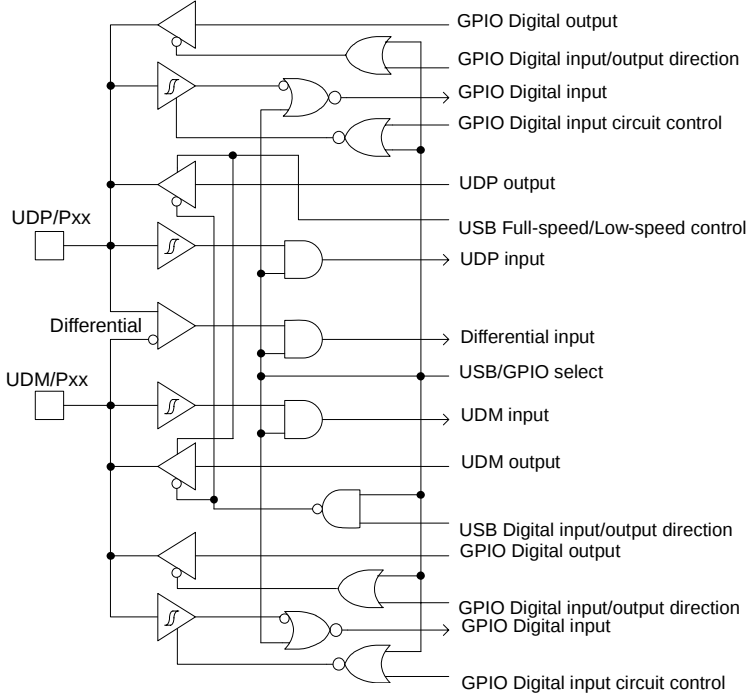
LQQ216

(Top View)

		125	VSS	126	VSS
		127	PRBSUDP1	128	VSS
		129	PRBSUDP2	129	VSS
		130	PRBSUDP3	130	VSS
		131	PRBSUDP4	131	VSS
		132	PRBSUDP5	132	VSS
		133	PRBSUDP6	133	VSS
		134	PRBSUDP7	134	VSS
		135	PRBSUDP8	135	VSS
		136	PRBSUDP9	136	VSS
		137	PRBSUDP10	137	VSS
		138	PRBSUDP11	138	VSS
		139	PRBSUDP12	139	VSS
		140	PRBSUDP13	140	VSS
		141	PRBSUDP14	141	VSS
		142	PRBSUDP15	142	VSS
		143	PRBSUDP16	143	VSS
		144	PRBSUDP17	144	VSS
		145	PRBSUDP18	145	VSS
		146	PRBSUDP19	146	VSS
		147	PRBSUDP20	147	VSS
		148	PRBSUDP21	148	VSS
		149	PRBSUDP22	149	VSS
		150	PRBSUDP23	150	VSS
		151	PRBSUDP24	151	VSS
		152	PRBSUDP25	152	VSS
		153	PRBSUDP26	153	VSS
		154	PRBSUDP27	154	VSS
		155	PRBSUDP28	155	VSS
		156	PRBSUDP29	156	VSS
		157	PRBSUDP30	157	VSS
		158	PRBSUDP31	158	VSS
		159	PRBSUDP32	159	VSS
		160	PRBSUDP33	160	VSS
		161	PRBSUDP34	161	VSS
		162	PRBSUDP35	162	VSS
		163	PRBSUDP36	163	VSS
		164	PRBSUDP37	164	VSS
		165	PRBSUDP38	165	VSS
		166	PRBSUDP39	166	VSS
		167	PRBSUDP40	167	VSS
		168	PRBSUDP41	168	VSS
		169	PRBSUDP42	169	VSS
		170	PRBSUDP43	170	VSS
		171	PRBSUDP44	171	VSS
		172	PRBSUDP45	172	VSS
		173	PRBSUDP46	173	VSS
		174	PRBSUDP47	174	VSS
		175	PRBSUDP48	175	VSS
		176	PRBSUDP49	176	VSS
		177	PRBSUDP50	177	VSS
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		179	PRBSUDP52	179	VSS
		180	PRBSUDP53	180	VSS
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		184	PRBSUDP57	184	VSS
		185	PRBSUDP58	185	VSS
		186	PRBSUDP59	186	VSS
		187	PRBSUDP60	187	VSS
		188	PRBSUDP61	188	VSS
		189	PRBSUDP62	189	VSS
		190	PRBSUDP63	190	VSS
		191	PRBSUDP64	191	VSS
		192	PRBSUDP65	192	VSS
		193	PRBSUDP66	193	VSS
		194	PRBSUDP67	194	VSS
		195	PRBSUDP68	195	VSS
		196	PRBSUDP69	196	VSS
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		198	PRBSUDP71	198	VSS
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		200	PRBSUDP73	200	VSS
		201	PRBSUDP74	201	VSS
		202	PRBSUDP75	202	VSS
		203	PRBSUDP76	203	VSS
		204	PRBSUDP77	204	VSS
		205	PRBSUDP78	205	VSS
		206	PRBSUDP79	206	VSS
		207	PRBSUDP80	207	VSS
		208	PRBSUDP81	208	VSS
		209	PRBSUDP82	209	VSS
		210	PRBSUDP83	210	VSS
		211	PRBSUDP84	211	VSS
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		219	PRBSUDP92	219	VSS
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		239	PRBSUDP112	239	VSS
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		272	PRBSUDP145	272	VSS
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		277	PRBSUDP150	277	VSS
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		289	PRBSUDP162	289	VSS
		290	PRBSUDP163	290	VSS
		291	PRBSUDP164	291	VSS
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		337	PRBSUDP210	337	VSS
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		353	PRBSUDP226	353	VSS
		354	PRBSUDP227	354	VSS
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		381	PRBSUDP254	381	VSS
		382	PRBSUDP255	382	VSS
		383	PRBSUDP256	383	VSS
		384	PRBSUDP257	384	VSS
		385	PRBSUDP258	385	VSS
		386	PRBSUDP259	386	VSS
		387	PRBSUDP260	387	VSS

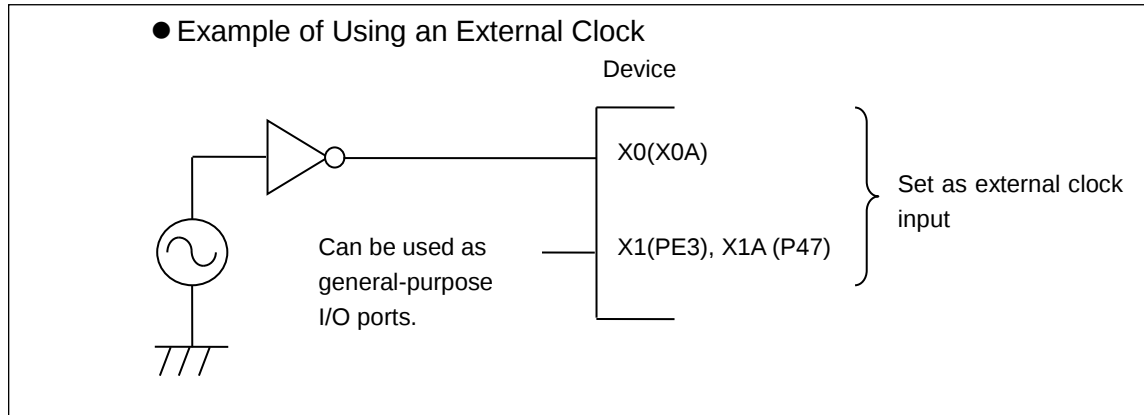
Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P30	General-purpose I/O port 3	34	24	-	G6
	P31		35	25	-	H4
	P32		36	26	21	H2
	P33		37	27	22	J1
	P34		38	28	23	H3
	P35		41	31	26	H6
	P36		42	32	27	J5
	P37		43	33	28	J4
	P38		44	34	29	J3
	P39		45	35	30	J2
	P3A		46	36	31	K1
	P3B		47	37	32	K2
	P3C		48	38	33	K3
	P3D		49	39	34	K4
	P3E		50	40	35	L1
	P40	General-purpose I/O port 4	56	46	38	N2
	P41		57	47	39	N3
	P42		58	48	40	M3
	P43		59	49	41	L4
	P44		60	50	42	M4
	P45		61	51	43	N4
	P46		73	58	50	P5
	P47		74	59	51	P6
	P48		76	61	53	N6
	P49		77	62	54	M6
	P4A		65	-	-	-
	P4B		66	-	-	-
	P4C		67	-	-	-
	P4D		68	-	-	-
	P4E		69	-	-	-

Type	Circuit	Remarks
C		• Open drain output • CMOS level hysteresis input
E		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off.
F		• CMOS level output • CMOS level hysteresis input • Input control • Analog input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off.

Type	Circuit	Remarks
G	 P-ch Digital output P-ch Digital output N-ch Digital output R Pull-up resistor control Digital input Standby mode control	• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -12 \text{ mA}$, $I_{OL} = 12 \text{ mA}$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off.
H	 GPIO Digital output GPIO Digital input/output direction GPIO Digital input GPIO Digital input circuit control UDP output USB Full-speed/Low-speed control UDP input Differential input USB/GPIO select UDM input UDM output USB Digital input/output direction GPIO Digital output GPIO Digital input/output direction GPIO Digital input GPIO Digital input circuit control	It is possible to select either USB I/O or GPIO function. When the USB I/O is selected: • Full-speed, low-speed control When the GPIO is selected: • CMOS level output • CMOS level hysteresis input • Standby mode control • $I_{OH} = -20.5 \text{ mA}$, $I_{OL} = 18.5 \text{ mA}$

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

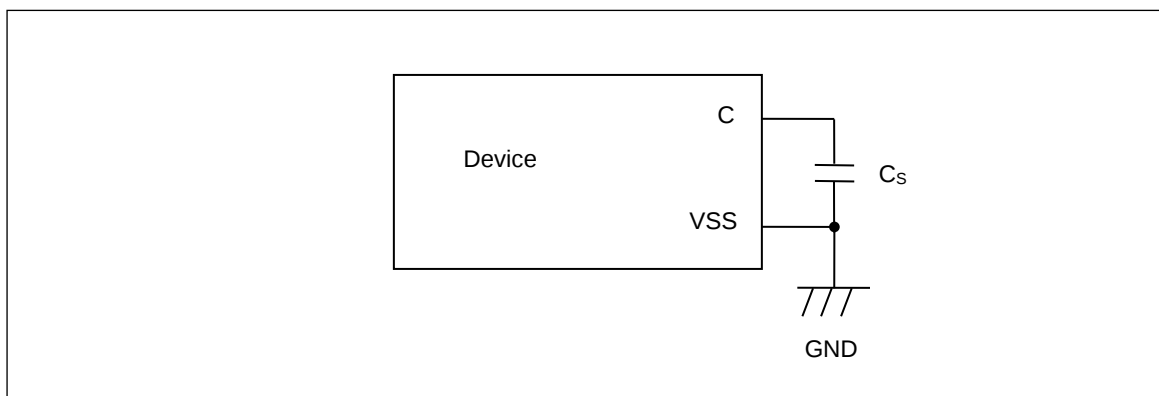


Handling When Using Multi-Function Serial Pin as I²C Pin

If the application uses the multi-function serial pin as an I²C pin, the P-channel transistor of the digital output must be disabled. I²C pins need to conform to electrical limitations like other pins, however, and avoid connecting to live external systems with the MCU power off.

C Pin

Devices in this series contain a regulator. Be sure to connect a smoothing capacitor (C_s) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. Some laminated ceramic capacitors have a large capacitance variation due to thermal fluctuation. Please select a capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of the device. A smoothing capacitor of about 4.7 μF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, the distance between the mode pins and VCC pins or VSS pins is as short as possible, and the connection impedance is low when the pins are pulled up/down such as for switching the pin level and rewriting the flash memory data. This is important to prevent the device from erroneously switching to test mode as a result of noise.

*8: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$P_d = V_{CC} \times I_{CC} + \sum (I_{OL} \times V_{OL}) + \sum ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I_{OL} : L level output current

I_{OH} : H level output current

V_{OL} : L level output voltage

V_{OH} : H level output voltage

I_{CC} is the current drawn by the device.

It can be analyzed as follows.

$$I_{CC} = I_{CC}(\text{INT}) + \sum I_{CC}(\text{IO})$$

$I_{CC}(\text{INT})$: Current drawn by internal logic and memory, etc. through the regulator

$\sum I_{CC}(\text{IO})$: Sum of current (I/O switching current) drawn by the output pin

For $I_{CC}(\text{INT})$, it can be anticipated by (1) Current Rating in 12.3. DC Characteristics (This rating value does not include $I_{CC}(\text{IO})$ for a value at pin fixed).

For $I_{CC}(\text{IO})$, it depends on system used by customers.

The calculation formula is shown below.

$$I_{CC}(\text{IO}) = (C_{\text{INT}} + C_{\text{EXT}}) \times V_{CC} \times f_{\text{SW}}$$

C_{INT} : Pin internal load capacitance
 C_{EXT} : External load capacitance of output pin
 f_{SW} : Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate $I_{CC}(\text{Max})$ as follows when the power dissipation can be evaluated by yourself:

Measure current value $I_{CC}(\text{Typ})$ at normal temperature (+25°C).

Add maximum leakage current value $I_{CC}(\text{leak_max})$ at operating on a value in (1).

$$I_{CC}(\text{Max}) = I_{CC}(\text{Typ}) + I_{CC}(\text{leak_max})$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	$I_{CC}(\text{leak_max})$	$T_J = +125^\circ\text{C}$	79.2 mA
		$T_J = +105^\circ\text{C}$	39.4 mA
		$T_J = +85^\circ\text{C}$	26.5 mA

Table 12-5 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency* ⁴	Value		Unit	Remarks
					Typ* ¹	Max* ²		
Power supply current	I _{CCS}	V _{CC}	Sleep operation* ⁵ (PLL)	200 MHz	88	188	mA	* ³ When all peripheral clocks are on
				192 MHz	85	184	mA	
				180 MHz	80	178	mA	
				160 MHz	72	164	mA	
				144 MHz	65	156	mA	
				120 MHz	55	144	mA	
				100 MHz	47	134	mA	
				80 MHz	38	124	mA	
				60 MHz	30	114	mA	
				40 MHz	21	104	mA	
				20 MHz	12	93	mA	
				8 MHz	7.4	87.2	mA	
				4 MHz	5.8	85.2	mA	* ³ When all peripheral clocks are off
				200 MHz	44	134	mA	
				192 MHz	42	132	mA	
				180 MHz	40	129	mA	
				160 MHz	36	123	mA	
				144 MHz	33	119	mA	
				120 MHz	28	113	mA	
				100 MHz	24	108	mA	
				80 MHz	20	103	mA	
				60 MHz	16	98	mA	
				40 MHz	12	93	mA	
				20 MHz	7.6	87.6	mA	
				8 MHz	5.2	84.7	mA	
				4 MHz	4.4	83.7	mA	

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V _{OL}	4 mA type	V _{CC} ≥ 4.5 V, I _{OL} = 4 mA	V _{SS}	-	0.4	V	
			V _{CC} < 4.5 V, I _{OL} = 2 mA					
		8 mA type	V _{CC} ≥ 4.5 V, I _{OL} = 8 mA	V _{SS}	-	0.4	V	
			V _{CC} < 4.5 V, I _{OL} = 4 mA					
		10 mA type	V _{CC} ≥ 4.5 V, I _{OL} = 10 mA	V _{SS}	-	0.4	V	
			V _{CC} < 4.5 V, I _{OL} = 8 mA					
		12 mA type	V _{CC} ≥ 4.5 V, I _{OL} = 12 mA	V _{SS}	-	0.4	V	
			V _{CC} < 4.5 V, I _{OL} = 8 mA					
		The pin doubled as USB I/O	USBV _{CC} ≥ 4.5 V, I _{OL} = 18.5 mA	V _{SS}	-	0.4	V	*1
			USBV _{CC} < 4.5 V, I _{OL} = 10.5 mA					
		The pin doubled as I ² C Fm+	V _{CC} ≥ 4.5 V, I _{OL} = 4 mA	V _{SS}	-	0.4	V	At GPIO
			V _{CC} < 4.5 V, I _{OL} = 3 mA					At I ² C Fm+
			V _{CC} ≤ 4.5 V, I _{OL} = 20 mA					
Input leak current	I _{IL}	-	-	- 5	-	+ 5	μA	
Pull-up resistor value	R _{PU}	Pull-up pin	V _{CC} ≥ 4.5 V	25	50	100	kΩ	
			V _{CC} < 4.5 V	30	80	200		
Input capacitance	C _{IN}	Other than VCC, USBVCC0, USBVCC1, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

*1: USBV_{CC}0 and USBV_{CC}1 are described as USBV_{CC}.

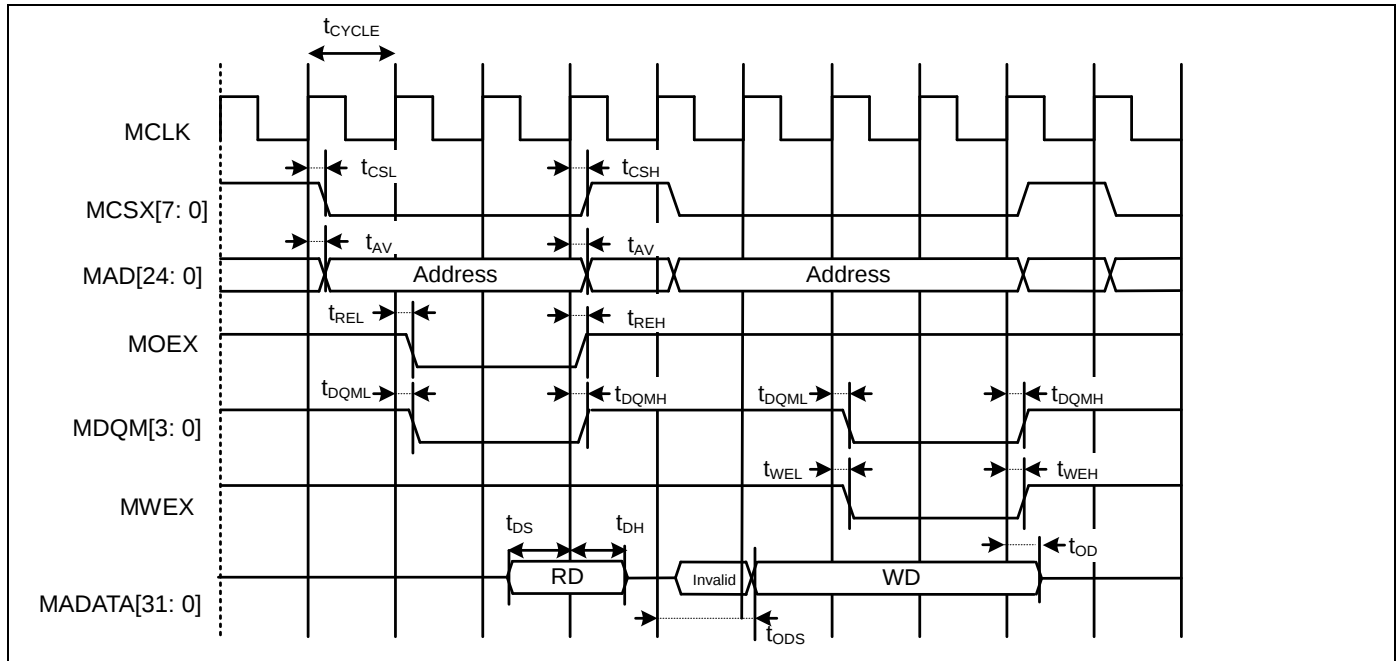
Separate Bus Access Synchronous SRAM Mode

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX[7: 0]	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up → MCLK ↑ time	t_{DS}	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1: 0] delay time	t_{DQML}	MCLK, MDQM[3: 0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[31: 0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[31: 0]	-	1	18	ns	

Note:

- When the external load capacitance $C_L = 30$ pF



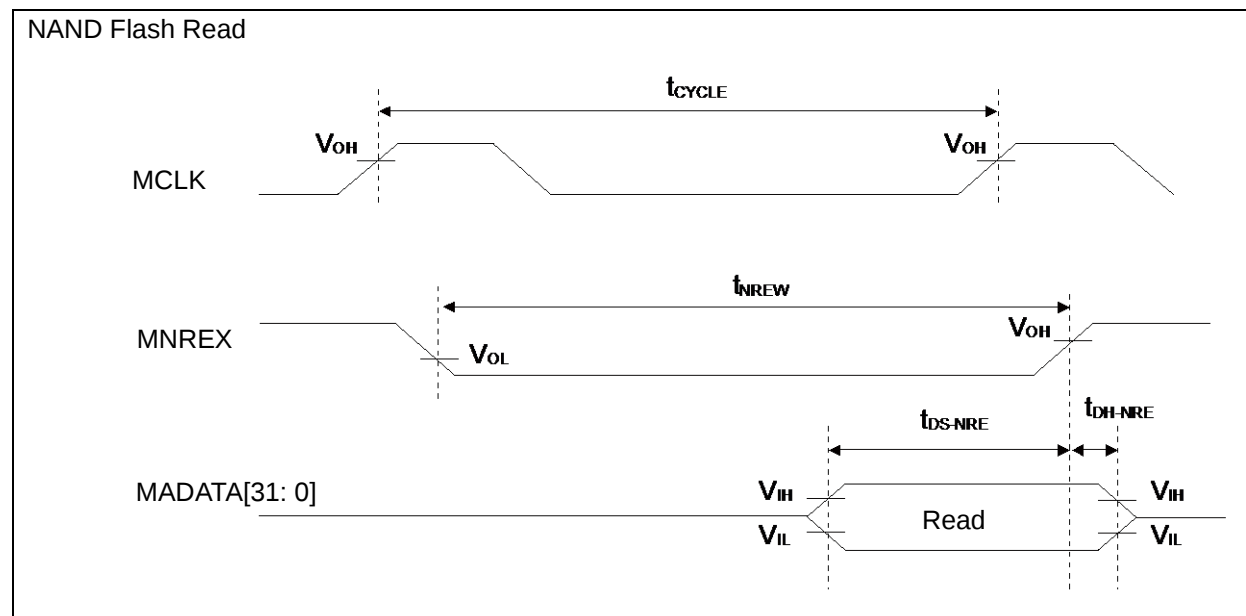
NAND Flash Mode

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MNREX Min pulse width	t_{NREW}	MNREX	-	$MCLK \times n - 3$	-	ns	
Data set up → MNREX ↑ time	$t_{DS - NRE}$	MNREX, MADATA[31: 0]	-	20	-	ns	
MNREX ↑ → Data hold time	$t_{DH - NRE}$	MNREX, MADATA[31: 0]	-	0	-	ns	
MNALE ↑ → MNWEX delay time	$t_{ALEH - NWEL}$	MNALE, MNWEX	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MNALE ↓ → MNWEX delay time	$t_{ALEL - NWEL}$	MNALE, MNWEX	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MNCLE ↑ → MNWEX delay time	$t_{CLEH - NWEL}$	MNCLE, MNWEX	-	$MCLK \times m - 9$	$MCLK \times m + 9$	ns	
MNWEX ↑ → MNCLE delay time	$t_{NWEH - CLEL}$	MNCLE, MNWEX	-	0	$MCLK \times m + 9$	ns	
MNWEX Min pulse width	t_{NWEW}	MNWEX	-	$MCLK \times n - 3$	-	ns	
MNWEX ↓ → Data output time	$t_{NWEL - DV}$	MNWEX, MADATA[31: 0]	-	-9	9	ns	
MNWEX ↑ → Data hold time	$t_{NWEH - DX}$	MNWEX, MADATA[31: 0]	-	0	$MCLK \times m + 9$	ns	

Note:

- When the external load capacitance $C_L = 30$ pF ($m = 0$ to 15 , $n = 1$ to 16)



When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t _{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t _{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t _{CSDI}		(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	ns
SCS↓→SCK↓ setup time	t _{CSSE}	External shift clock operation	3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCK↑→SCS↑ hold time	t _{CSHE}		0	-	0	-	ns
SCS deselect time	t _{CSDE}		3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCS ↓ →SOT delay time	t _{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t _{DSE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C_L = 30 pF.

High-Speed Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↑→SOT delay time	t _{SHOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↓ setup time	t _{IVSLI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↓→SIN hold time	t _{SLIXI}	SCKx, SINx	External shift clock operation	5	-	5	-	ns
Serial clock L pulse width	t _{SLSH}	SCKx		2t _{CYCP} - 5	-	2t _{CYCP} - 5	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx		t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↑→SOT delay time	t _{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t _{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t _{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
 No chip select: SIN4_0, SOT4_0, SCK4_0
 Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)

12.8 Low-Voltage Detection Characteristics

12.8.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

12.8.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	t _{LVDW}	-	-	-	6000×t _{CYCP} *	μs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.11 Standby Recovery Time

12.11.1 Recovery cause: Interrupt/WKUP

The time from the interrupt occurring to the time of program operation start is shown.

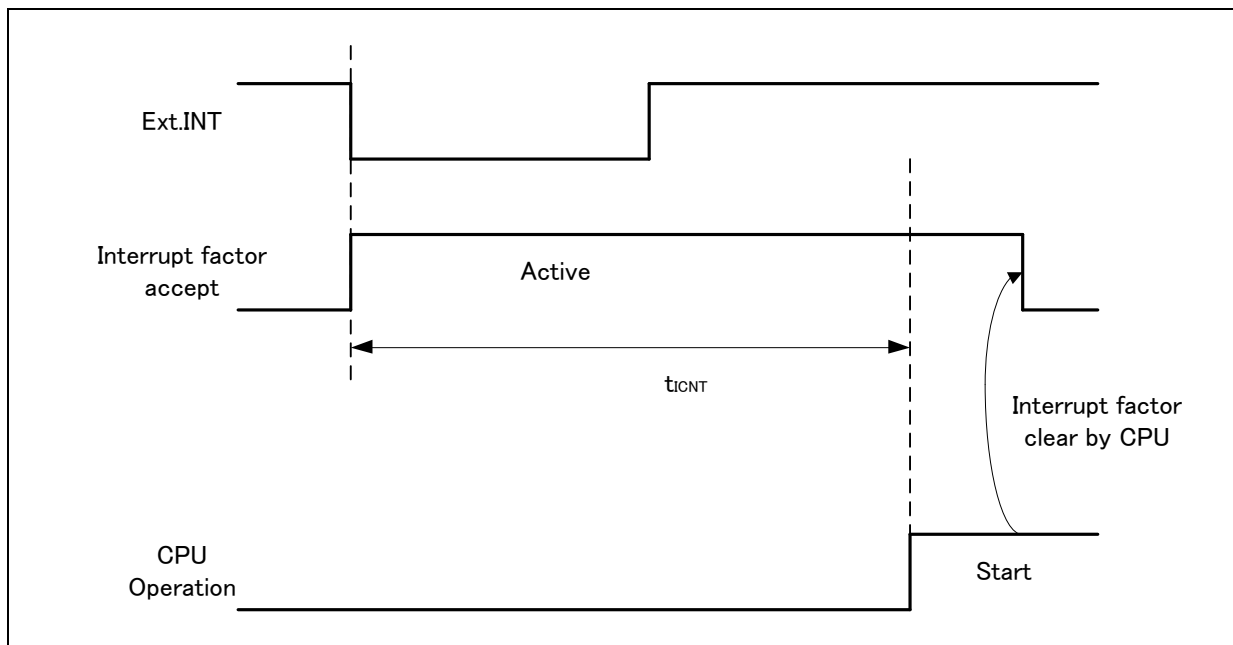
Recovery Count Time

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t _{ICNT}	HCLK×1		μs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	μs	
Low-speed CR Timer mode		450	900	μs	
Sub Timer mode		896	1136	μs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		316	581	μs	
RTC mode Stop mode (Low-speed CR/sub Run mode return)		270	540	μs	
Deep Standby RTC mode with RAM retention		365	667	μs	without RAM retention
Deep Standby Stop mode with RAM retention		365	667	μs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

12.11.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

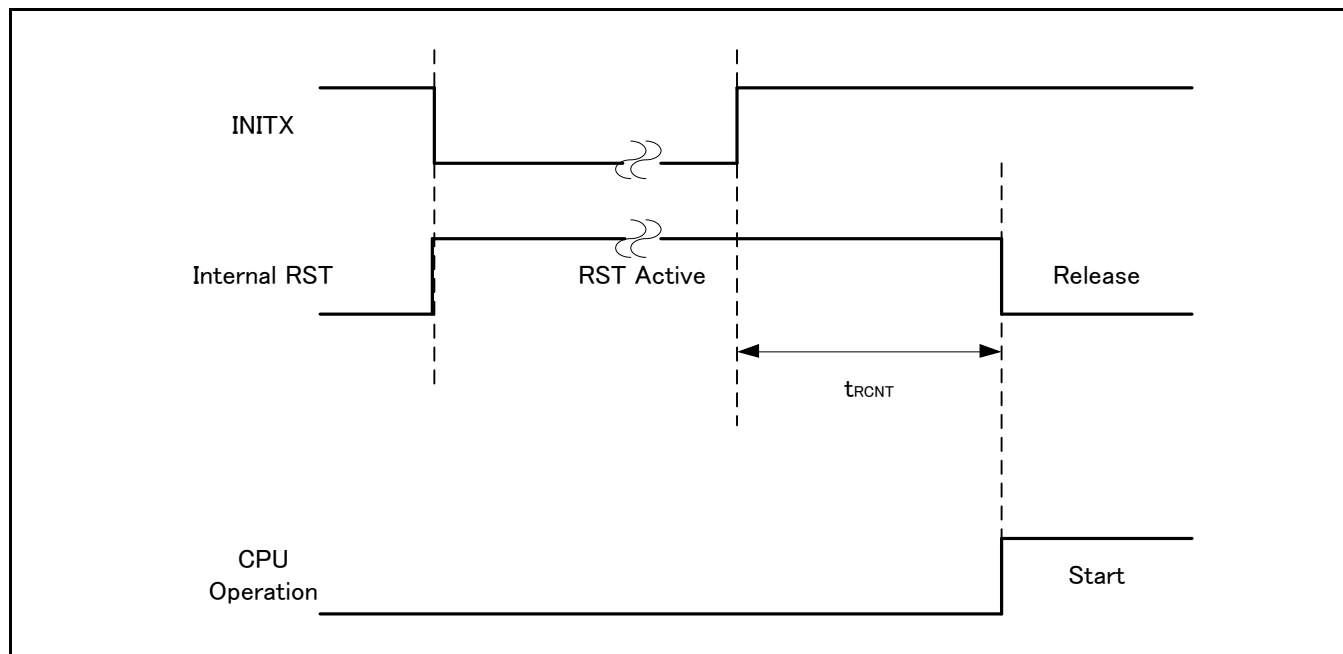
Recovery Count Time

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

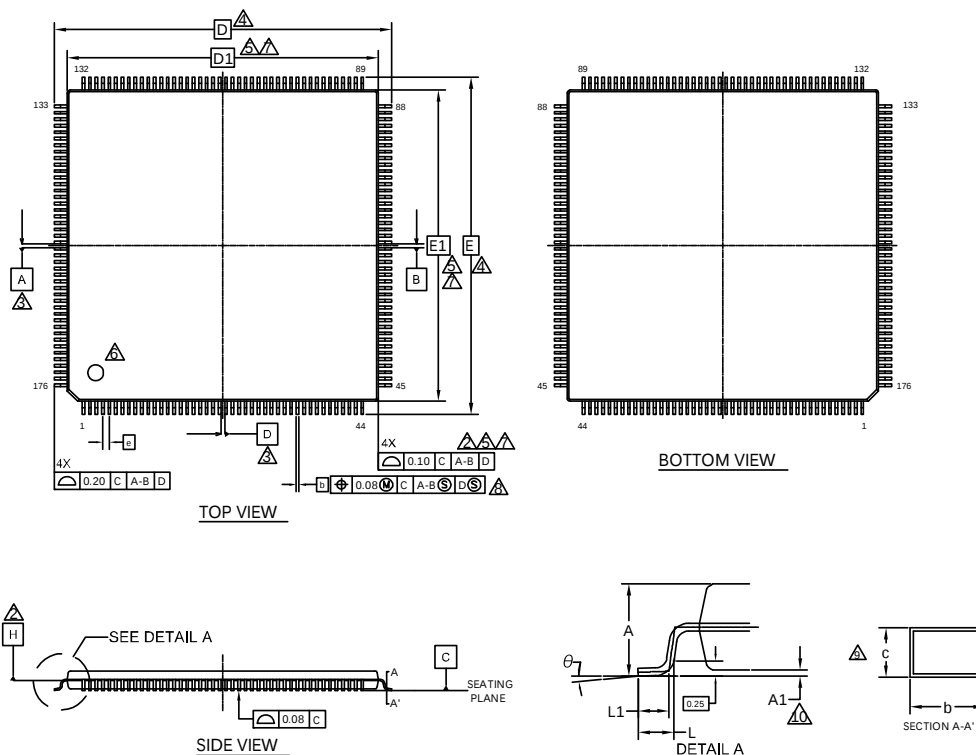
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	μs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	μs	
Low-speed CR Timer mode		315	567	μs	
Sub Timer mode		315	567	μs	
RTC mode Stop mode		315	567	μs	
Deep Standby RTC mode with RAM retention Deep Standby Stop mode with RAM retention		336	667	μs	without RAM retention
		336	667	μs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



Package Type	Package Code
LQFP 176	LQP 176



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC		
D1	24.00 BSC		
e	0.50 BSC		
E	26.00 BSC		
E1	24.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15150 **

PACKAGE OUTLINE, 176 LEAD LQFP
24.0X24.0X1.7 MM LQP176 REV**

Document History

Document Title: S6E2C5 Series 32-bit ARM® Cortex®-M4F, FM4 Microcontroller

Document Number: 002-04984

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	AKIH	04/22/2015	New Spec.
*A	5126421	HITK	02/08/2016	Company name and layout design change. Added the note of TAP pin. Updated Package Code and Dimensions (LQFP-144, LQFP-176, LQFP-216).
*B	5634625	YSKA	02/20/2017	Updated 12.4.8 Power-On Reset Timing. Changed parameter from "Power Supply rise time(t_{VCCR})[ms]" to "Power ramp rate(dV/dt)[mV/us]" and add some comments. (Page 117) Modified CSIO timing typo (12.4.12 CSIO(SPI) Timing) Deleted "SPI=1, MS=0" in the titles and added MS=0,1 in the schematic (Page 138-145 , 154-161) Modified RTC description(Features, Real-Time Clock (RTC)) Deleted "second , or day of the week" in the Interrupt function.(Page.3) Modifications related to the VBAT in the following chapter. "7. Handling Devices" Notes on Power-on (Page. 78) "11. Pin Status in Each CPU State" List of VBAT Domain Pin Status (Page. 94) "12.3.1 Current Rating" Table12-9. Typical and Maximum Current Consumption in Deep Standby STOP Mode, Deep Standby RTC Mode and VBAT (Page. 109) Change the name from "USB Function" to "USB Device" (Page 1 , 8 , 60) Updated "14. Package dimensions "(Page 195-198)" Deleted MPNs below from "13. Ordering Information" (Page 194) S6E2C58H0AGV20000, S6E2C59H0AGV20000, S6E2C5AH0AGV20000, S6E2C58J0AGV20000, S6E2C59J0AGV20000, S6E2C5AJ0AGV20000, S6E2C58J0AGB10000, S6E2C59J0AGB10000, S6E2C5AJ0AGB10000, S6E2C58L0AGL20000, S6E2C59L0AGL20000, S6E2C5AL0AGL20000 Added MPNs below to "13. Ordering Information" (Page 194) S6E2C58H0AGV2000A, S6E2C59H0AGV2000A, S6E2C5AH0AGV2000A, S6E2C58J0AGV2000A, S6E2C59J0AGV2000A, S6E2C5AJ0AGV2000A, S6E2C58J0AGB1000A, S6E2C59J0AGB1000A, S6E2C5AJ0AGB1000A, S6E2C58L0AGL2000A, S6E2C59L0AGL2000A, S6E2C5AL0AGL2000A Deleted Baud rate spec for High-Speed Synchronous Serial in "12.4.12 CSIO(SPI) Timing"(Page 146-152) Modified the expression of the "Built-in CR" and add Note in the "1. Product Lineup"(Page 9) Modified typo(SCLKx_0 -> SCKx_0)(Page 130 , 132 , 134 , 136) Added Maximum Access size in "Features"(Page 1) Updated IO circuit (type A) (Page 64)