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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, I ² C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	192-LFBGA
Supplier Device Package	192-FBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c59j0agb1000a

Low-power Consumption Mode

Six low power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

Peripheral Clock Gating

The system can reduce the current consumption of the total system with gating the operation clocks of peripheral functions not used.

VBAT

The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32-kHz oscillation circuit
- Power-on circuit
- Back up register: 32 bytes
- Port circuit

Debug

- Serial wire JTAG debug port (SWJ-DP)
- Embedded trace macrocells (ETM) provide comprehensive debug and trace facilities.
- AHB trace macrocells (HTM)

Unique ID

Unique value of the device (41-bit) is set.

Power Supply

- Four power supplies
 - Wide range voltage:
VCC = 2.7 V to 5.5 V
 - Power supply for USB ch 0 I/O:
USBVCC0 = 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
 - Power supply for USB ch 1 I/O:
USBVCC1 = 3.0 V to 3.6 V (when USB is used)
= 2.7 V to 5.5 V (when GPIO is used)
 - Power supply for VBAT:
VBAT = 1.65 V to 5.5 V

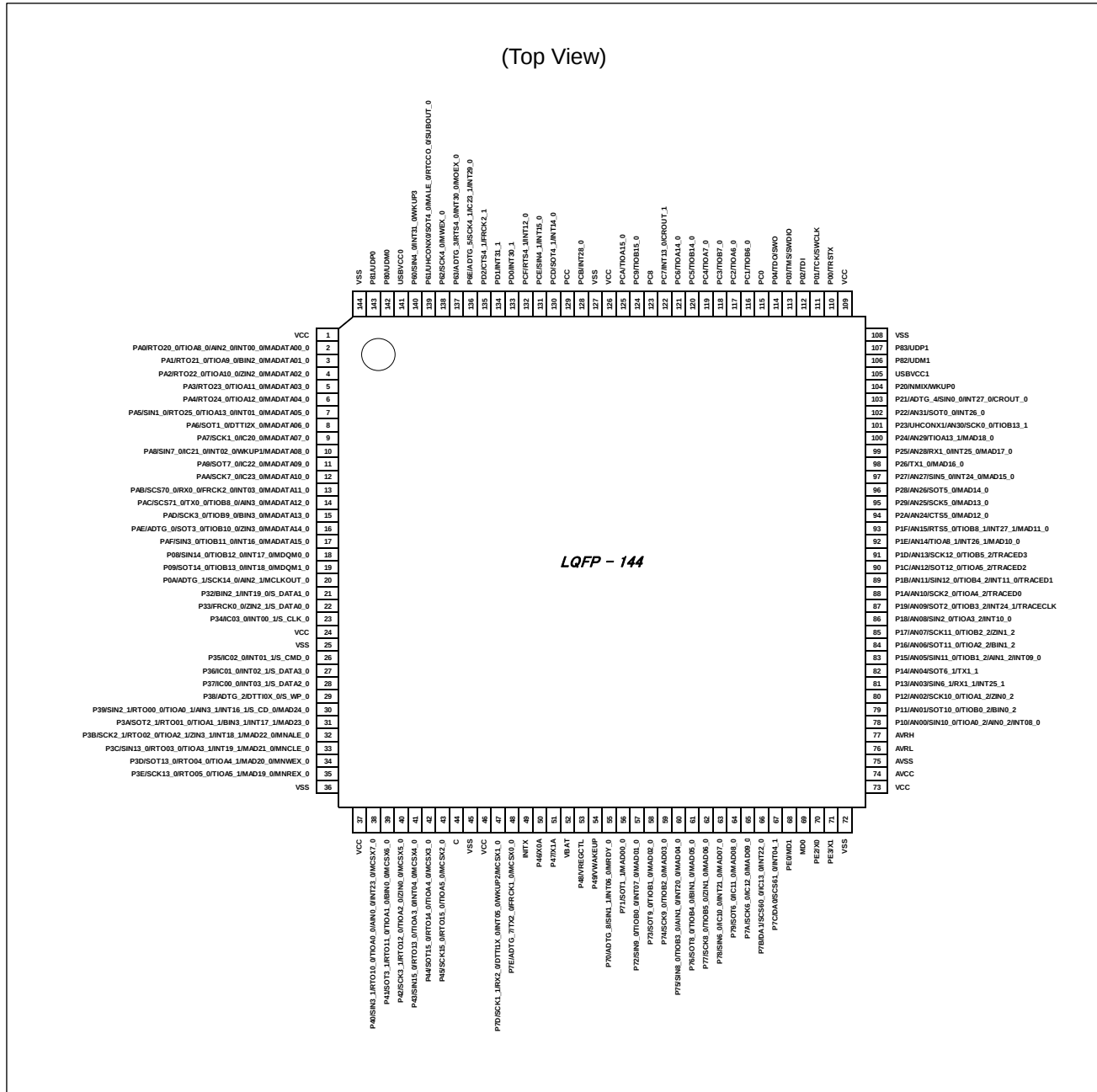
Product Name		S6E2C58H0A S6E2C59H0A S6E2C5AH0A	S6E2C58J0A S6E2C59J0A S6E2C5AJ0A	S6E2C58L0A S6E2C59L0A S6E2C5AL0A
Built-in CR	High-speed	4 MHz		
	Low-speed	100 kHz		
Debug function		SWJ-DP/ETM/HTM		
Unique ID		Yes		

Notes:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.
- See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.

3. Pin Assignments

LQS144



Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

4. Pin Descriptions

List of Pin Functions

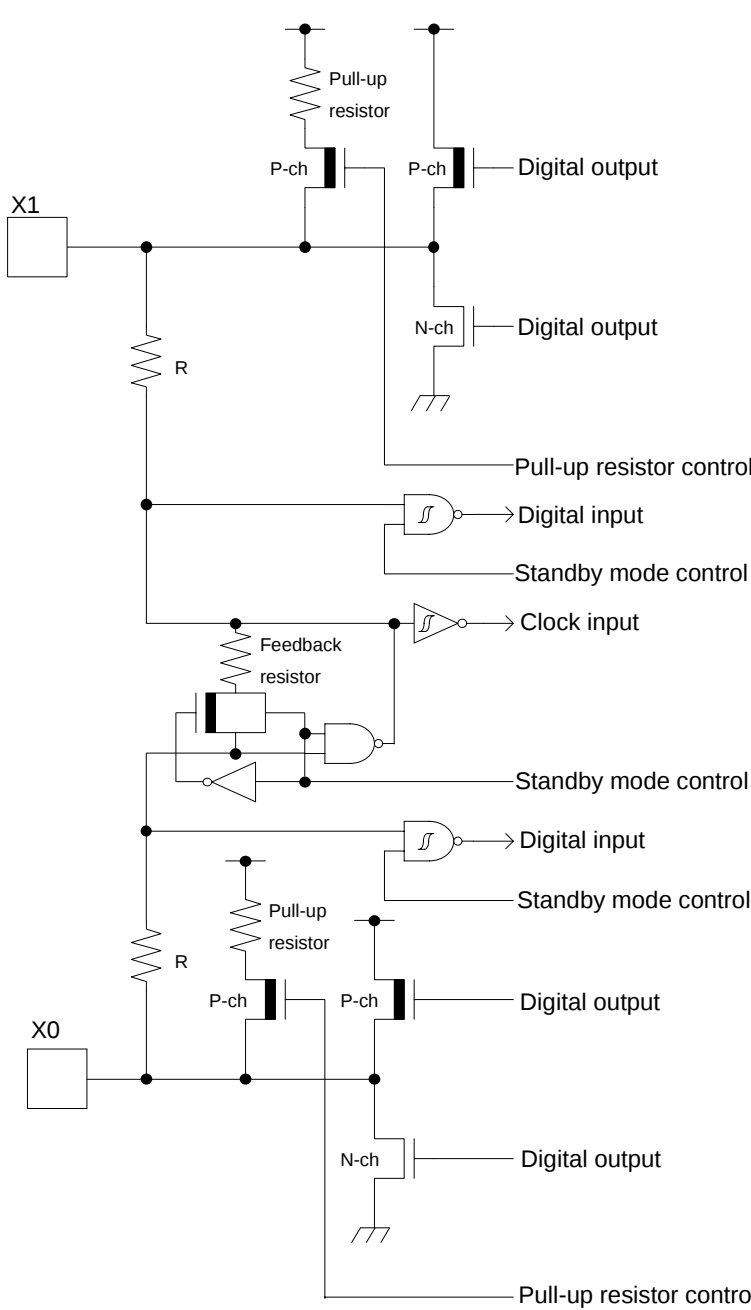
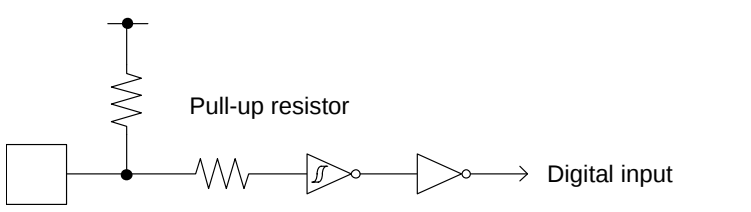
The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
1	1	1	C1	VCC	-	-
2	2	2	B2	PA0	G	K
				RTO20_0 (PPG20_0)		
				TIOA8_0		
				AIN2_0		
				INT00_0		
				MADATA00_0		
3	3	3	C2	PA1	G	I
				RTO21_0 (PPG20_0)		
				TIOA9_0		
				BIN2_0		
				MADATA01_0		
4	4	4	C3	PA2	G	I
				RTO22_0 (PPG22_0)		
				TIOA10_0		
				ZIN2_0		
				MADATA02_0		
5	5	5	D5	PA3	G	I
				RTO23_0 (PPG22_0)		
				TIOA11_0		
				MADATA03_0		
6	6	6	D2	PA4	G	I
				RTO24_0 (PPG24_0)		
				TIOA12_0		
				MADATA04_0		
7	7	7	D1	PA5	G	K
				SIN1_0		
				RTO25_0 (PPG24_0)		
				TIOA13_0		
				INT01_0		
				MADATA05_0		

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
84	69	59	J8	P74	E	I
				SCK9_0 (SCL9_0)		
				TIOB2_0		
				MAD03_0		
85	70	-	N8	PF2	L	I
				RTO10_1 (PPG10_1)		
				TIOA6_1		
				MRASX_0		
86	71	-	M8	PF3	L	K
				RTO11_1 (PPG10_1)		
				TIOB6_1		
				INT05_1 MCASX_0		
87	72	-	N9	PF4	L	K
				RTO12_1 (PPG12_1)		
				TIOA7_1		
				INT06_1 MSDWEX_0		
88	73	-	P9	PF5	L	K
				RTO13_1 (PPG12_1)		
				TIOB7_1		
				INT07_1 MCSX8_0		
89	74	-	M9	PF6	L	K
				RTO14_1 (PPG14_1)		
				TIOA14_1		
				INT20_1 MSDCKE_0		
90	75	-	L9	PF7	L	K
				RTO15_1 (PPG14_1)		
				TIOB14_1		
				INT21_1 MSDCLK_0		
91	76	60	K9	P75	E	K
				SIN8_0		
				TIOB3_0		
				AIN1_0 INT20_0 MAD04_0		
92	77	61	P10	P76	E	I
				SOT8_0 (SDA8_0)		
				TIOB4_0		
				BIN1_0 MAD05_0		

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation/GPIO function. When the main oscillation is selected: - Oscillation feedback resistor: approximately 1 MΩ - Standby mode control When the GPIO is selected: - CMOS level output. - CMOS level hysteresis input - Pull-up resistor control - Standby mode control - Pull-up resistor: approximately 50 kΩ $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$
B		- CMOS level hysteresis input - Pull-up resistor: approximately 50 kΩ

7. Handling Devices

Power-Supply Pins

In products with multiple VCC and VSS pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. All of these pins should be connected externally to the power supply or ground lines, however, in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating.

Be sure to connect the current-supply source with the power pins and GND pins of this device at low impedance. It is also advisable that a ceramic capacitor of approximately 0.1 μF be connected as a bypass capacitor between VCC and VSS near this device.

A malfunction may occur when the power-supply voltage fluctuates rapidly even though the fluctuation is within the guaranteed operating range of the VCC power supply voltage. As a rule of voltage stabilization, suppress voltage fluctuation so that the fluctuation in VCC ripple (peak-to-peak value) at the commercial frequency (50 Hz/60 Hz) does not exceed 10% of the standard VCC value, and the transient fluctuation rate does not exceed 0.1V/ μs at a momentary fluctuation such as switching the power supply.

Crystal Oscillator Circuit

Noise near the X0/X1 and X0A/X1A pins may cause the device to malfunction. Design the printed circuit board so that X0/X1, X0A/X1A pins, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.

It is strongly recommended that the PC board artwork be designed such that the X0/X1 and X0A/X1A pins are surrounded by ground plane, as this is expected to produce stable operation.

Evaluate the oscillation introduced by the use of the crystal oscillator by your mount board.

Sub Crystal Oscillator

The sub-oscillator circuit for devices in this family is low gain to keep current consumption low. To stabilize the oscillation, Cypress recommends a crystal oscillator that meets the following conditions:

- Surface mount type
 - Size: More than 3.2 mm $\times$ 1.5 mm
 - Load capacitance: Approximately 6 pF to 7 pF
- Lead type
 - Load capacitance: Approximately 6 pF to 7 pF

List of Pin Behavior by Mode State

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return From Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Main crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops*1, it will be Hi-Z/ Internal input fixed at 0					
C	INITX input pin	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ input enabled	GPIO selected	Hi-Z/ input enabled	GPIO selected

List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on reset*1	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer Mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return From Deep Standby Mode State	VBAT RTC Mode State	Return From VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	Sub crystal oscillator input pin/ external sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected		Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop mode

*8: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

Table 12-5 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency* ⁴	Value		Unit	Remarks
					Typ* ¹	Max* ²		
Power supply current	I _{CCS}	V _{CC}	Sleep operation* ⁵ (PLL)	200 MHz	88	188	mA	* ³ When all peripheral clocks are on
				192 MHz	85	184	mA	
				180 MHz	80	178	mA	
				160 MHz	72	164	mA	
				144 MHz	65	156	mA	
				120 MHz	55	144	mA	
				100 MHz	47	134	mA	
				80 MHz	38	124	mA	
				60 MHz	30	114	mA	
				40 MHz	21	104	mA	
				20 MHz	12	93	mA	
				8 MHz	7.4	87.2	mA	
				4 MHz	5.8	85.2	mA	* ³ When all peripheral clocks are off
				200 MHz	44	134	mA	
				192 MHz	42	132	mA	
				180 MHz	40	129	mA	
				160 MHz	36	123	mA	
				144 MHz	33	119	mA	
				120 MHz	28	113	mA	
				100 MHz	24	108	mA	
				80 MHz	20	103	mA	
				60 MHz	16	98	mA	
				40 MHz	12	93	mA	
				20 MHz	7.6	87.6	mA	
				8 MHz	5.2	84.7	mA	
				4 MHz	4.4	83.7	mA	

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

12.3.2 Pin Characteristics

($V_{CC} = USBV_{CC0} = USBV_{CC1} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	$V_{CC} \times 0.8$	-	$V_{CC} + 0.3$	V	
		MADATAxx	$V_{CC} > 3.0 V$, $V_{CC} \leq 3.6 V$,	2.4	-	$V_{CC} + 0.3$	V	At External Bus
		5 V tolerant input pin	-	$V_{CC} \times 0.8$	-	$V_{SS} + 5.5$	V	
		Input pin doubled as I ² C Fm+	-	$V_{CC} \times 0.7$	-	$V_{SS} + 5.5$	V	
		TTL Schmitt input pin	-	2.0	-	$V_{CC} + 0.3$	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
				$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
		5 V tolerant input pin	-	$V_{SS} - 0.3$	-	$V_{CC} \times 0.2$	V	
		Input pin doubled as I ² C Fm+	-	V_{SS}	-	$V_{CC} \times 0.3$	V	
		TTL Schmitt input pin	-	$V_{SS} - 0.3$	-	0.8	V	
H level output voltage	V_{OH}	4 mA type	$V_{CC} \geq 4.5 V$, $I_{OH} = -4 \text{ mA}$	$V_{CC} - 0.5$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$, $I_{OH} = -2 \text{ mA}$					
		8 mA type	$V_{CC} \geq 4.5 V$, $I_{OH} = -8 \text{ mA}$	$V_{CC} - 0.5$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$, $I_{OH} = -4 \text{ mA}$					
		10 mA type	$V_{CC} \geq 4.5 V$, $I_{OH} = -10 \text{ mA}$	$V_{CC} - 0.5$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$, $I_{OH} = -8 \text{ mA}$					
		12 mA type	$V_{CC} \geq 4.5 V$, $I_{OH} = -12 \text{ mA}$	$V_{CC} - 0.5$	-	V_{CC}	V	
			$V_{CC} < 4.5 V$, $I_{OH} = -8 \text{ mA}$					
		The pin doubled as USB I/O	$USBV_{CC} \geq 4.5 V$, $I_{OH} = -20.5 \text{ mA}$	$USBV_{CC} - 0.4$	-	$USBV_{CC}$	V	*1
			$USBV_{CC} < 4.5 V$, $I_{OH} = -13.0 \text{ mA}$					
		The pin doubled as I ² C Fm+	$V_{CC} \geq 4.5 V$, $I_{OH} = -4 \text{ mA}$	$V_{CC} - 0.5$	-	V_{CC}	V	At GPIO
			$V_{CC} < 4.5 V$, $I_{OH} = -3 \text{ mA}$					

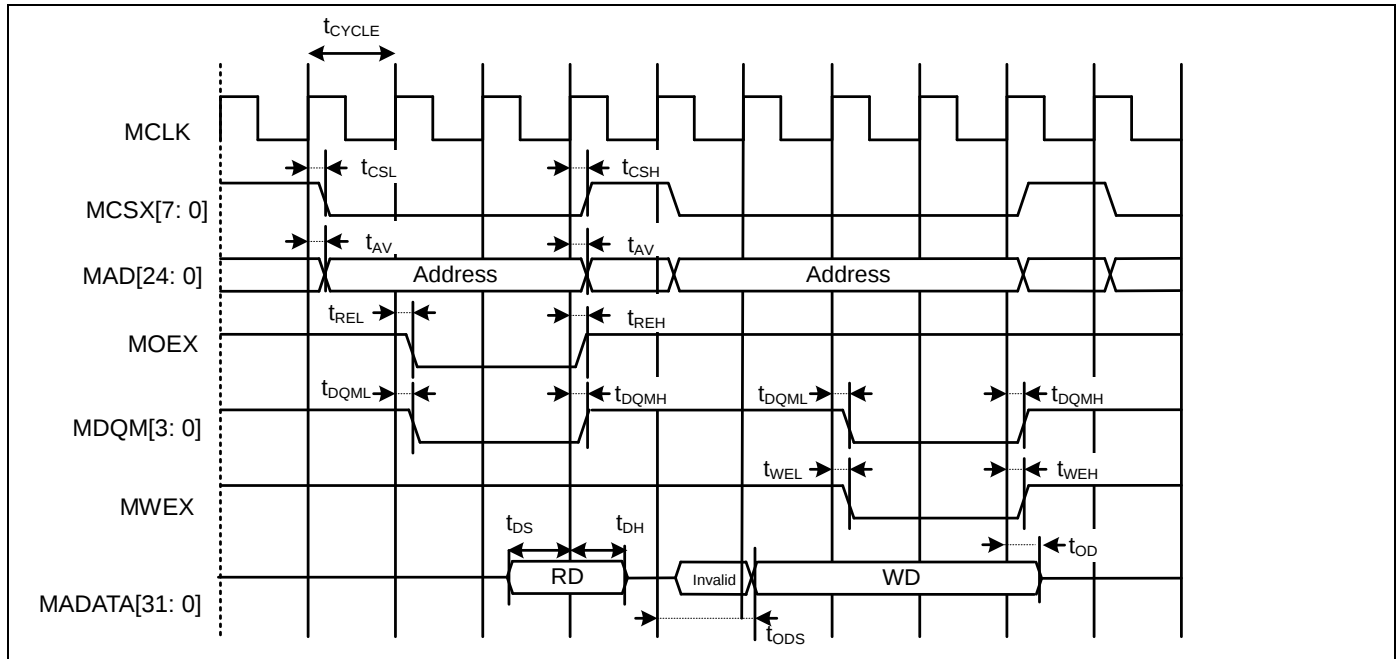
Separate Bus Access Synchronous SRAM Mode

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX[7: 0]	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up → MCLK ↑ time	t_{DS}	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1: 0] delay time	t_{DQML}	MCLK, MDQM[3: 0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[31: 0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[31: 0]	-	1	18	ns	

Note:

- When the external load capacitance $C_L = 30$ pF



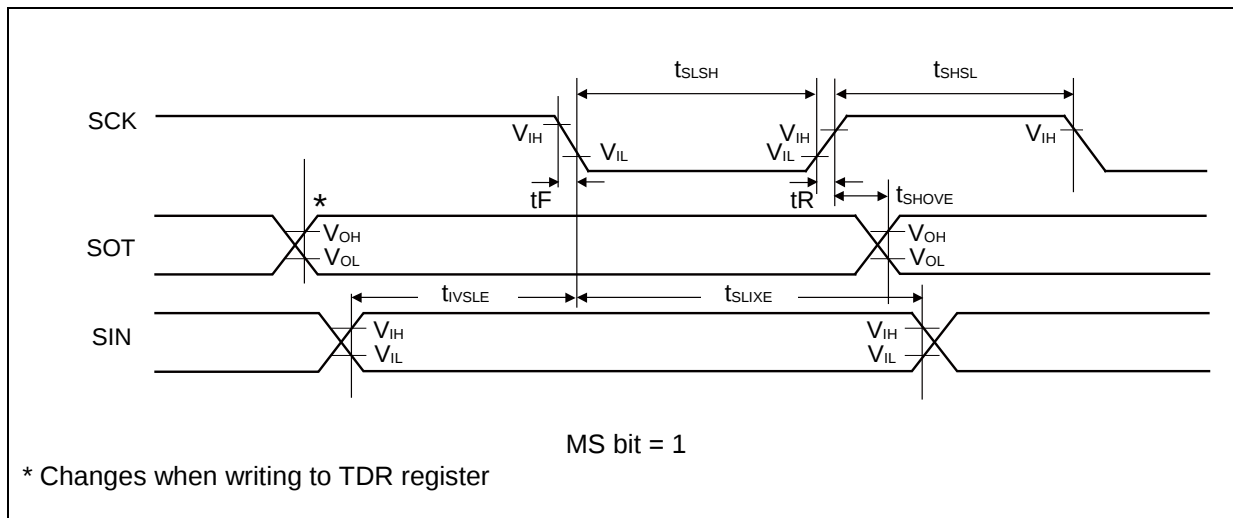
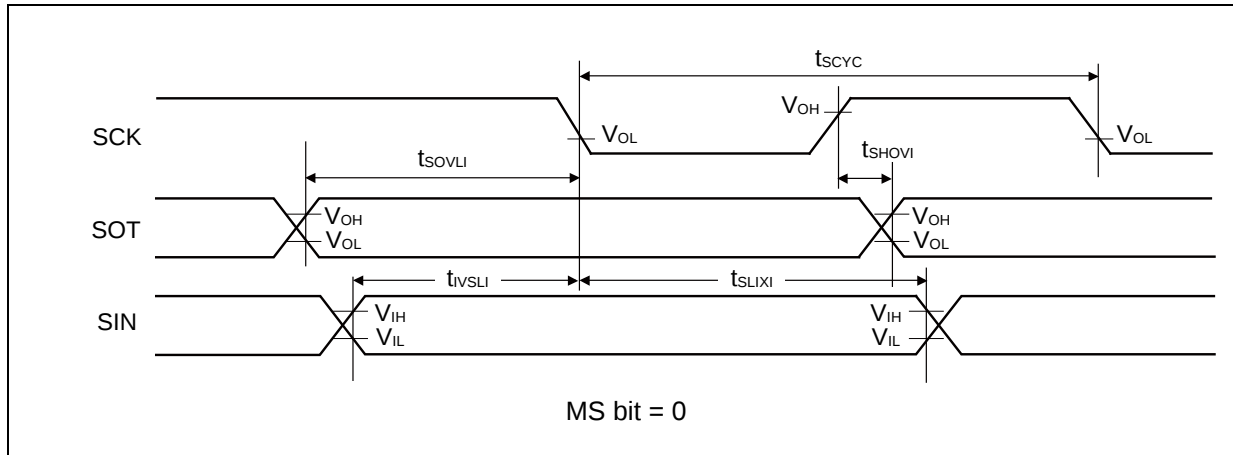
High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

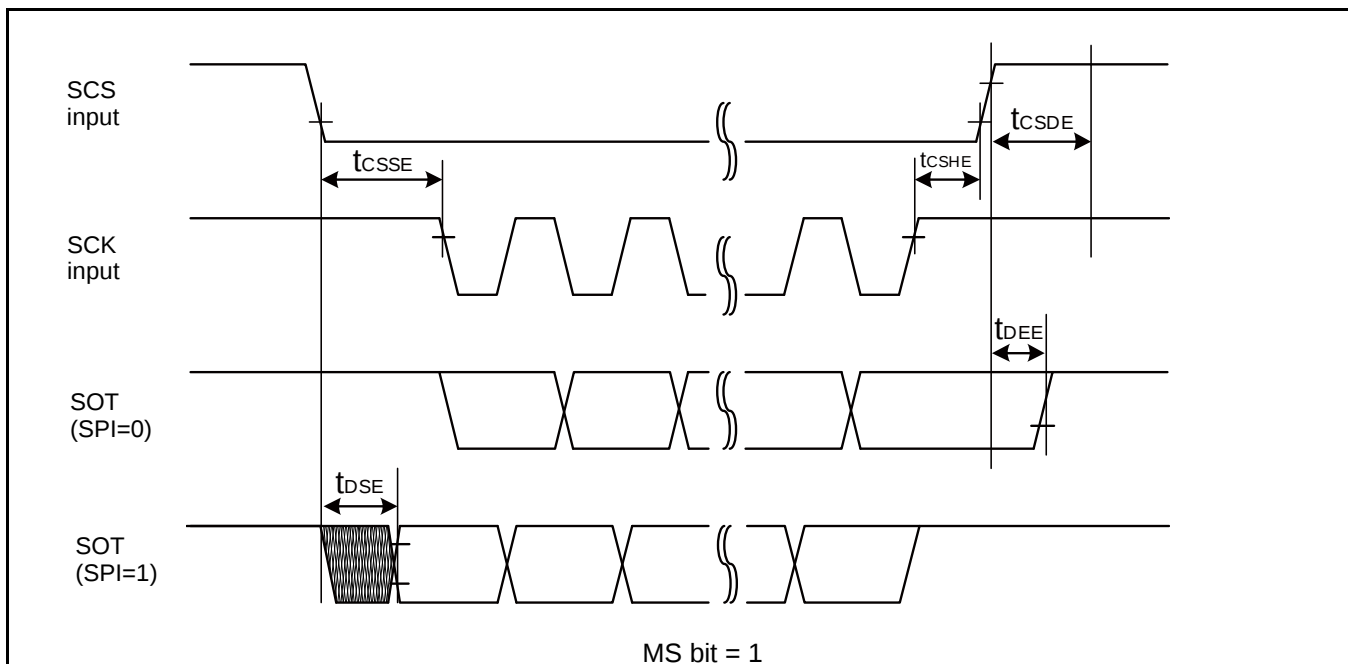
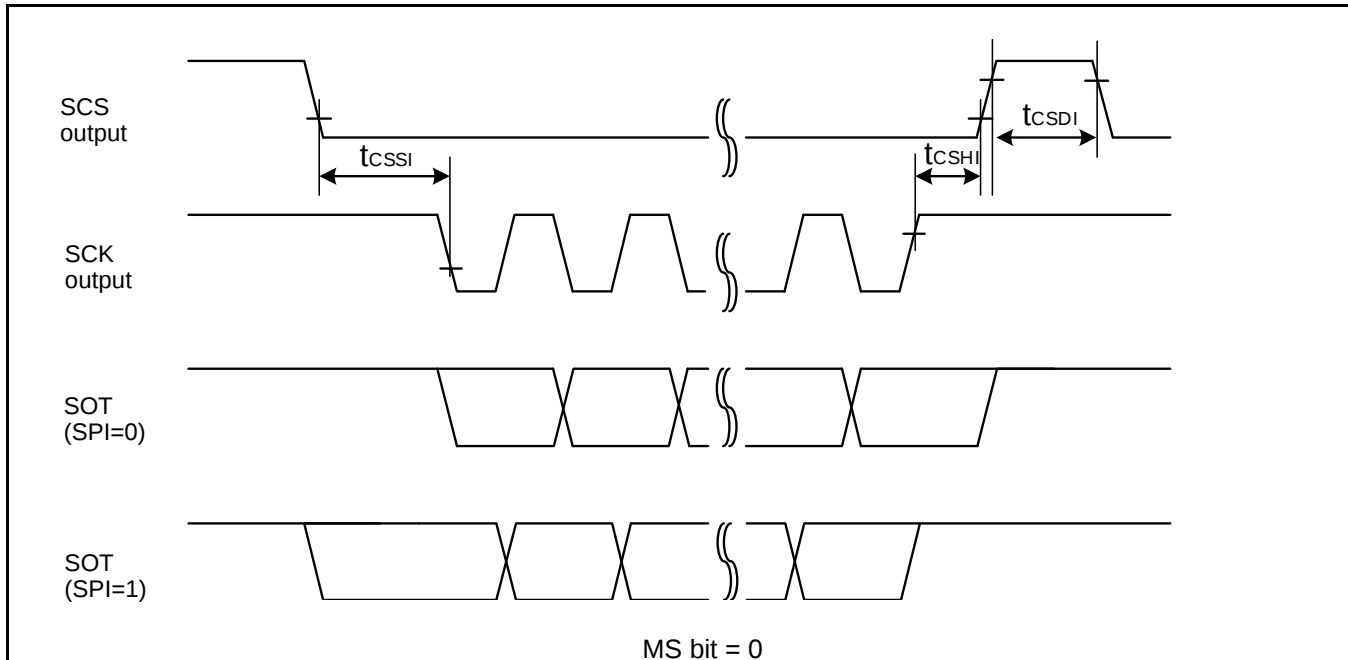
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↓→SOT delay time	t _{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t _{IVSHI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↑→SIN hold time	t _{SHIXI}	SCKx, SINx	External shift clock operation	5	-	5	-	ns
Serial clock L pulse width	t _{SLSH}	SCKx		2t _{CYCP} - 5	-	2t _{CYCP} - 5	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx		t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↓→SOT delay time	t _{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t _{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t _{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
 No chip select: SIN4_0, SOT4_0, SCK4_0
 Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)



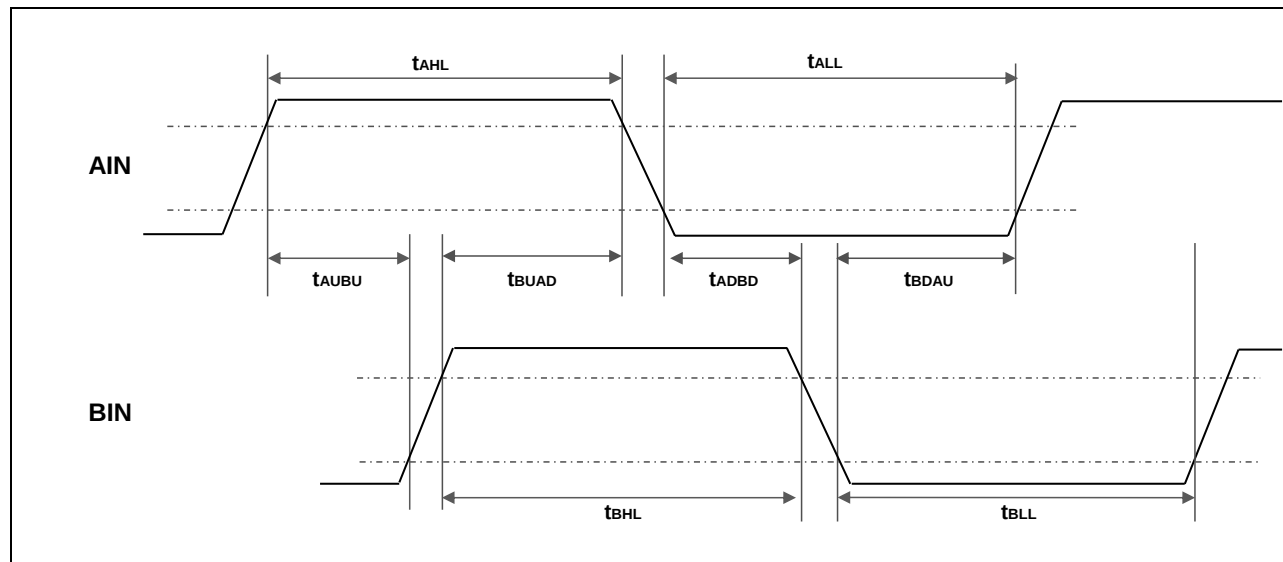


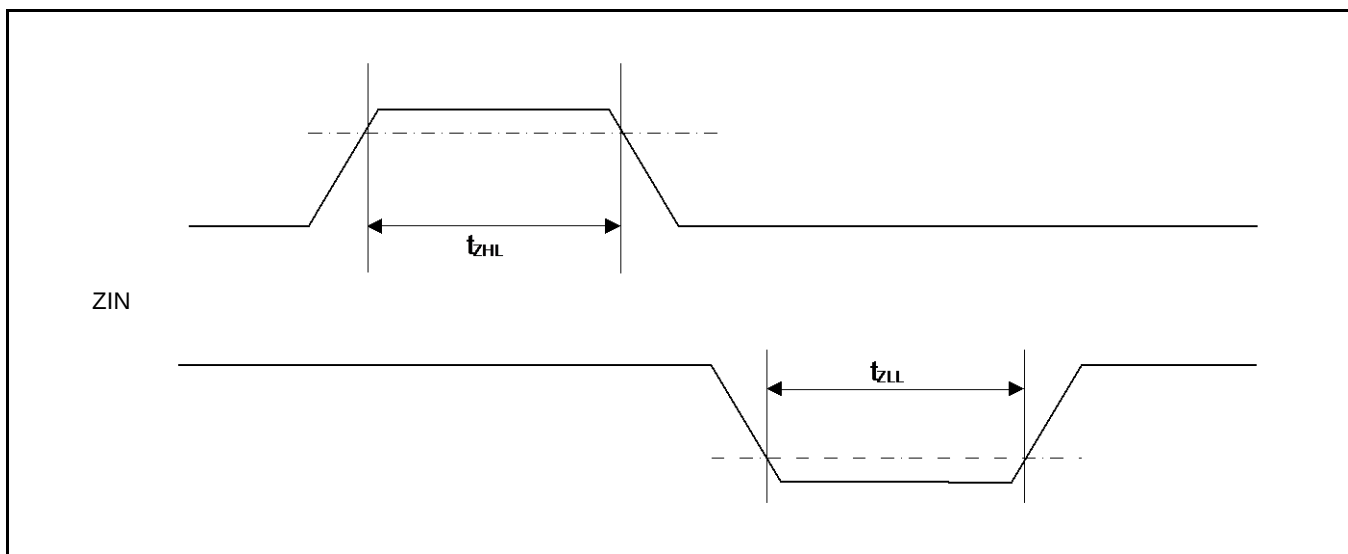
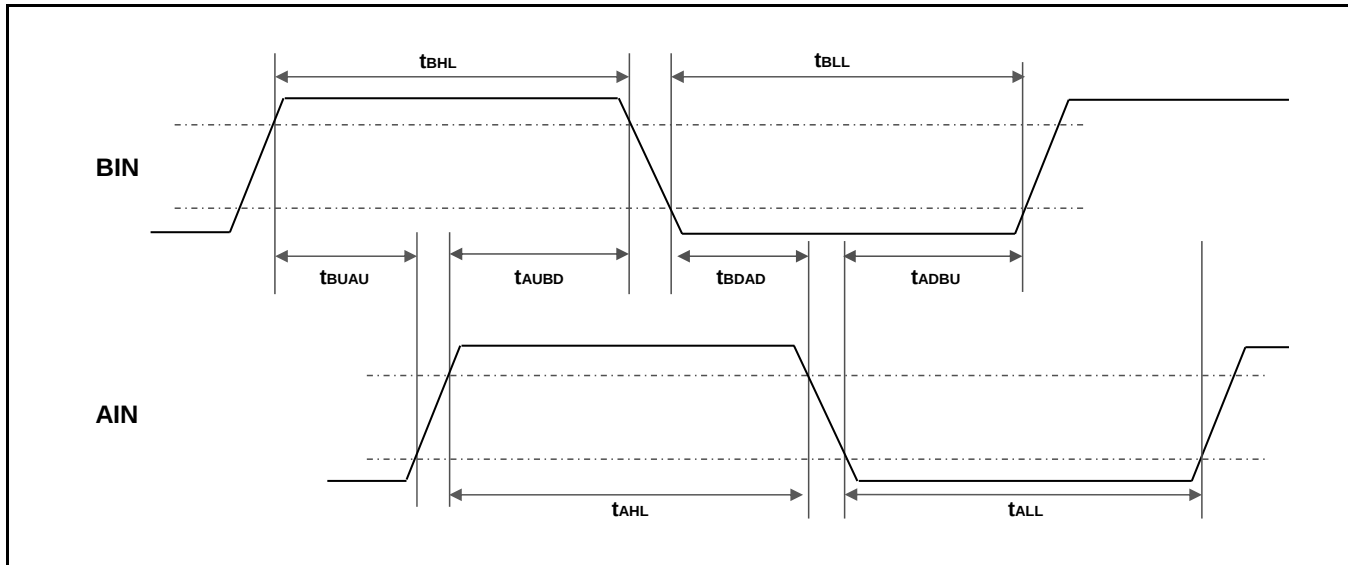
12.4.14 Quadrature Position/Revolution Counter Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}^*$	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rise time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR: CGSC = 0			
ZIN pin L width	t_{ZLL}	QCR: CGSC = 0			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR: CGSC = 1			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR: CGSC = 1			

*: t_{CYCP} indicates the APB bus clock cycle time except when in Stop mode, in Timer mode. For more information about the APB bus number to which the quadrature position/revolution counter is connected, see "8. Block Diagram" in this data sheet.





12.4.16 SD Card Interface Timing

Default-Speed Mode

■ Clock CLK (All values are referenced to V_{IH} and V_{IL} transition points)

($V_{CC} = 2.7V$ to $3.6V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	$C_{CARD} \leq 10$ pF (1card)	0	25	MHz
Clock frequency Identification Mode	f_{OD}	S_CLK		0/100	400	kHz
Clock low time	t_{WL}	S_CLK		10	-	ns
Clock high time	t_{WH}	S_CLK		10	-	ns
Clock rise time	t_{TLH}	S_CLK		-	10	ns
Clock fall time	t_{THL}	S_CLK		-	10	ns

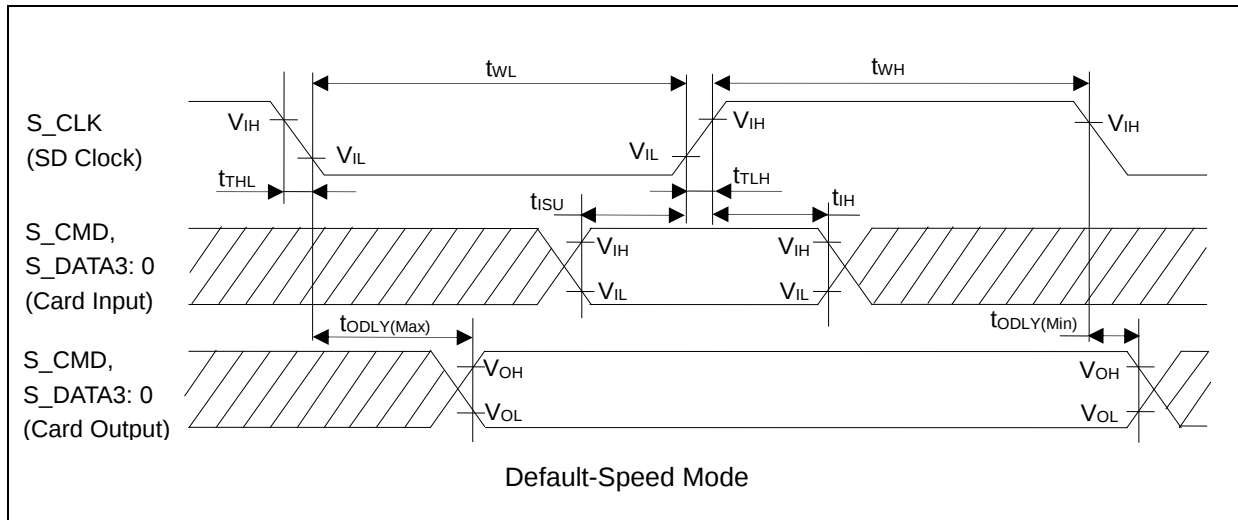
*: 0 Hz means to stop the clock. The given minimum frequency range is for cases where a continuous clock is required.

■ Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	$C_{CARD} \leq 10$ pF (1card)	5	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		5	-	ns

■ Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output Delay time during Data Transfer Mode	t_{ODLY}	S_CMD, S_DATA3: 0	$C_{CARD} \leq 40$ pF (1card)	0	14	ns
Output Delay time during Identification Mode	t_{ODLY}	S_CMD, S_DATA3: 0		0	50	ns

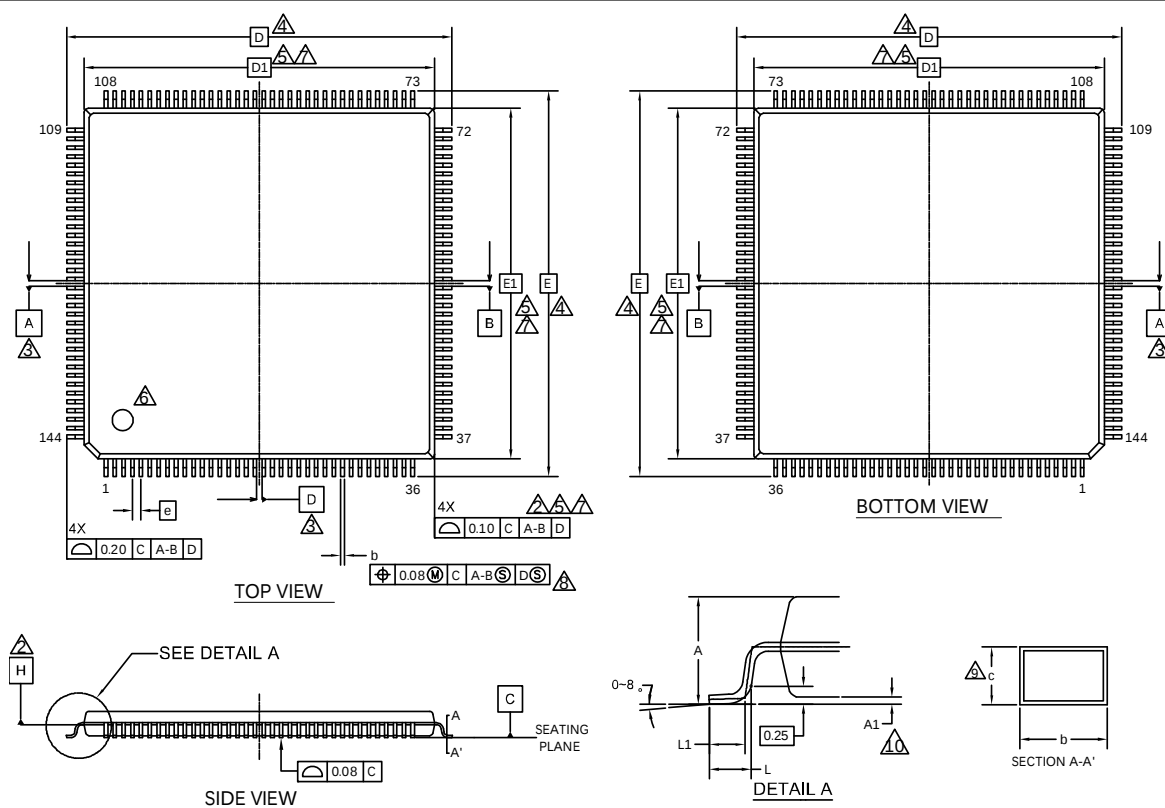


Notes:

- The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.
- For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).

14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS 144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.00	—	0.20
b	0.17	0.22	0.27
c	0.09	—	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE.
- DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 **

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 Rev**