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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, I ² C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c59j0agv2000a

2. Packages

Package \ Product Name	S6E2C58H0A S6E2C59H0A S6E2C5AH0A	S6E2C58J0A S6E2C59J0A S6E2C5AJ0A	S6E2C58L0A S6E2C59L0A S6E2C5AL0A
LQFP: LQS144 (0.5-mm pitch)	○	-	-
LQFP: LQP176 (0.5-mm pitch)	-	○	-
BGA : LBE192 (0.8-mm pitch)	-	○	-
LQFP: LQQ216 (0.4-mm pitch)	-	-	○

○: Supported

Note:

- See 14. Package Dimensions for detailed information on each package.

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
84	69	59	J8	P74	E	I
				SCK9_0 (SCL9_0)		
				TIOB2_0		
				MAD03_0		
85	70	-	N8	PF2	L	I
				RTO10_1 (PPG10_1)		
				TIOA6_1		
				MRASX_0		
86	71	-	M8	PF3	L	K
				RTO11_1 (PPG10_1)		
				TIOB6_1		
				INT05_1 MCASX_0		
87	72	-	N9	PF4	L	K
				RTO12_1 (PPG12_1)		
				TIOA7_1		
				INT06_1 MSDWEX_0		
88	73	-	P9	PF5	L	K
				RTO13_1 (PPG12_1)		
				TIOB7_1		
				INT07_1 MCSX8_0		
89	74	-	M9	PF6	L	K
				RTO14_1 (PPG14_1)		
				TIOA14_1		
				INT20_1 MSDCKE_0		
90	75	-	L9	PF7	L	K
				RTO15_1 (PPG14_1)		
				TIOB14_1		
				INT21_1 MSDCLK_0		
91	76	60	K9	P75	E	K
				SIN8_0		
				TIOB3_0		
				AIN1_0 INT20_0 MAD04_0		
92	77	61	P10	P76	E	I
				SOT8_0 (SDA8_0)		
				TIOB4_0		
				BIN1_0 MAD05_0		

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
154	124	100	E12	P24	F	L
				AN29		
				TIOA13_1		
				MAD18_0		
155	125	101	E13	P23	F	L
				UHCONX1		
				AN30		
				SCK0_0 (SCL0_0)		
156	126	102	D12	TIOB13_1	F	M
				P22		
				AN31		
				SOT0_0 (SDA0_0)		
157	127	103	D13	INT26_0	I	K
				P21		
				ADTG_4		
				SIN0_0		
158	128	104	C13	INT27_0	I	F
				CROUT_0		
				P20		
				NMIX		
159	129	105	E14	WKUP0	-	-
				USBVCC1		
160	130	106	D14	P82	H	R
				UDM1		
161	131	107	C14	P83	H	R
				UDP1		
162	132	108	B14	VSS	-	-
163	133	109	A13	VCC	-	-
164	134	110	B13	P00	E	G
				TRSTX		
165	135	111	A12	P01	E	G
				TCK		
				SWCLK		
166	136	112	C12	P02	E	G
				TDI		
167	137	113	B12	P03	E	G
				TMS		
				SWDIO		
168	138	114	B11	P04	E	G
				TDO		
				SWO		
169	139	-	C11	P90	S	K
				INT12_1		
				Q_IO3_0		
170	140	-	D11	P91	S	K
				SIN5_1		
				INT13_1		
				Q_IO2_0		
171	141	-	B10	P92	S	K
				SOT5_1 (SDA5_1)		
				INT14_1		
				Q_IO1_0		

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 7	TIOA7_0	Base Timer ch.7 TIOA Pin	181	149	119	F9
	TIOA7_1		87	72	-	N9
	TIOA7_2		202	-	-	-
	TIOB7_0	Base Timer ch.7 TIOB Pin	180	148	118	E9
	TIOB7_1		88	73	-	P9
	TIOB7_2		201	-	-	-
Base Timer 8	TIOA8_0	Base Timer ch.8 TIOA Pin	2	2	2	B2
	TIOA8_1		142	116	92	G10
	TIOA8_2		10	10	-	E2
	TIOB8_0	Base Timer ch.8 TIOB Pin	18	17	14	F4
	TIOB8_1		143	117	93	G9
	TIOB8_2		11	11	-	E3
Base Timer 9	TIOA9_0	Base Timer ch.9 TIOA Pin	3	3	3	C2
	TIOA9_1		126	102	-	J10
	TIOA9_2		12	12	-	E4
	TIOB9_0	Base Timer ch.9 TIOB Pin	23	18	15	F5
	TIOB9_1		127	103	-	J9
	TIOB9_2		13	-	-	-
Base Timer 10	TIOA10_0	Base Timer ch.10 TIOA Pin	4	4	4	C3
	TIOA10_1		128	104	-	H10
	TIOA10_2		19	-	-	-
	TIOB10_0	Base Timer ch.10 TIOB Pin	24	19	16	F6
	TIOB10_1		129	105	-	J14
	TIOB10_2		20	-	-	-
Base Timer 11	TIOA11_0	Base Timer ch.11 $\emptyset$ TIOA Pin	5	5	5	D5
	TIOA11_1		138	112	-	G13
	TIOA11_2		33	-	-	-
	TIOB11_0	Base Timer ch.11 TIOB Pin	25	20	17	G2
	TIOB11_1		139	113	-	F14
	TIOB11_2		51	41	-	L2
Base Timer 12	TIOA12_0	Base Timer ch.12 TIOA Pin	6	6	6	D2
	TIOA12_1		140	114	-	G12
	TIOA12_2		52	42	-	L3
	TIOB12_0	Base Timer ch.12 TIOB Pin	30	21	18	G3
	TIOB12_1		141	115	-	G11
	TIOB12_2		53	43	-	M2

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 13	TIOA13_0	Base Timer ch.13 TIOA Pin	7	7	7	D1
	TIOA13_1		154	124	100	E12
	TIOA13_2		34	24	-	G6
	TIOB13_0	Base Timer ch.13 TIOB Pin	31	22	19	G4
	TIOB13_1		155	125	101	E13
	TIOB13_2		35	25	-	H4
Base Timer 14	TIOA14_0	Base Timer ch.14 TIOA Pin	183	151	121	D8
	TIOA14_1		89	74	-	M9
	TIOA14_2		204	-	-	-
	TIOB14_0	Base Timer ch.14 TIOB Pin	182	150	120	C8
	TIOB14_1		90	75	-	L9
	TIOB14_2		203	-	-	-
Base Timer 15	TIOA15_0	Base Timer ch.15 TIOA Pin	187	155	125	B7
	TIOA15_1		78	63	-	K5
	TIOA15_2		206	-	-	-
	TIOB15_0	Base Timer ch.15 TIOB Pin	186	154	124	F8
	TIOB15_1		79	64	-	K6
	TIOB15_2		205	-	-	-
CAN 0	TX0_0	CAN interface ch.0 TX output pin	18	17	14	F4
	TX0_1		35	25	-	H4
	TX0_2		176	-	-	-
	RX0_0	CAN interface ch.0 RX output pin	17	16	13	F3
	RX0_1		34	24	-	G6
	RX0_2		175	-	-	-
CAN 1	TX1_0	CAN interface ch.1 TX output pin	152	122	98	E10
	TX1_1		118	98	82	K11
	TX1_2		148	-	-	-
	RX1_0	CAN interface ch.1 RX output pin	153	123	99	E11
	RX1_1		117	97	81	K14
	RX1_2		149	-	-	-
CAN 2 (CAN-FD)	TX2_0	CAN-FD interface ch.2 TX output pin	71	56	48	M5
	TX2_1		79	64	-	K6
	TX2_2		69	-	-	-
	RX2_0	CAN-FD interface ch.2 RX input pin	70	55	47	L5
	RX2_1		78	63	-	K5
	RX2_2		68	-	-	-

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PA0	General-purpose I/O port A	2	2	2	B2
	PA1		3	3	3	C2
	PA2		4	4	4	C3
	PA3		5	5	5	D5
	PA4		6	6	6	D2
	PA5		7	7	7	D1
	PA6		8	8	8	D3
	PA7		9	9	9	D4
	PA8		14	13	10	E5
	PA9		15	14	11	F1
	PAA		16	15	12	F2
	PAB		17	16	13	F3
	PAC		18	17	14	F4
	PAD		23	18	15	F5
	PAE		24	19	16	F6
	PAF		25	20	17	G2
	PB0	General-purpose I/O port B	126	102	-	J10
	PB1		127	103	-	J9
	PB2		128	104	-	H10
	PB3		129	105	-	J14
	PB4		138	112	-	G13
	PB5		139	113	-	F14
	PB6		140	114	-	G12
	PB7		141	115	-	G11
	PB8		119	-	-	-
	PB9		120	-	-	-
	PBA		121	-	-	-
	PBB		122	-	-	-
	PBC		148	-	-	-
	PBD		149	-	-	-
	PBE		150	-	-	-
	PBF		151	-	-	-

11. Pin Status in Each CPU State

The terms used for pin status have the following meanings:

■ **INITX = 0**

This is the period when the INITX pin is at the L level.

■ **INITX = 1**

This is the period when the INITX pin is at the H level.

■ **SPL = 0**

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 0.

■ **SPL = 1**

This is the status that the standby pin level setting bit (SPL) in the standby mode control register (STB_CTL) is set to 1.

■ **Input enabled**

Indicates that the input function can be used.

■ **Internal input fixed at 0**

This is the status that the input function cannot be used. Internal input is fixed at L.

■ **Hi-Z**

Indicates that the pin drive transistor is disabled and the pin is put in the Hi-Z state.

■ **Setting disabled**

Indicates that the setting is disabled.

■ **Maintain previous state**

Maintains the state that was immediately prior to entering the current mode.

If a built-in peripheral function is operating, the output follows the peripheral function.

If the pin is being used as a port, that output is maintained.

■ **Analog input is enabled**

Indicates that the analog input is enabled.

■ **Trace output**

Indicates that the trace function can be used.

■ **GPIO selected**

In Deep standby mode, pins switch to the general-purpose I/O port.

■ **Setting prohibition**

Prohibition of a setting by specification limitation

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return From Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
M	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/ internal input fixed at 0			
N	GPIO selected									
	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	Trace selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Trace output	GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
	Resource other than above selected						Hi-Z/ internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return From Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled
	External interrupt enable selected									
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/ internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
	GPIO selected									
R	GPIO selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled	Maintain previous state	Maintain previous state	Hi-Z/ internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at 0	GPIO selected
	USB I/O pin	Setting disabled	Setting disabled	Setting disabled	Hi-Z at transmission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at transmission/ input enabled/ internal input fixed at 0 at reception	Hi-Z at transmission/ input enabled/ internal input fixed at 0 at reception	Hi-Z/ input enabled	Hi-Z/ input enabled	Hi-Z/ input enabled
V	Ethernet I/O selected *4	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/ internal input fixed at "0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/ internal input fixed at 0			
	GPIO selected									

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return From Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
W	Ethernet input/output selected*4	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External interrupt enable selected									
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled						
	GPIO selected									

*1: Oscillation is stopped at sub Timer mode, sub CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

*2: Maintain previous state at Timer mode. GPIO selected internal input fixed at 0 at RTC mode, Stop mode.

*3: Maintain previous state at Timer mode. Hi-Z/internal input fixed at 0 at RTC mode, Stop mode.

*4: It shows the case selected by EPFR14.E_SPLC register.

Table 12-4 Typical and Maximum Current Consumption in Normal Operation (Other Than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I _{CC}	V _{CC}	Normal operation *6, *7 (main oscillation)	*5	4 MHz	4.7	84.9	mA	*3 When all peripheral clocks are on
						3.9	83.8	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in High-speed CR)	*5	4 MHz	3.0	83.2	mA	*3 When all peripheral clocks are on
						2.1	82.0	mA	*3 When all peripheral clocks are off
			Normal operation *6, *8 (sub oscillation)	*5	32 kHz	0.78	80.37	mA	*3 When all peripheral clocks are on
						0.77	80.36	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in low-speed CR)	*5	100 kHz	0.81	80.39	mA	*3 When all peripheral clocks are on
						0.78	80.38	mA	*3 When all peripheral clocks are off

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

*6: With data access to a MainFlash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

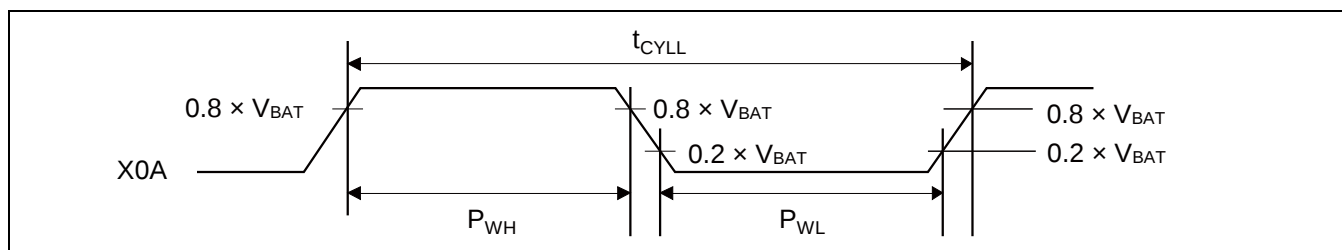
*8: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

12.4.2 Sub Clock Input Characteristics

($V_{BAT} = 1.65V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	μs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL} , P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see Sub crystal oscillator in 7. Handling Devices.



12.4.3 Built-In CR Oscillation Characteristics

Built-In High-speed CR

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	$T_J = -20^{\circ}C$ to $+105^{\circ}C$	3.92	4	4.08	MHz	When trimming *1
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	3.88	4	4.12		
		$T_J = -40^{\circ}C$ to $+125^{\circ}C$	3	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	μs	*2

*1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

*2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

Built-In Low-speed CR

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

12.4.12 CSIO (SPI) Timing

Synchronous serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-		-	8	-	8	Mbps
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↓→SOT delay time	t _{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t _{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t _{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t _{SLSH}	SCKx		2t _{CYCP} - 10	-	2t _{CYCP} - 10	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx	External shift clock operation	t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↓→SOT delay time	t _{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t _{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t _{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.

When Using Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t _{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK↑→SCS↑ hold time	t _{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t _{CSDI}		(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	ns
SCS↓→SCK↓ setup time	t _{CSSE}	External shift clock operation	3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCK↑→SCS↑ hold time	t _{CSHE}		0	-	0	-	ns
SCS deselect time	t _{CSDE}		3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCS ↓ →SOT delay time	t _{DSE}		-	40	-	40	ns
SCS ↑ →SOT delay time	t _{DSE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C_L = 30 pF.

When Using Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Units
			Min	Max	Min	Max	
SCS ↑ → SCK ↑ setup time	t _{CSSI}	Internal shift clock operation	(*1)-50	(*1)+0	(*1)-50	(*1)+0	ns
SCK ↓ → SCS ↓ hold time	t _{CSHI}		(*2)+0	(*2)+50	(*2)+0	(*2)+50	ns
SCS deselect time	t _{CSDI}		(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	(*3)-50 +5t _{CYCP}	(*3)+50 +5t _{CYCP}	ns
SCS ↑ → SCK ↑ setup time	t _{CSSE}	External shift clock operation	3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCK ↓ → SCS ↓ hold time	t _{CSHE}		0	-	0	-	ns
SCS deselect time	t _{CSDE}		3t _{CYCP} +30	-	3t _{CYCP} +30	-	ns
SCS ↑ → SOT delay time	t _{DSE}		-	40	-	40	ns
SCS ↓ → SOT delay time	t _{DEE}		0	-	0	-	ns

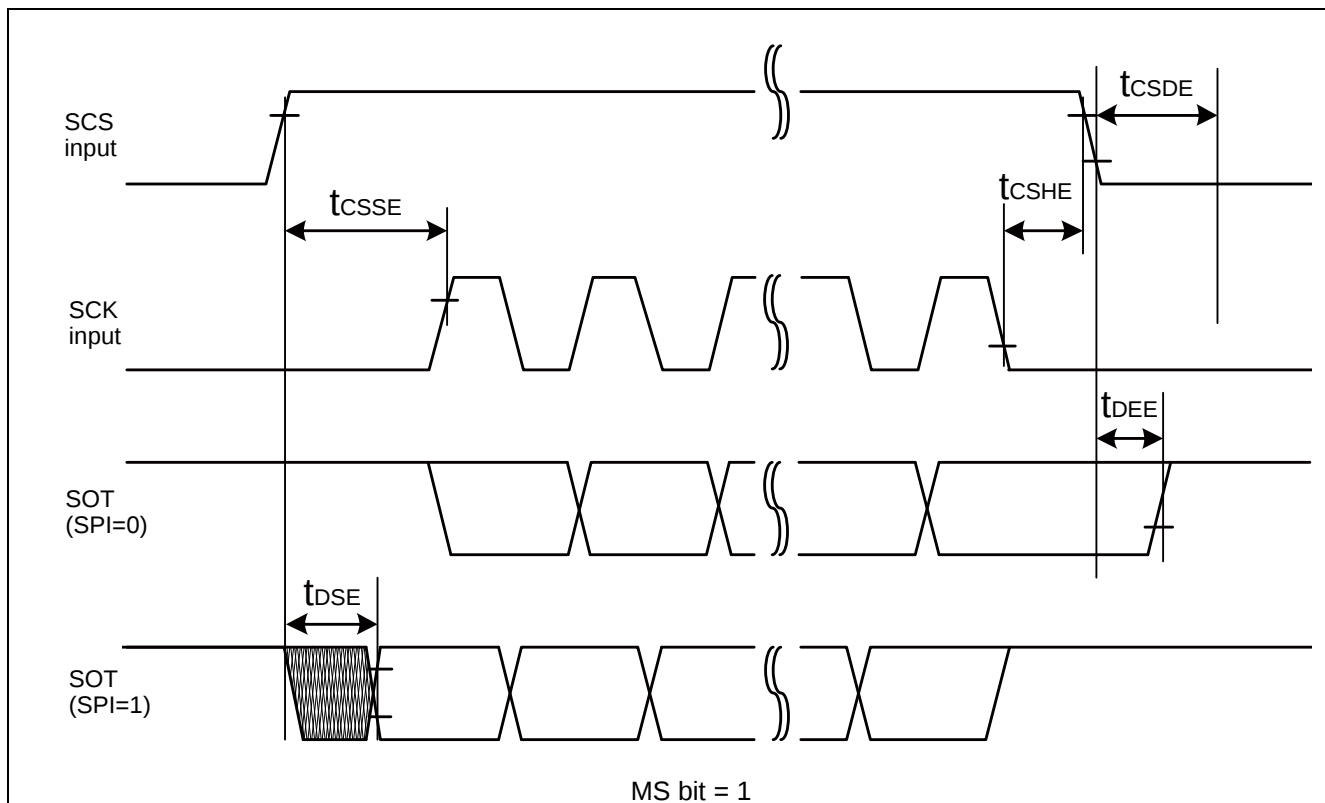
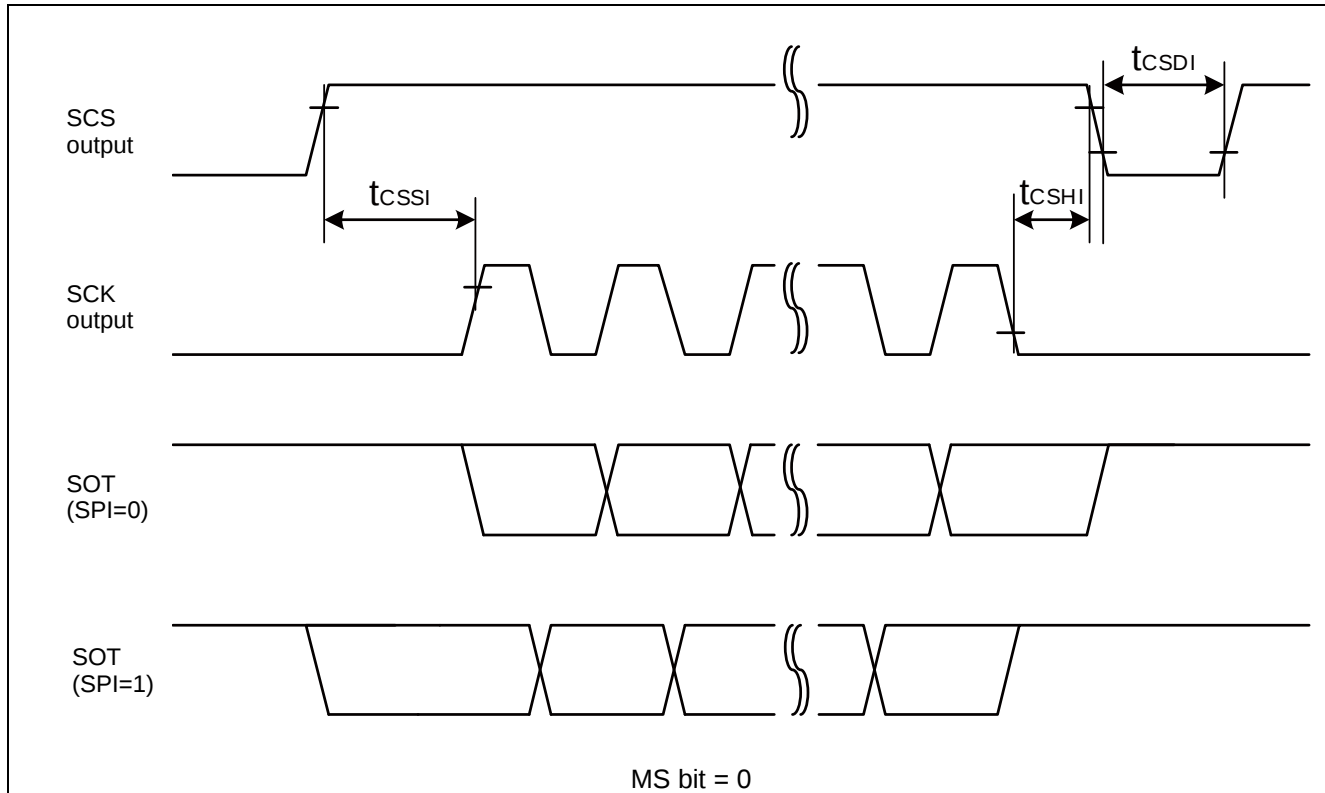
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C_L = 30 pF.



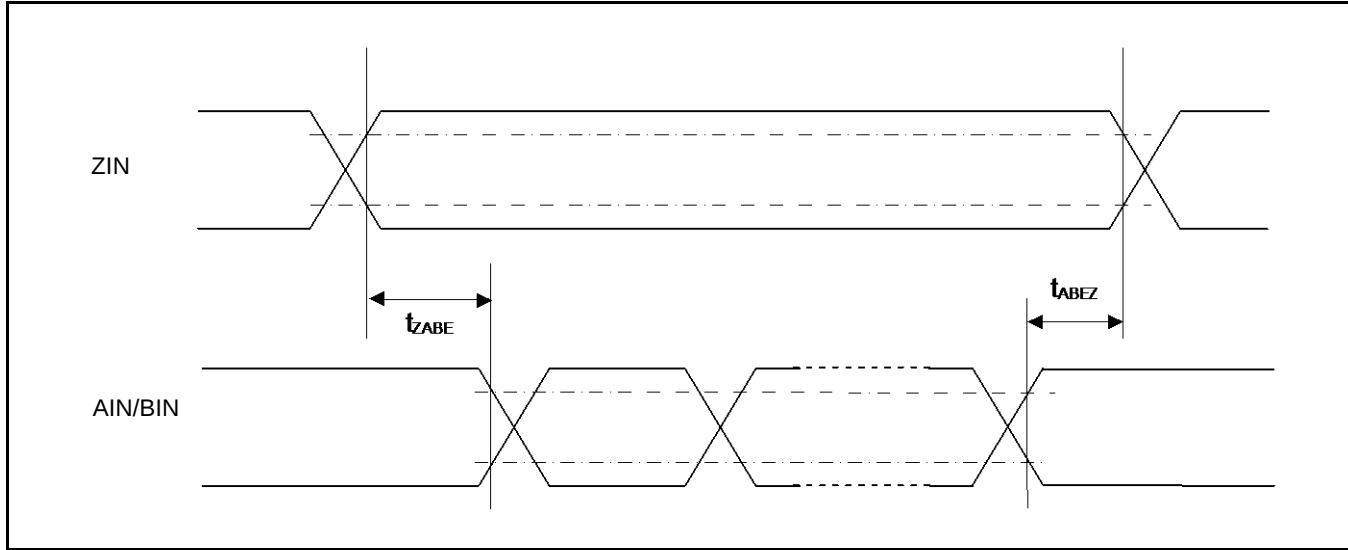
High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↓→SOT delay time	t _{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t _{IVSHI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↑→SIN hold time	t _{SHIXI}	SCKx, SINx	External shift clock operation	5	-	5	-	ns
Serial clock L pulse width	t _{SLSH}	SCKx		2t _{CYCP} - 5	-	2t _{CYCP} - 5	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx		t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↓→SOT delay time	t _{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t _{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t _{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

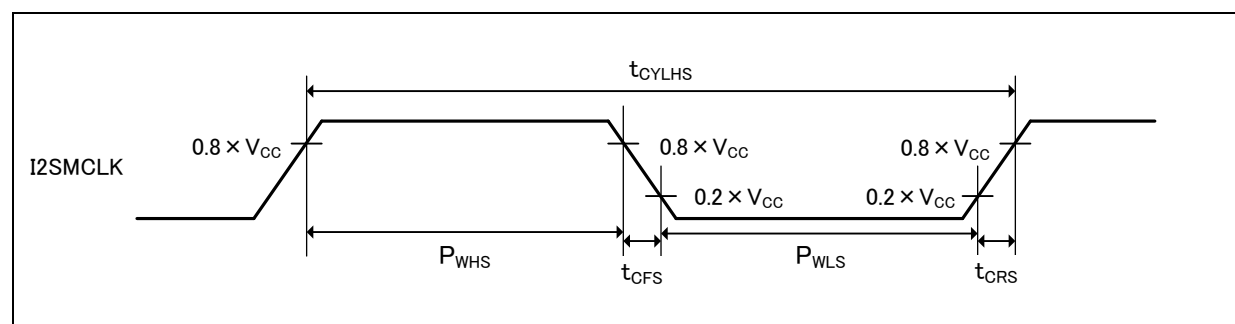
- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
 No chip select: SIN4_0, SOT4_0, SCK4_0
 Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)



I2SMCLK Input Characteristics

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

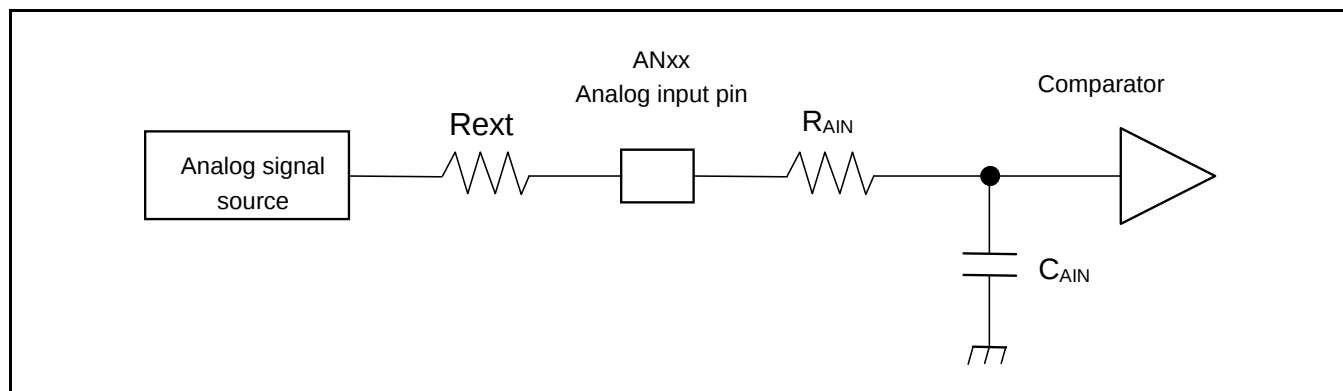
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input frequency	f_{CHS}	I2SMCK	-	-	25	MHz	
Input clock cycle	t_{CYLHS}	-	-	40	-	ns	
Input clock pulse width	-	-	P_{WHS}/t_{CYLHS} P_{WLS}/t_{CYLHS}	45	55	%	When using external clock
Input clock rise time and fall time	t_{CFS} t_{CRS}	-	-	-	5	ns	When using external clock



I2SMCLK Output Characteristics

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Output frequency	f_{CHS}	I2SMCK	-	-	12.288	MHz	



(Equation 1) $T_s \geq (R_{AIN} + R_{ext}) \times C_{AIN} \times 9$

- t_s : Sampling time
- R_{AIN} : Input resistance of A/D = 1.2 k Ω at $4.5V \leq AV_{CC} \leq 5.5V$
Input resistance of A/D = 1.8 k Ω at $2.7V \leq AV_{CC} < 4.5V$
- C_{AIN} : Input capacity of A/D = 12.05 pF at $2.7V \leq AV_{CC} \leq 5.5V$
- R_{ext} : Output impedance of external circuit

(Equation 2) $T_c = T_{cck} \times 14$

- t_c : Compare time
- t_{cck} : Compare clock cycle