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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, I ² C, LINbus, SD, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c5ah0agv2000a

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
37	27	22	J1	P33	L	I
				FRCK0_0		
				ZIN2_1		
				S_DATA0_0		
38	28	23	H3	P34	L	K
				IC03_0		
				INT00_1		
				S_CLK_0		
39	29	24	H1	VCC	-	-
40	30	25	H5	VSS	-	-
41	31	26	H6	P35	L	K
				IC02_0		
				INT01_1		
				S_CMD_0		
42	32	27	J5	P36	L	K
				IC01_0		
				INT02_1		
				S_DATA3_0		
43	33	28	J4	P37	L	K
				IC00_0		
				INT03_1		
				S_DATA2_0		
44	34	29	J3	P38	E	I
				ADTG_2		
				DTTIOX_0		
				S_WP_0		
45	35	30	J2	P39	G	K
				SIN2_1		
				RTO00_0 (PPG00_0)		
				TIOA0_1		
				AIN3_1		
				INT16_1		
				S_CD_0		
				MAD24_0		
46	36	31	K1	P3A	G	K
				SOT2_1 (SDA2_1)		
				RTO01_0 (PPG00_0)		
				TIOA1_1		
				BIN3_1		
				INT17_1		
				MAD23_0		
47	37	32	K2	P3B	G	K
				SCK2_1 (SCL2_1)		
				RTO02_0 (PPG02_0)		
				TIOA2_1		
				ZIN3_1		
				INT18_1		
				MAD22_0		
				MNALE_0		

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
69	-	-	-	P4E	E	I
				SCS73_1		
				TX2_2		
70	55	47	L5	P7D	L	Q
				SCK1_1 (SCL1_1)		
				RX2_0		
				DTT1X_0		
				INT05_0		
				WKUP2		
				MCSX1_0		
71	56	48	M5	P7E	L	I
				ADTG_7		
				TX2_0		
				FRCK1_0		
				MCSX0_0		
72	57	49	N5	INITX	B	C
73	58	50	P5	P46	P	S
				X0A		
74	59	51	P6	P47	Q	T
				X1A		
75	60	52	P8	VBAT	-	-
76	61	53	N6	P48	O	U
				VREGCTL		
77	62	54	M6	P49	O	U
				VWAKEUP		
78	63	-	K5	PF0	E	K
				SCS63_0		
				RX2_1		
				FRCK1_1		
				TIOA15_1		
				INT22_1		
79	64	-	K6	PF1	E	K
				SCS62_0		
				TX2_1		
				TIOB15_1		
				INT23_1		
80	65	55	L6	P70	I	K
				ADTG_8		
				SIN1_1		
				INT06_0		
				MRDY_0		
81	66	56	J6	P71	E	I
				SOT1_1 (SDA1_1)		
				MAD00_0		
82	67	57	L8	P72	E	K
				SIN9_0		
				TIOB0_0		
				INT07_0		
				MAD01_0		
83	68	58	K8	P73	E	I
				SOT9_0 (SDA9_0)		
				TIOB1_0		
				MAD02_0		

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
106	86	70	P12	PE2	A	A
				X0		
107	87	71	P13	PE3	A	B
				X1		
108	88	72	N14	VSS	-	-
109	89	73	M14	VCC	-	-
110	90	74	M13	AVCC	-	-
111	91	75	M12	AVSS	-	-
112	92	76	L13	AVRL	-	-
113	93	77	L12	AVRH	-	-
114	94	78	L11	P10	F	M
				AN00		
				SIN10_0		
				TIOA0_2		
				AIN0_2		
				INT08_0		
115	95	79	K13	P11	F	L
				AN01		
				SOT10_0 (SDA10_0)		
				TIOB0_2		
				BIN0_2		
116	96	80	K12	P12	F	L
				AN02		
				SCK10_0 (SCL10_0)		
				TIOA1_2		
				ZIN0_2		
117	97	81	K14	P13	F	M
				AN03		
				SIN6_1		
				RX1_1		
				INT25_1		
118	98	82	K11	P14	F	L
				AN04		
				SOT6_1 (SDA6_1)		
				TX1_1		
119	-	-	-	PB8	E	O
				ADTG_6		
				SCS63_1		
				INT08_2		
				TRACED8		
120	-	-	-	PB9	E	O
				SIN9_1		
				AIN2_2		
				INT09_2		
				TRACED9		
121	-	-	-	PBA	E	N
				SOT9_1 (SDA9_1)		
				BIN2_2		
				TRACED10		

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
143	117	93	G9	P1F	F	M
				AN15		
				RTS5_0		
				TIOB8_1		
				INT27_1		
				MAD11_0		
144	118	94	F10	P2A	F	L
				AN24		
				CTS5_0		
				MAD12_0		
145	119	95	F11	P29	F	L
				AN25		
				SCK5_0 (SCL5_0)		
				MAD13_0		
146	120	96	F12	P28	F	L
				AN26		
				SOT5_0 (SDA5_0)		
				MAD14_0		
147	121	97	F13	P27	F	M
				AN27		
				SIN5_0		
				INT24_0		
				MAD15_0		
148	-	-	-	PBC	E	N
				TX1_2		
				TRACED12		
149	-	-	-	PBD	E	O
				SCK0_1 (SCL0_1)		
				RX1_2		
				AIN3_2		
				INT10_2		
				TRACED13		
150	-	-	-	PBE	E	N
				SOT0_1 (SDA0_1)		
				BIN3_2		
				TRACED14		
151	-	-	-	PBF	E	O
				SIN0_1		
				ZIN3_2		
				INT11_2		
				TRACED15		
152	122	98	E10	P26	E	I
				TX1_0		
				MAD16_0		
153	123	99	E11	P25	F	M
				AN28		
				RX1_0		
				INT25_0		
				MAD17_0		

Signal Descriptions

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel.

Use the extended port function register (EPFR) to select the pin.

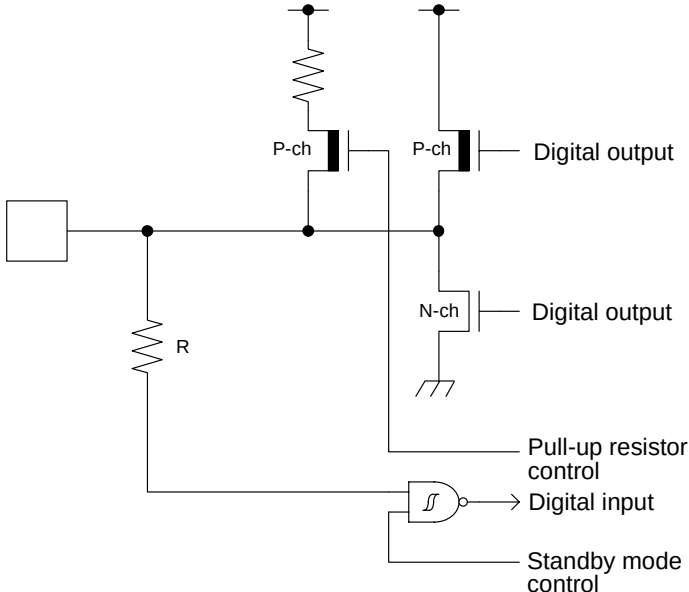
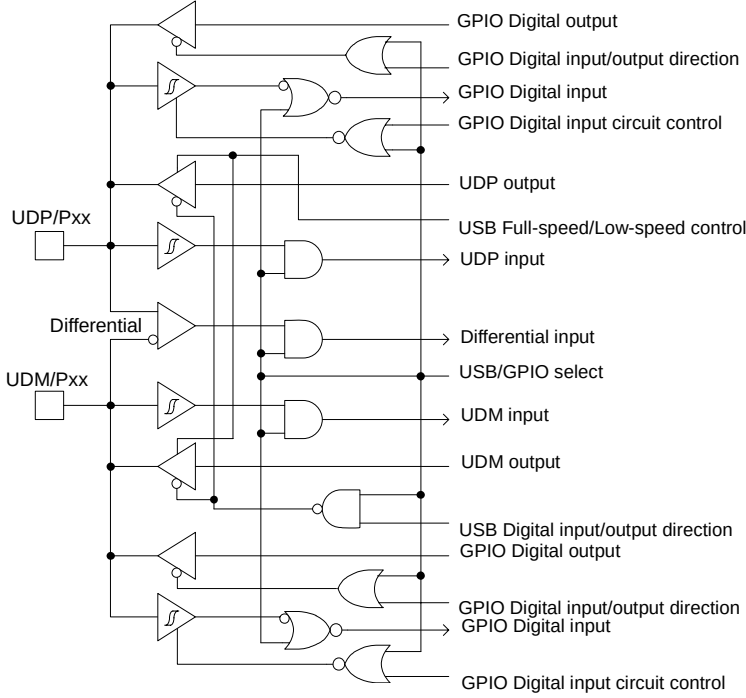
Module	Pin name	Function	Pin No			
			LQO 216	LQP 176	LQS 144	LBE 192
ADC	ADTG_0	A/D converter external trigger input pin	24	19	16	F6
	ADTG_1		32	23	20	G5
	ADTG_2		44	34	29	J3
	ADTG_3		209	169	137	C5
	ADTG_4		157	127	103	D13
	ADTG_5		198	166	136	D6
	ADTG_6		119	-	-	-
	ADTG_7		71	56	48	M5
	ADTG_8		80	65	55	L6
	AN00	A/D converter analog input pin. ANxx describes ADC ch.xx.	114	94	78	L11
	AN01		115	95	79	K13
	AN02		116	96	80	K12
	AN03		117	97	81	K14
	AN04		118	98	82	K11
	AN05		123	99	83	J13
	AN06		124	100	84	J12
	AN07		125	101	85	J11
	AN08		130	106	86	H9
	AN09		131	107	87	H12
	AN10		132	108	88	H14
	AN11		133	109	89	G14
	AN12		134	110	90	H13
	AN13		135	111	91	H11
	AN14		142	116	92	G10
	AN15		143	117	93	G9
	AN16		126	102	-	J10
	AN17		127	103	-	J9
	AN18		128	104	-	H10
	AN19		129	105	-	J14
	AN20		138	112	-	G13
	AN21		139	113	-	F14
	AN22		140	114	-	G12
	AN23		141	115	-	G11
	AN24		144	118	94	F10
	AN25		145	119	95	F11
	AN26		146	120	96	F12
	AN27		147	121	97	F13
	AN28		153	123	99	E11
	AN29		154	124	100	E12
	AN30		155	125	101	E13
	AN31		156	126	102	D12

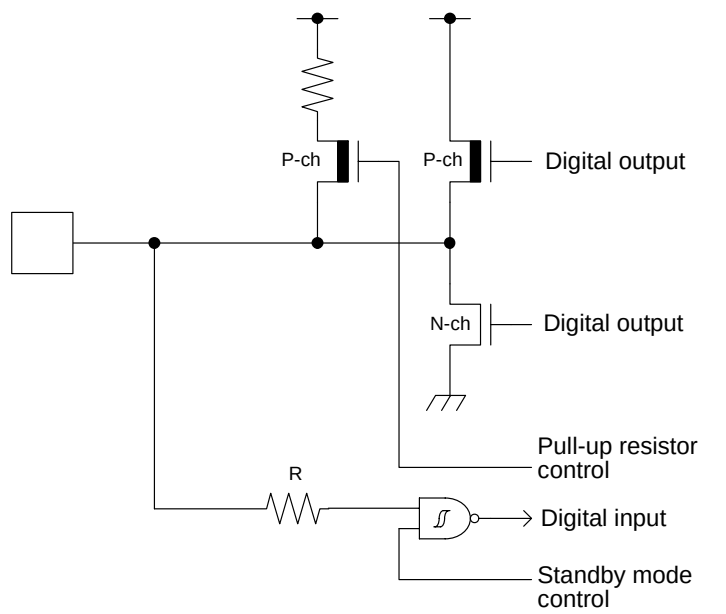
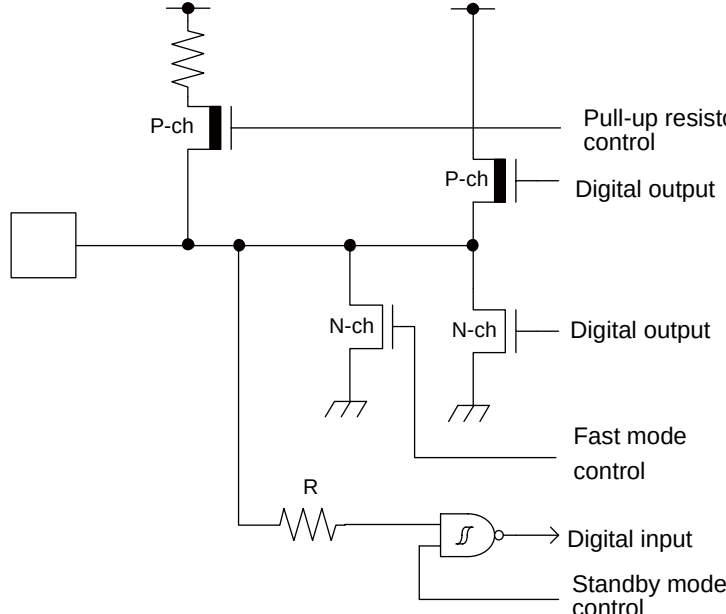
Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P70	General-purpose I/O port 7	80	65	55	L6
	P71		81	66	56	J6
	P72		82	67	57	L8
	P73		83	68	58	K8
	P74		84	69	59	J8
	P75		91	76	60	K9
	P76		92	77	61	P10
	P77		93	78	62	N10
	P78		96	79	63	L10
	P79		97	80	64	K10
	P7A		98	81	65	M10
	P7B		99	82	66	N11
	P7C		100	83	67	M11
	P7D		70	55	47	L5
	P7E		71	56	48	M5
	P80	General-purpose I/O port 8	214	174	142	A3
	P81		215	175	143	A2
	P82		160	130	106	D14
	P83		161	131	107	C14
	P90	General-purpose I/O port 9	169	139	-	C11
	P91		170	140	-	D11
	P92		171	141	-	B10
	P93		172	142	-	C10
	P94		173	143	-	D10
	P95		174	144	-	B9
	P96		175	-	-	-
	P97		176	-	-	-

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-function serial 7	SIN7_0	Multi-function serial interface ch.7 input pin	14	13	10	E5
	SIN7_1		103	-	-	-
	SOT7_0 (SDA7_0)	Multi-function serial interface ch.7 output pin.	15	14	11	F1
	SOT7_1 (SDA7_1)	This pin operates as SOT7 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA7 when it is used in an I ² C (operation mode 4).	102	-	-	-
	SCK7_0 (SCL7_0)	Multi-function serial interface ch.7 clock I/O pin.	16	15	12	F2
	SCK7_1 (SCL7_1)	This pin operates as SCK7 when it is used in a CSIO (operation modes 2) and as SCL7 when it is used in an I ² C (operation mode 4).	101	-	-	-
	SCS70_0	Multi-function serial interface ch.7 chip select 0 input/output pin	17	16	13	F3
	SCS70_1		94	-	-	-
	SCS71_0	Multi-function serial interface ch.7 chip select1 input/output pin	18	17	14	F4
	SCS71_1		95	-	-	-
	SCS72_0	Multi-function serial interface ch.7 chip select 2 input/output pin	10	10	-	E2
	SCS72_1		68	-	-	-
	SCS73_0	Multi-function serial interface ch.7 chip select 3 input/output pin	11	11	-	E3
	SCS73_1		69	-	-	-
Multi-function serial 8	SIN8_0	Multi-function serial interface ch.8 input pin	91	76	60	K9
	SIN8_1		138	112	-	G13
	SOT8_0 (SDA8_0)	Multi-function serial interface ch.8 output pin.	92	77	61	P10
	SOT8_1 (SDA8_1)	This pin operates as SOT8 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA8 when it is used in an I ² C (operation mode 4).	139	113	-	F14
	SCK8_0 (SCL8_0)	Multi-function serial interface ch.8 clock I/O pin.	93	78	62	N10
	SCK8_1 (SCL8_1)	This pin operates as SCK8 when it is used in a CSIO (operation modes 2) and as SCL8 when it is used in an I ² C (operation mode 4).	140	114	-	G12
Multi-function serial 9	SIN9_0	Multi-function serial interface ch.9 input pin	82	67	57	L8
	SIN9_1		120	-	-	-
	SOT9_0 (SDA9_0)	Multi-function serial interface ch.9 output pin.	83	68	58	K8
	SOT9_1 (SDA9_1)	This pin operates as SOT9 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA9 when it is used in an I ² C (operation mode 4).	121	-	-	-
	SCK9_0 (SCL9_0)	Multi-function serial interface ch.9 clock I/O pin.	84	69	59	J8
	SCK9_1 (SCL9_1)	This pin operates as SCK9 when it is used in a CSIO (operation modes 2) and as SCL9 when it is used in an I ² C (operation mode 4).	122	-	-	-

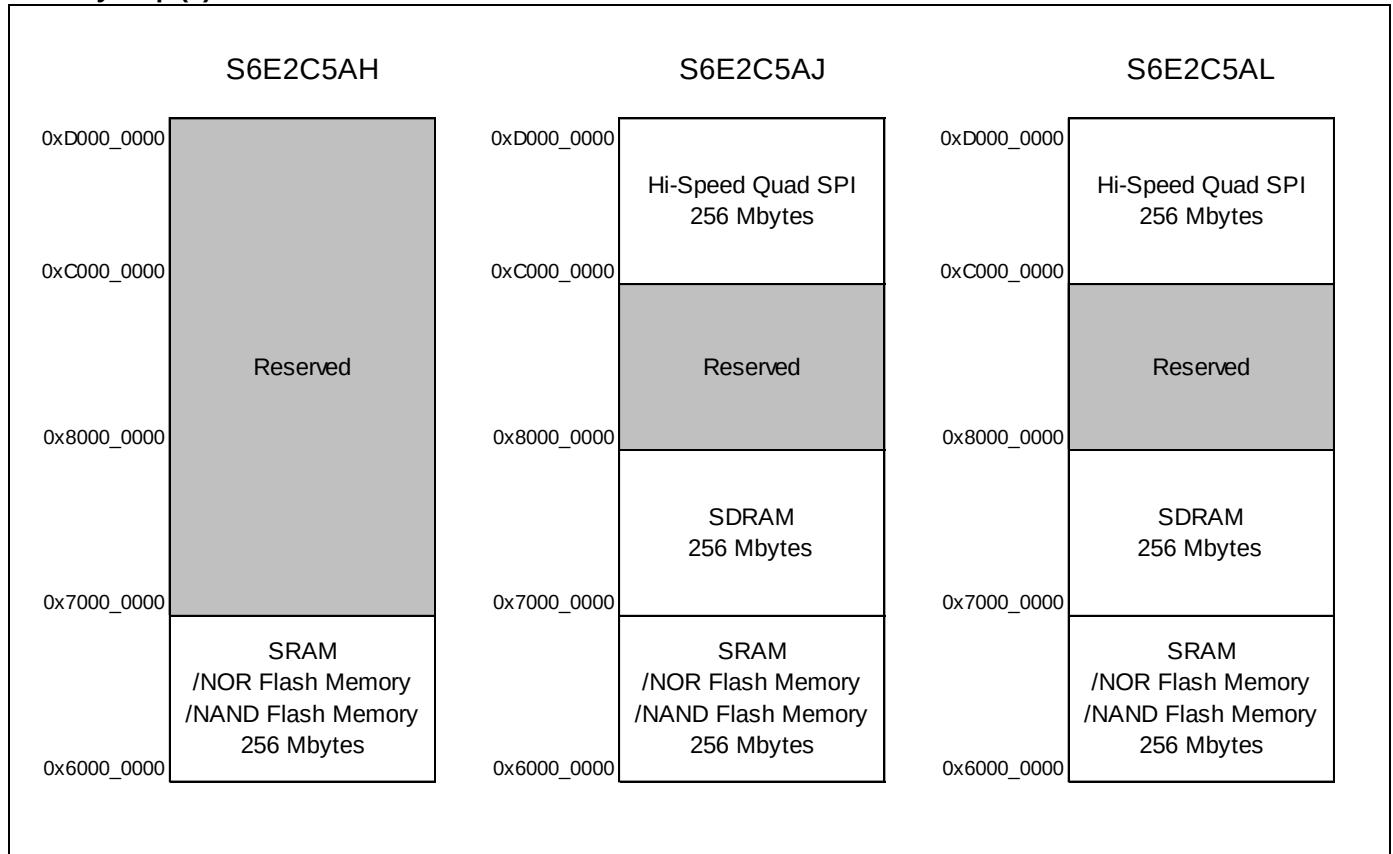
Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-function Timer 1	DTT1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of Multi-function timer 1.	70	55	47	L5
	DTT1X_1		94	-	-	-
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	71	56	48	M5
	FRCK1_1		78	63	-	K5
	IC10_0	16-bit input capture input pin of Multi-function timer 1. ICxx describes channel number.	96	79	63	L10
	IC10_1		95	-	-	-
	IC11_0		97	80	64	K10
	IC11_1		101	-	-	-
	IC12_0		98	81	65	M10
	IC12_1		102	-	-	-
	IC13_0		99	82	66	N11
	IC13_1		103	-	-	-
	RTO10_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1.	56	46	38	N2
	RTO10_1 (PPG10_1)	This pin operates as PPG10 when it is used in PPG1 output modes.	85	70	-	N8
	RTO11_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1.	57	47	39	N3
	RTO11_1 (PPG10_1)	This pin operates as PPG10 when it is used in PPG1 output modes.	86	71	-	M8
	RTO12_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1.	58	48	40	M3
	RTO12_1 (PPG12_1)	This pin operates as PPG12 when it is used in PPG1 output modes.	87	72	-	N9
	RTO13_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1.	59	49	41	L4
	RTO13_1 (PPG12_1)	This pin operates as PPG12 when it is used in PPG1 output modes.	88	73	-	P9
	RTO14_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1.	60	50	42	M4
	RTO14_1 (PPG14_1)	This pin operates as PPG14 when it is used in PPG1 output modes.	89	74	-	M9
	RTO15_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1.	61	51	43	N4
	RTO15_1 (PPG14_1)	This pin operates as PPG14 when it is used in PPG1 output modes.	90	75	-	L9

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Quadrature Position/ Revolution Counter 3	AIN3_0	QPRC ch.3 AIN input pin	18	17	14	F4
	AIN3_1		45	35	30	J2
	AIN3_2		149	-	-	-
	BIN3_0	QPRC ch.3 BIN input pin	23	18	15	F5
	BIN3_1		46	36	31	K1
	BIN3_2		150	-	-	-
	ZIN3_0	QPRC ch.3 ZIN input pin	24	19	16	F6
	ZIN3_1		47	37	32	K2
	ZIN3_2		151	-	-	-
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of Real-time clock	211	171	139	C4
	RTCCO_1		33	-	-	-
	SUBOUT_0	Sub clock output pin	211	171	139	C4
	SUBOUT_1		33	-	-	-
USB0	UDM0	USB ch.0 device/host D – pin	214	174	142	A3
	UDP0	USB ch.0 device/host D + pin	215	175	143	A2
	UHCONX0	USB ch.0 external pull-up control pin	211	171	139	C4
USB1	UDM1	USB ch.1 device/host D – pin	160	130	106	D14
	UDP1	USB ch.1 device/host D + pin	161	131	107	C14
	UHCONX1	USB ch.1 external pull-up control pin	155	125	101	E13
Low-Power Consumption Mode	WKUP0	Deep standby mode return signal input pin 0	158	128	104	C13
	WKUP1	Deep standby mode return signal input pin 1	14	13	10	E5
	WKUP2	Deep standby mode return signal input pin 2	70	55	47	L5
	WKUP3	Deep standby mode return signal input pin 3	212	172	140	B3
DAC	DA0	D/A converter ch.0 analog output pin	100	83	67	M11
	DA1	D/A converter ch.1 analog output pin	99	82	66	N11
VBAT	VREGCTL	On-board regulator control pin	76	61	53	N6
	VWAKEUP	The return signal input pin from a hibernation state	77	62	54	M6

Type	Circuit	Remarks
G	 P-ch Digital output P-ch Digital output N-ch Digital output R Pull-up resistor control Digital input Standby mode control	• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -12 \text{ mA}$, $I_{OL} = 12 \text{ mA}$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off.
H	 GPIO Digital output GPIO Digital input/output direction GPIO Digital input GPIO Digital input circuit control UDP output USB Full-speed/Low-speed control UDP input Differential input USB/GPIO select UDM input UDM output USB Digital input/output direction GPIO Digital output GPIO Digital input/output direction GPIO Digital input GPIO Digital input circuit control UDP/Pxx Differential UDM/Pxx	It is possible to select either USB I/O or GPIO function. When the USB I/O is selected: • Full-speed, low-speed control When the GPIO is selected: • CMOS level output • CMOS level hysteresis input • Standby mode control • $I_{OH} = -20.5 \text{ mA}$, $I_{OL} = 18.5 \text{ mA}$

Type	Circuit	Remarks
L	 P-ch Digital output N-ch Digital output Pull-up resistor control Digital input Standby mode control	• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -8 \text{ mA}$, $I_{OL} = 8 \text{ mA}$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off.
N	 P-ch Pull-up resistor control Digital output N-ch Digital output Fast mode control Digital input Standby mode control	• CMOS level output • CMOS level hysteresis input • 5V tolerant • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ (GPIO) • $I_{OL} = 20 \text{ mA}$ (Fast mode Plus) • Available to control of PZR register (pseudo-open drain control) • For PZR registers, refer to GPIO in the "FM4 Family Peripheral Manual Main Part (002-04856)". • When this pin is used as an I²C pin, the digital output P-ch transistor is always off.

Memory Map (3)



List of VBAT Domain Pin Status

VBAT Pin Status Type	Function Group	Power-on reset*1	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer Mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return From Deep Standby Mode State	VBAT RTC Mode State	Return From VBAT RTC Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	Power Supply Stable	Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	-	-
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	-	-
S	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	Sub crystal oscillator input pin/ external sub clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Maintain previous state	Maintain previous state
T	GPIO selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Setting prohibition	-
	External sub clock input selected	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	Sub crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state/ When oscillation stops, Hi-Z*2	Maintain previous state	Maintain previous state	Maintain previous state
U	Resource selected	Hi-Z	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state
	GPIO selected		Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state	Maintain previous state

*1: When VBAT and VCC power on.

*2: When the SOSCNTL bit in the WTOSCCNT register is 0, the sub crystal oscillator output pin is maintained in the previous state. When the SOSCNTL bit in the WTOSCCNT register is 1, oscillation is stopped at Stop mode and Deep Standby Stop mode

12.4.12 CSIO (SPI) Timing

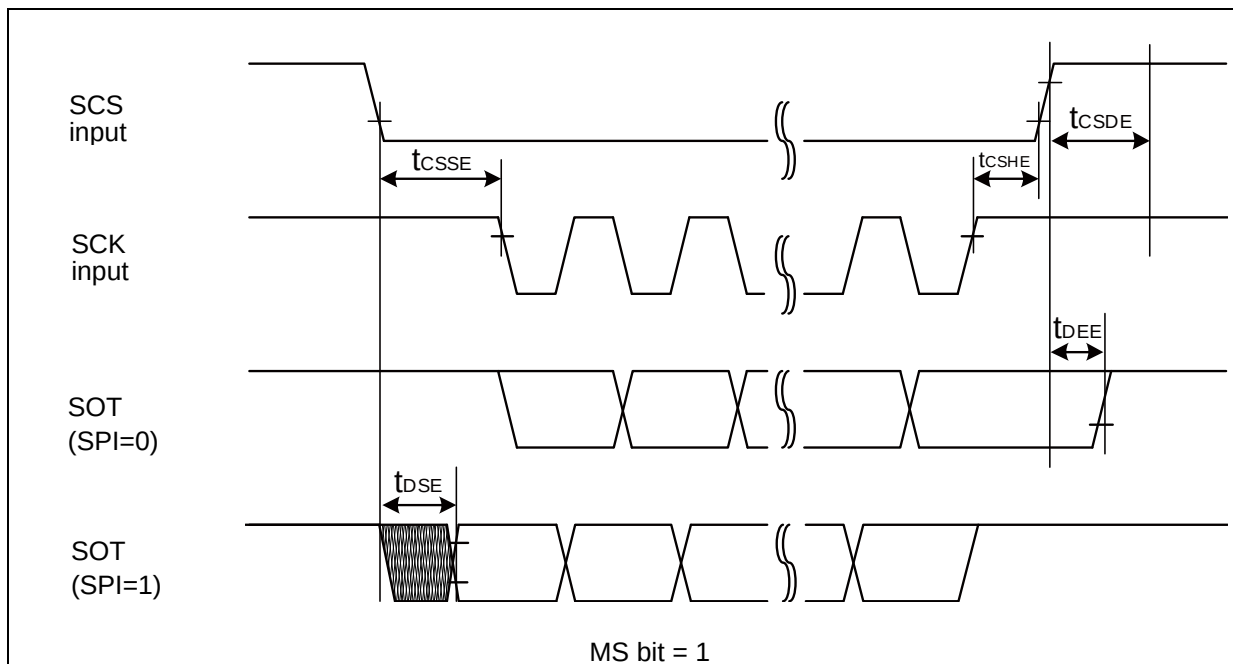
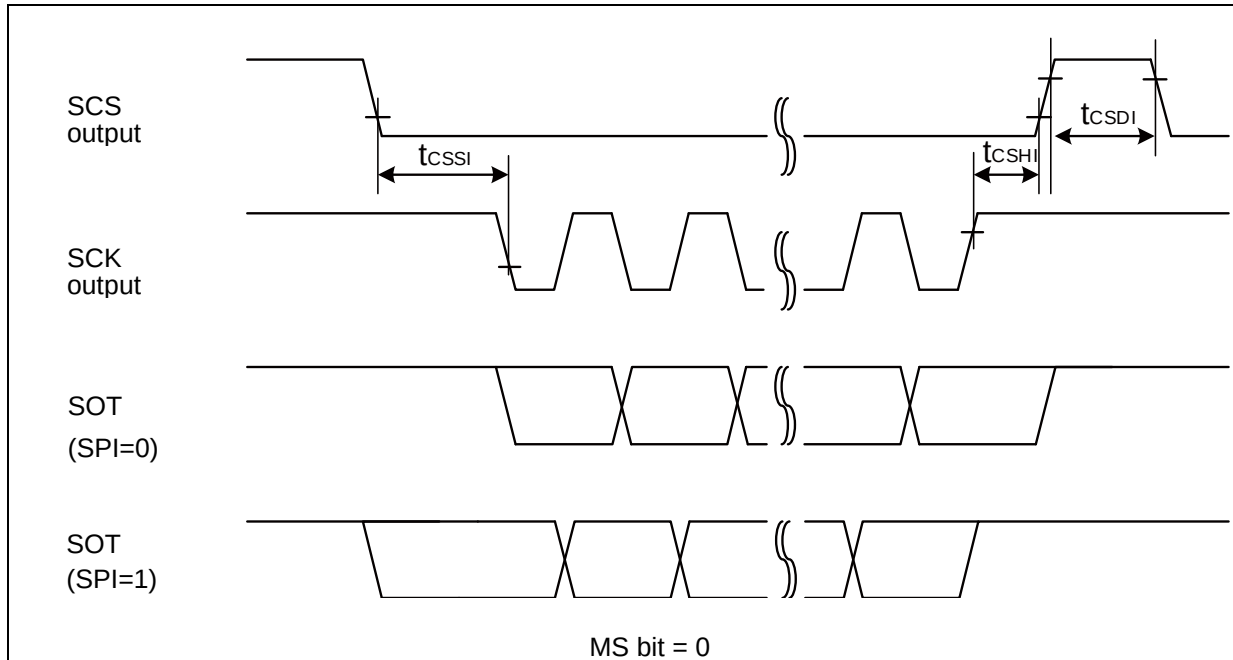
Synchronous serial (SPI = 0, SCINV = 0)

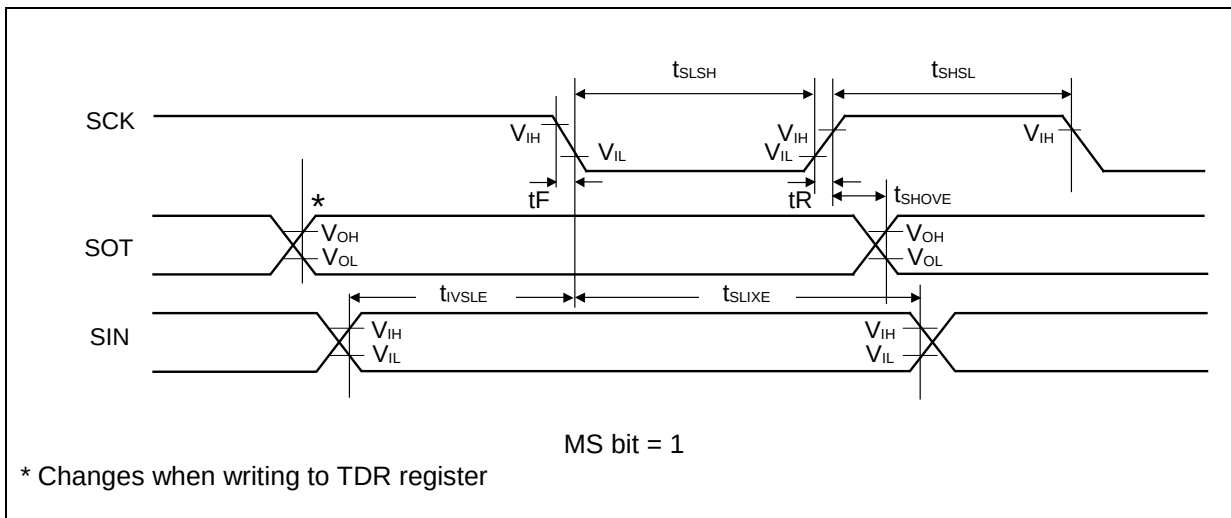
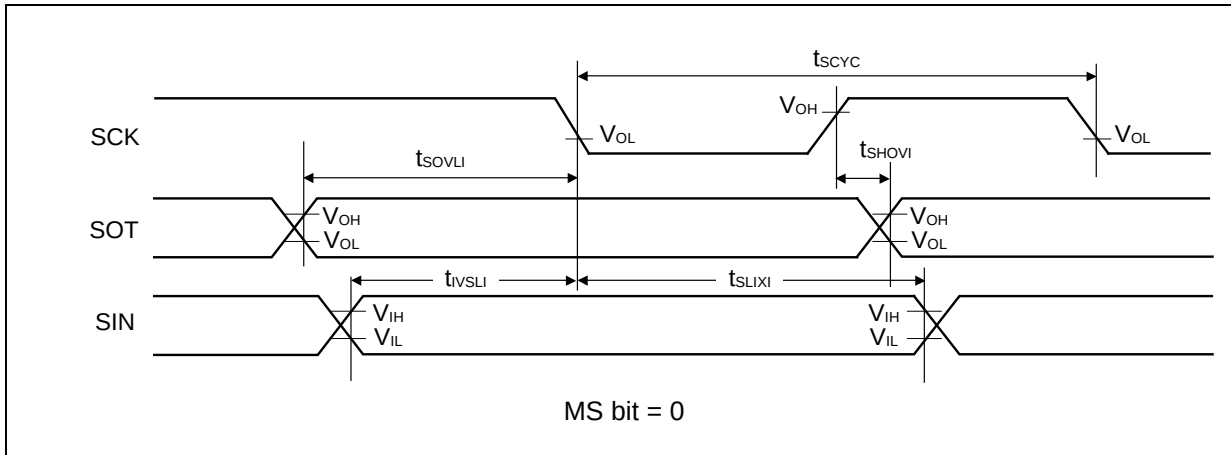
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-		-	8	-	8	Mbps
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↓→SOT delay time	t _{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t _{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t _{SHIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t _{SLSH}	SCKx		2t _{CYCP} - 10	-	2t _{CYCP} - 10	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx	External shift clock operation	t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↓→SOT delay time	t _{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t _{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t _{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.





When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t _{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t _{CShI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t _{CSDI}		(*3)-20 +5t _{CYCP}	(*3)+20 +5t _{CYCP}	(*3)-20 +5t _{CYCP}	(*3)+20 +5t _{CYCP}	ns
SCS↑→SCK↑ setup time	t _{CSSE}	External shift clock operation	3t _{CYCP} +15	-	3t _{CYCP} +15	-	ns
SCK↓→SCS↓ hold time	t _{CSHE}		0	-	0	-	ns
SCS deselect time	t _{CSDE}		3t _{CYCP} +15	-	3t _{CYCP} +15	-	ns
SCS↑→SOT delay time	t _{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t _{DEE}		0	-	0	-	ns

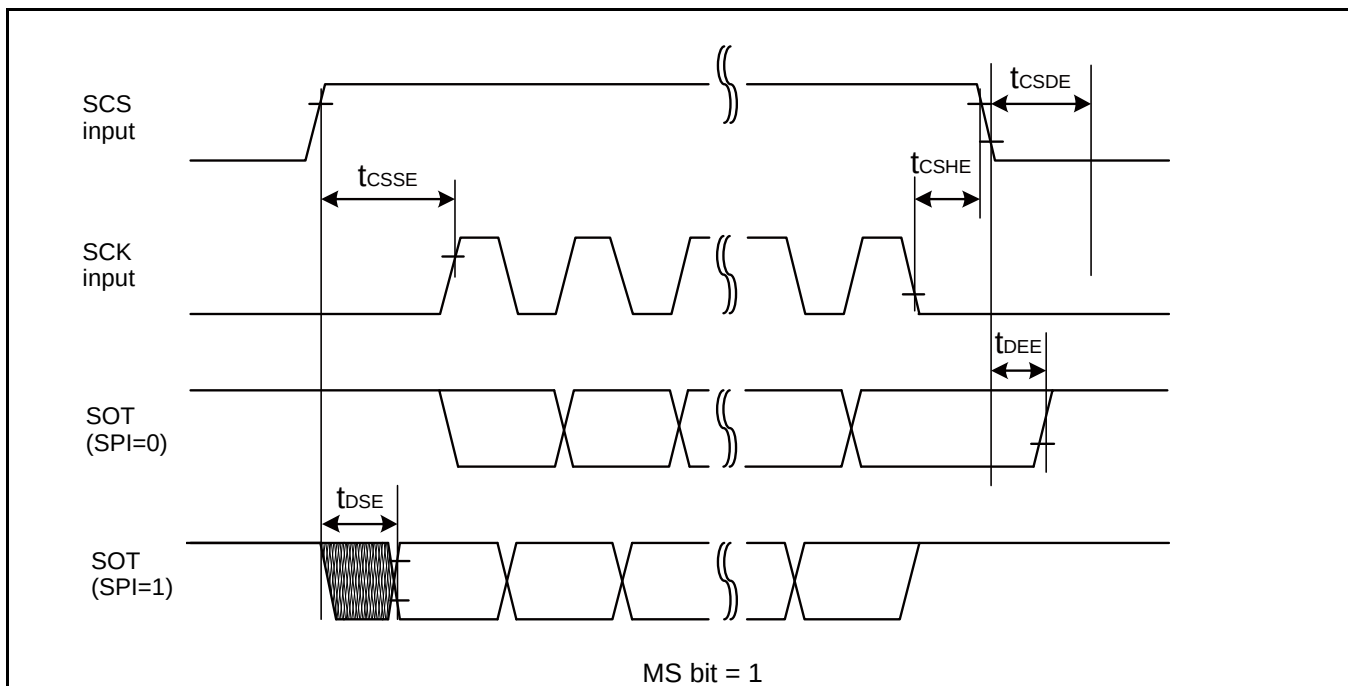
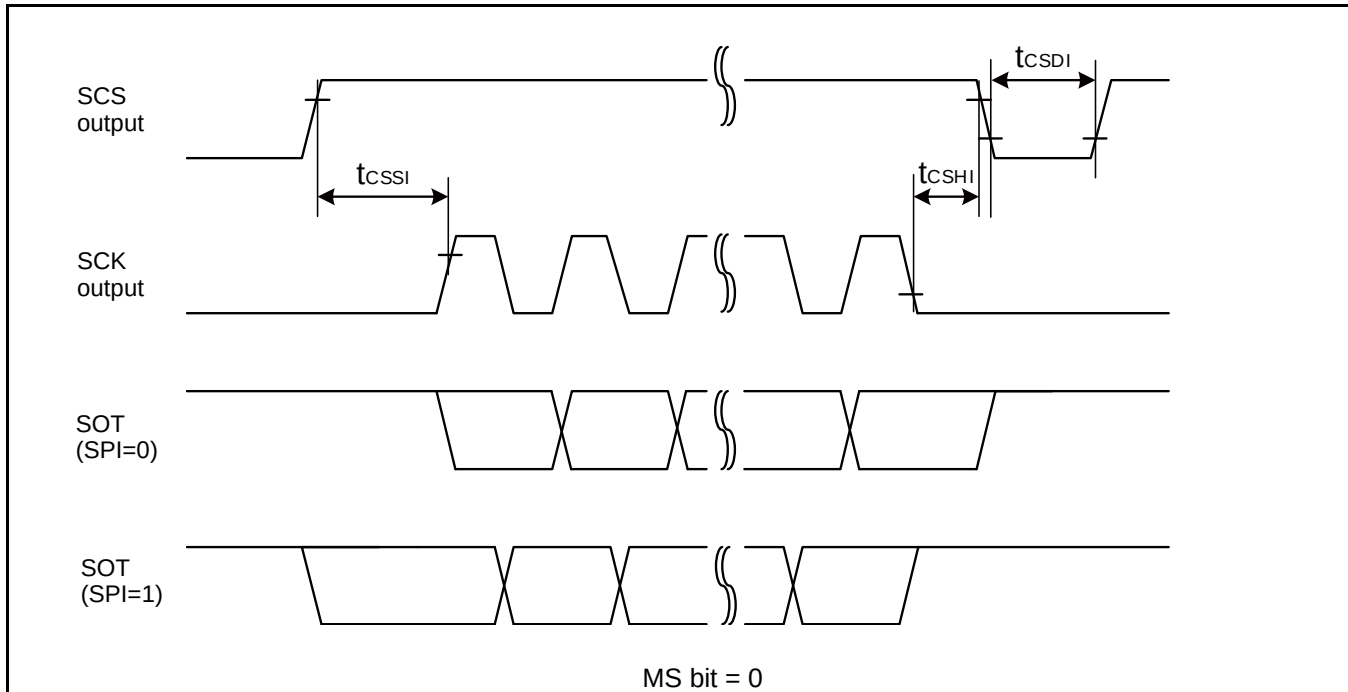
(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

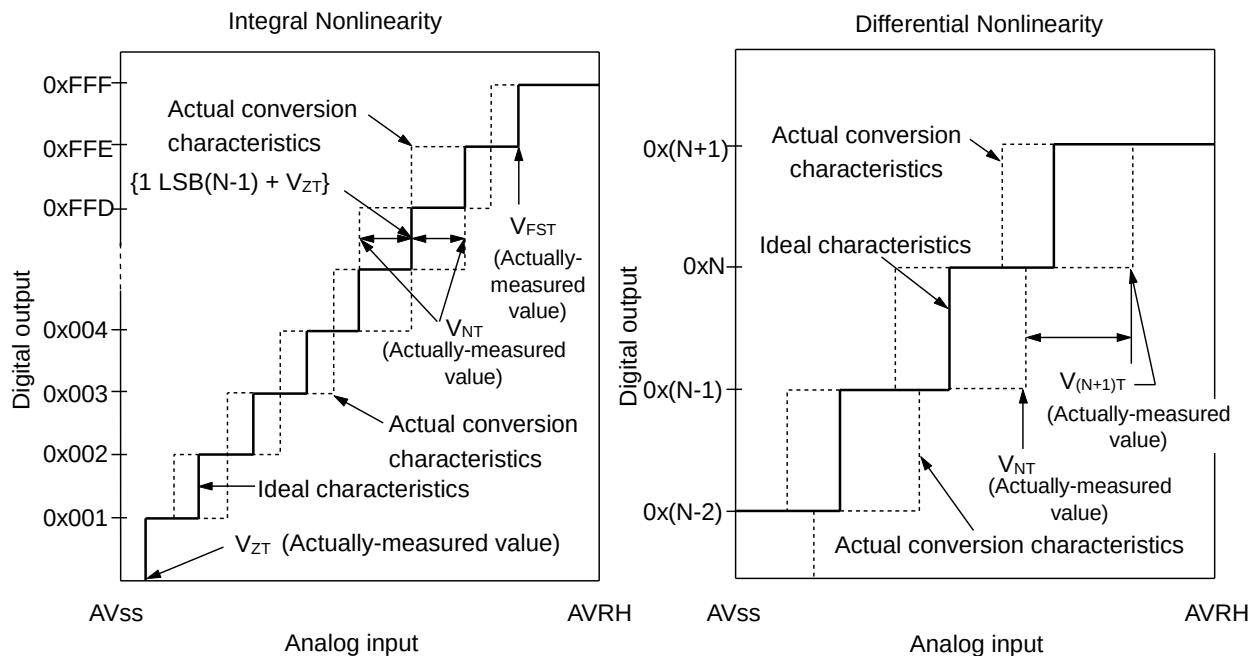
Notes:

- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C_L = 30 pF.



Definition of 12-bit A/D Converter Terms

- **Resolution:** Analog variation that is recognized by an A/D converter.
- **Integral Nonlinearity:** Deviation of the line between the zero-transition point (0b000000000000 ↔ 0b000000000001) and the full-scale transition point (0b111111111110 ↔ 0b111111111111) from the actual conversion characteristics.
- **Differential Nonlinearity:** Deviation from the ideal value of the input voltage that is required to change the output code by 1 LSB.



$$\text{Integral Nonlinearity of digital output } N = \frac{V_{NT} - \{1\text{LSB} \times (N - 1) + V_{ZT}\}}{1\text{LSB}} \text{ [LSB]}$$

$$\text{Differential Nonlinearity of digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1\text{LSB}} - 1 \text{ [LSB]}$$

$$1\text{LSB} = \frac{V_{FST} - V_{ZT}}{4094}$$

- N: A/D converter digital output value.
- V_{ZT} : Voltage at which the digital output changes from 0x000 to 0x001.
- V_{FST} : Voltage at which the digital output changes from 0xFFE to 0xFFFF.
- V_{NT} : Voltage at which the digital output changes from 0x(N - 1) to 0xN.

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