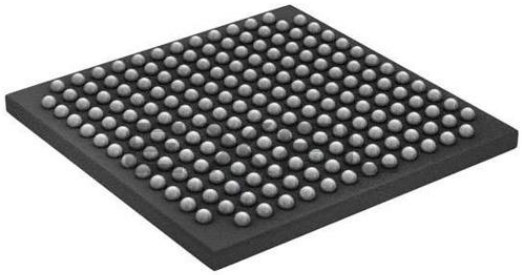
Infineon Technologies - S6E2C5AJ0AGB1000A Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	192-LFBGA
Supplier Device Package	192-FBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c5aj0agb1000a

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
122	-	-	-	PBB SCK9_1 (SCL9_1) ZIN2_2 TRACED11	E	N
123	99	83	J13	P15 AN05 SIN11_0 TIOB1_2 AIN1_2 INT09_0	F	M
124	100	84	J12	P16 AN06 SOT11_0 (SDA11_0) TIOA2_2 BIN1_2	F	L
125	101	85	J11	P17 AN07 SCK11_0 (SCL11_0) TIOB2_2 ZIN1_2	F	L
126	102	-	J10	PB0 AN16 SCK6_1 (SCL6_1) TIOA9_1	F	L
127	103	-	J9	PB1 AN17 SCS60_1 TIOB9_1 INT08_1	F	M
128	104	-	H10	PB2 AN18 SCS61_1 TIOA10_1 INT09_1	F	M
129	105	-	J14	PB3 AN19 SCS62_1 TIOB10_1	F	L
130	106	86	H9	P18 AN08 SIN2_0 TIOA3_2 INT10_0	F	M
131	107	87	H12	P19 AN09 SOT2_0 (SDA2_0) TIOB3_2 INT24_1 TRACECLK	F	O

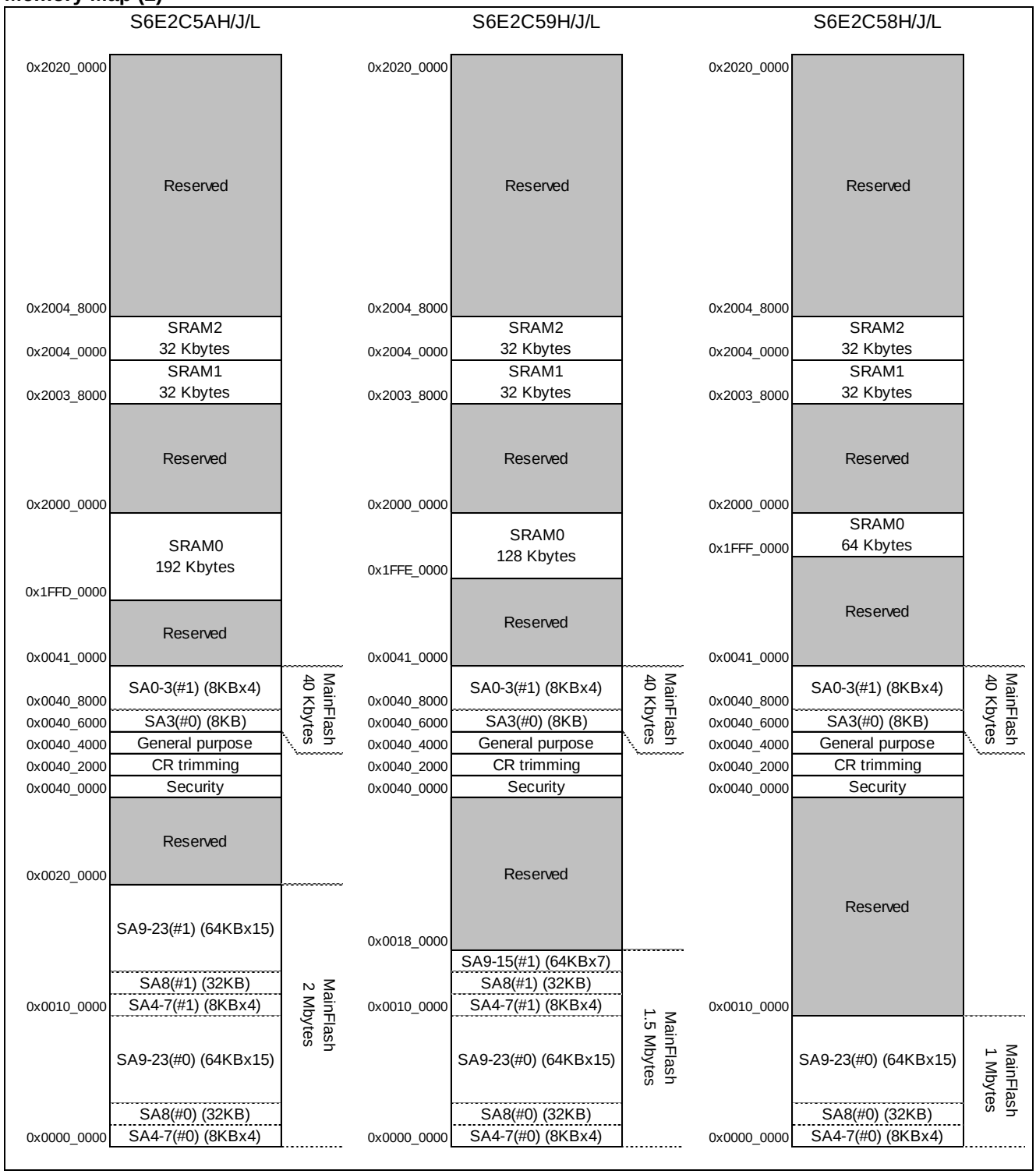
Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
External Interrupt	INT06_0	External interrupt request 06 input pin	80	65	55	L6
	INT06_1		87	72	-	N9
	INT06_2		103	-	-	-
	INT07_0	External interrupt request 07 input pin	82	67	57	L8
	INT07_1		88	73	-	P9
	INT07_2		102	-	-	-
	INT08_0	External interrupt request 08 input pin	114	94	78	L11
	INT08_1		127	103	-	J9
	INT08_2		119	-	-	-
	INT09_0	External interrupt request 09 input pin	123	99	83	J13
	INT09_1		128	104	-	H10
	INT09_2		120	-	-	-
	INT10_0	External interrupt request 10 input pin	130	106	86	H9
	INT10_1		138	112	-	G13
	INT10_2		149	-	-	-
	INT11_0	External interrupt request 11 input pin	133	109	89	G14
	INT11_1		139	113	-	F14
	INT11_2		151	-	-	-
	INT12_0	External interrupt request 12 input pin	194	162	132	E7
	INT12_1		169	139	-	C11
	INT12_2		175	-	-	-
	INT13_0	External interrupt request 13 input pin	184	152	122	E8
	INT13_1		170	140	-	D11
	INT13_2		176	-	-	-
	INT14_0	External interrupt request 14 input pin	192	160	130	A6
	INT14_1		171	141	-	B10
	INT14_2		201	-	-	-
	INT15_0	External interrupt request 15 input pin	193	161	131	D7
	INT15_1		172	142	-	C10
	INT15_2		206	-	-	-
	INT16_0	External interrupt request 16 input pin	25	20	17	G2
	INT16_1		45	35	30	J2
	INT17_0	External interrupt request 17 input pin	30	21	18	G3
	INT17_1		46	36	31	K1
	INT18_0	External interrupt request 18 input pin	31	22	19	G4
	INT18_1		47	37	32	K2
	INT19_0	External interrupt request 19 input pin	36	26	21	H2
	INT19_1		48	38	33	K3
	INT20_0	External interrupt request 20 input pin	91	76	60	K9

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	PA0	General-purpose I/O port A	2	2	2	B2
	PA1		3	3	3	C2
	PA2		4	4	4	C3
	PA3		5	5	5	D5
	PA4		6	6	6	D2
	PA5		7	7	7	D1
	PA6		8	8	8	D3
	PA7		9	9	9	D4
	PA8		14	13	10	E5
	PA9		15	14	11	F1
	PAA		16	15	12	F2
	PAB		17	16	13	F3
	PAC		18	17	14	F4
	PAD		23	18	15	F5
	PAE		24	19	16	F6
	PAF		25	20	17	G2
	PB0	General-purpose I/O port B	126	102	-	J10
	PB1		127	103	-	J9
	PB2		128	104	-	H10
	PB3		129	105	-	J14
	PB4		138	112	-	G13
	PB5		139	113	-	F14
	PB6		140	114	-	G12
	PB7		141	115	-	G11
	PB8		119	-	-	-
	PB9		120	-	-	-
	PBA		121	-	-	-
	PBB		122	-	-	-
	PBC		148	-	-	-
	PBD		149	-	-	-
	PBE		150	-	-	-
	PBF		151	-	-	-

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-function serial 0	SIN0_0	Multi-function serial interface ch.0 input pin	157	127	103	D13
	SIN0_1		151	-	-	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch.0 output pin This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I^2C (operation mode 4).	156	126	102	D12
	SOT0_1 (SDA0_1)		150	-	-	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch.0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I^2C (operation mode 4)	155	125	101	E13
	SCK0_1 (SCL0_1)		149	-	-	-
Multi-function serial 1	SIN1_0	Multi-function serial interface ch.1 input pin	7	7	7	D1
	SIN1_1		80	65	55	L6
	SOT1_0 (SDA1_0)	Multi-function serial interface ch.1 output pin This pin operates as SOT1 when it is used in a UART/CSIO/LIN(operation modes 0 to 3) and as SDA1 when it is used in an I^2C (operation mode 4).	8	8	8	D3
	SOT1_1 (SDA1_1)		81	66	56	J6
	SCK1_0 (SCL1_0)	Multi-function serial interface ch.1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation modes 2) and as SCL1 when it is used in an I^2C (operation mode 4).	9	9	9	D4
	SCK1_1 (SCL1_1)		70	55	47	L5
Multi-function serial 2	SIN2_0	Multi-function serial interface ch.2 input pin	130	106	86	H9
	SIN2_1		45	35	30	J2
	SOT2_0 (SDA2_0)	Multi-function serial interface ch.2 output pin This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I^2C (operation mode 4).	131	107	87	H12
	SOT2_1 (SDA2_1)		46	36	31	K1
	SCK2_0 (SCL2_0)	Multi-function serial interface ch.2 clock I/O Pin. This pin operates as SCK2 when it is used in a CSIO (operation modes 2) and as SCL2 when it is used in an I^2C (operation mode 4).	132	108	88	H14
	SCK2_1 (SCL2_1)		47	37	32	K2

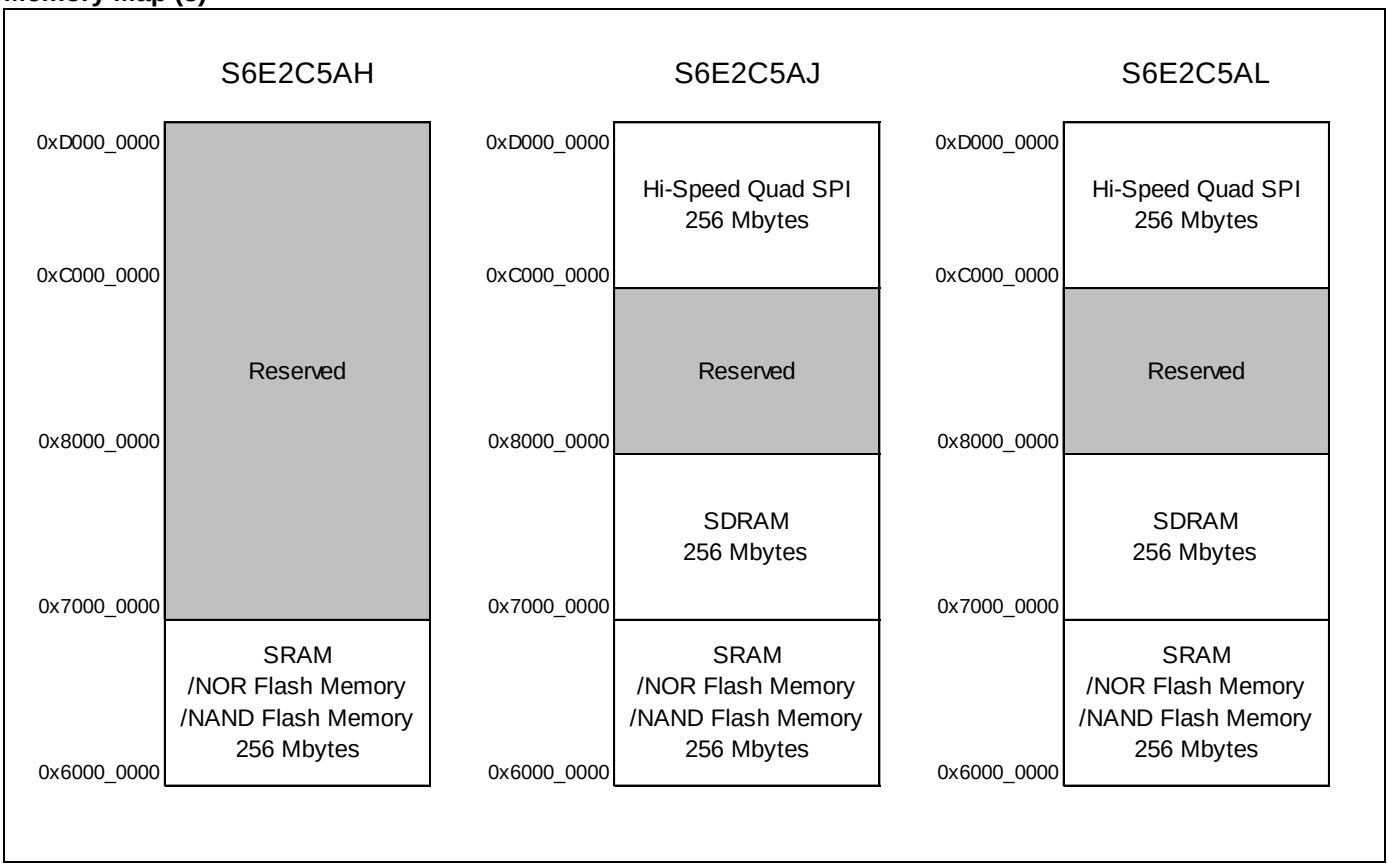
Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Mode	MD1	Mode 1 pin. During serial programming to Flash memory, MD1=L must be input.	104	84	68	N13
	MD0	Mode 0 pin. During normal operation, MD0=L must be input. During serial programming to Flash memory, MD0=H must be input.	105	85	69	N12
Power	VCC	Power supply Pin	1	1	1	C1
			39	29	24	H1
			55	45	37	N1
			64	54	46	P4
			109	89	73	M14
			137	-	-	-
			163	133	109	A13
			188	156	126	A9
	USBVCC0	3.3V Power supply port for USB I/O	213	173	141	A4
	USBVCC1		159	129	105	E14
GND	VSS	GND Pin	40	30	25	H5
			54	44	36	M1
			63	53	45	P3
			108	88	72	N14
			136	-	-	-
			162	132	108	B14
			189	157	127	A8
			216	176	144	B1
			-	-	-	E1
			-	-	-	G1
			-	-	-	P7
			-	-	-	P11
			-	-	-	L14
			-	-	-	A11
			-	-	-	A5
			-	-	-	N7
			-	-	-	M7
			-	-	-	K7
			-	-	-	J7
			-	-	-	G7
			-	-	-	H7
			-	-	-	H8
			-	-	-	G8

Memory Map (2)



* See S6E2CC/S6E2C5/S6E2C4/S6E2C3/S6E2C2/S6E2C1 Series Flash Programming Manual to confirm the detail of flash Memory.

Memory Map (3)


S6E2C5AH
0xD000_0000
0xC000_0000
0x8000_0000
0x7000_0000
0x6000_0000
Reserved
SRAM
/NOR Flash Memory
/NAND Flash Memory
256 Mbytes
S6E2C5AJ
0xD000_0000
0xC000_0000
0x8000_0000
0x7000_0000
0x6000_0000
Hi-Speed Quad SPI
256 Mbytes
Reserved
SDRAM
256 Mbytes
SRAM
/NOR Flash Memory
/NAND Flash Memory
256 Mbytes
S6E2C5AL
0xD000_0000
0xC000_0000
0x8000_0000
0x7000_0000
0x6000_0000
Hi-Speed Quad SPI
256 Mbytes
Reserved
SDRAM
256 Mbytes
SRAM
/NOR Flash Memory
/NAND Flash Memory
256 Mbytes

Start Address	End Address	Bus	Peripherals
0x4004_0000	0x4004_FFFF	AHB	USB ch 0
0x4005_0000	0x4005_FFFF		USB ch 1
0x4006_0000	0x4006_0FFF		DMAC register
0x4006_1000	0x4006_1FFF		DSTC register
0x4006_2000	0x4006_2FFF		CAN ch 0
0x4006_3000	0x4006_3FFF		CAN ch 1
0x4006_4000	0x4006_BFFF		Reserved
0x4006_C000	0x4006_CFFF		I^2S
0x4006_D000	0x4006_DFFF		Reserved
0x4006_E000	0x4006_EFFF		SD card I/F
0x4006_F000	0x4006_FFFF		GPIO
0x4007_0000	0x4007_FFFF		CAN-FD (CAN ch 2)
0x4008_0000	0x4008_0FFF		Programmable-CRC
0x4008_1000	0x41FF_FFFF		Reserved
0x200E_0000	0x200E_FFFF		Workflash I/F register
0xD000_0000	0xDFFF_FFFF		High-speed quad SPI control register

Current Explanation Diagram

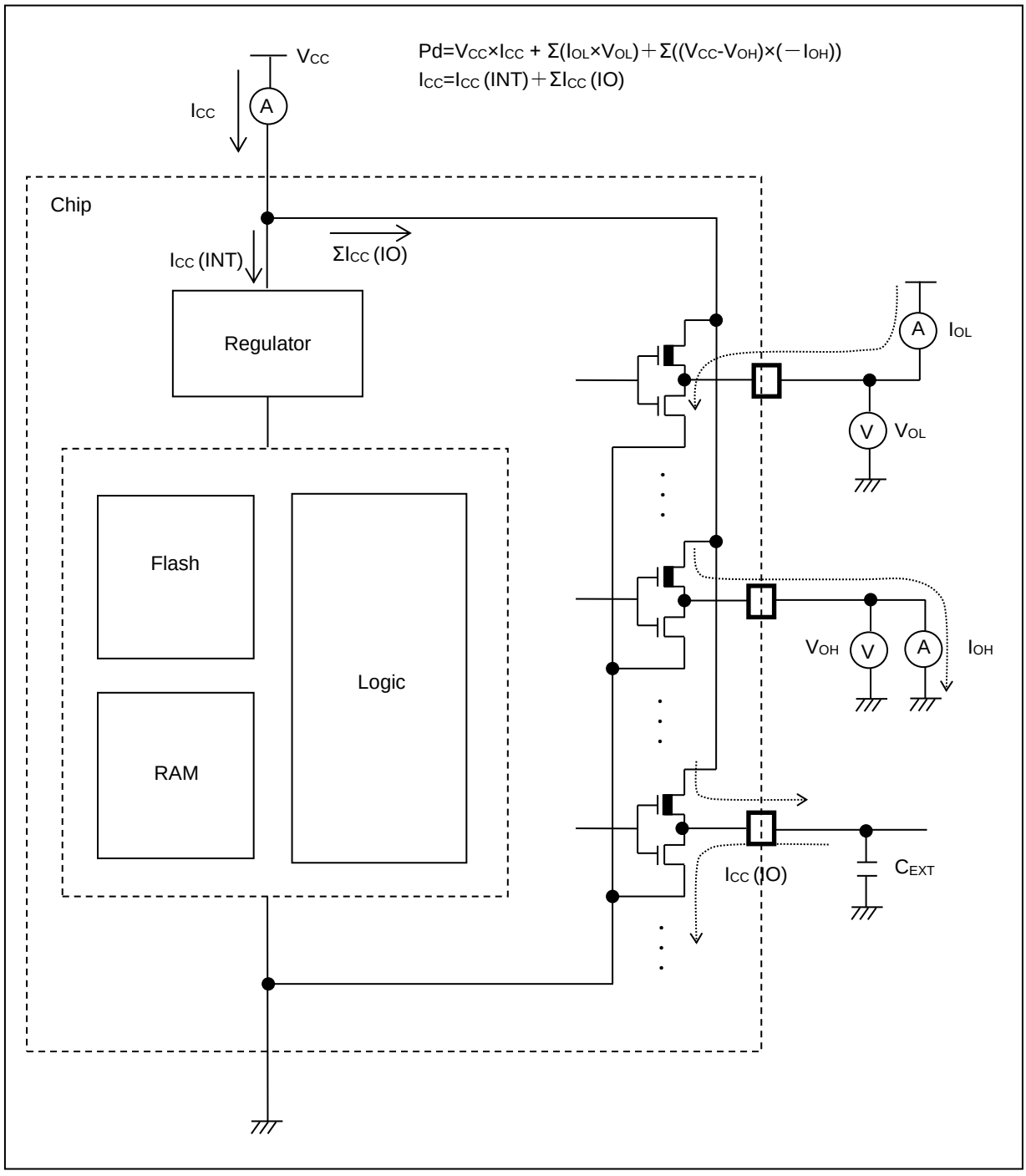


Table 12-5 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation*5 (PLL)	200 MHz	88	188	mA	*3 When all peripheral clocks are on
				192 MHz	85	184	mA	
				180 MHz	80	178	mA	
				160 MHz	72	164	mA	
				144 MHz	65	156	mA	
				120 MHz	55	144	mA	
				100 MHz	47	134	mA	
				80 MHz	38	124	mA	
				60 MHz	30	114	mA	
				40 MHz	21	104	mA	
				20 MHz	12	93	mA	
				8 MHz	7.4	87.2	mA	
				4 MHz	5.8	85.2	mA	
				200 MHz	44	134	mA	*3 When all peripheral clocks are off
				192 MHz	42	132	mA	
				180 MHz	40	129	mA	
				160 MHz	36	123	mA	
				144 MHz	33	119	mA	
				120 MHz	28	113	mA	
				100 MHz	24	108	mA	
				80 MHz	20	103	mA	
				60 MHz	16	98	mA	
				40 MHz	12	93	mA	
				20 MHz	7.6	87.6	mA	
				8 MHz	5.2	84.7	mA	
				4 MHz	4.4	83.7	mA	

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

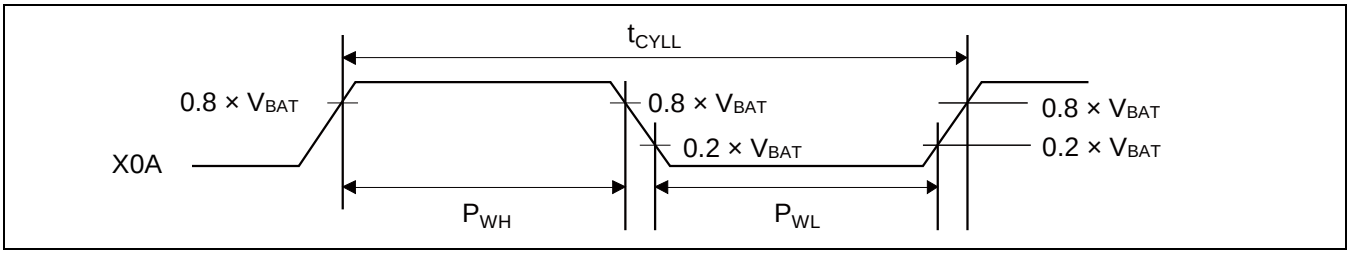
*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

12.4.2 Sub Clock Input Characteristics

(V_{BAT} = 1.65V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input frequency	$1/t_{CYLL}$	X0A, X1A	-	-	32.768	-	kHz	When crystal oscillator is connected *
			-	32	-	100	kHz	When using external clock
Input clock cycle	t_{CYLL}		-	10	-	31.25	µs	When using external clock
Input clock pulse width	-		P_{WH}/t_{CYLL}, P_{WL}/t_{CYLL}	45	-	55	%	When using external clock

*: For more information about crystal oscillator, see Sub crystal oscillator in 7. Handling Devices.



12.4.3 Built-In CR Oscillation Characteristics

Built-In High-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRH}	T_J = - 20°C to + 105°C	3.92	4	4.08	MHz	When trimming *1
		T_J = - 40°C to + 125°C	3.88	4	4.12		
		T_J = - 40°C to + 125°C	3	4	5		When not trimming
Frequency stabilization time	t_{CRWT}	-	-	-	30	µs	*2

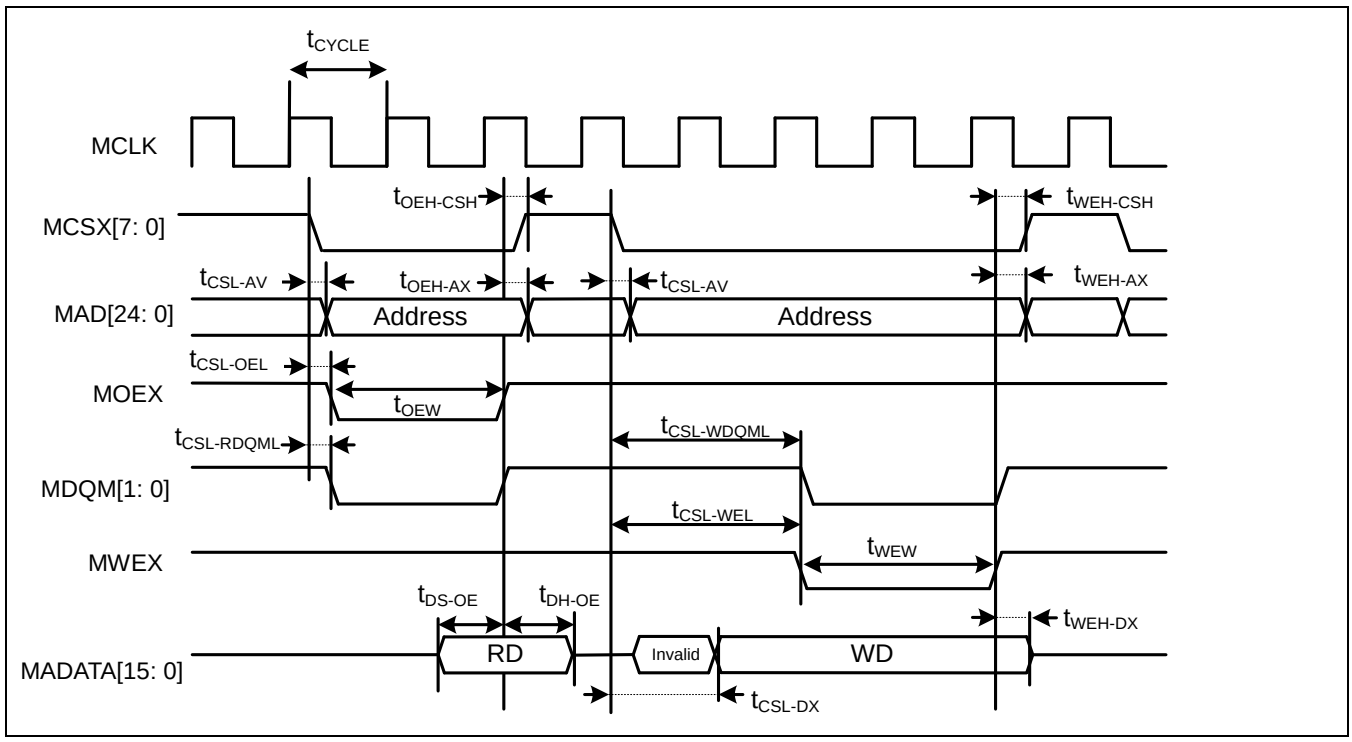
*1: In the case of using the values in CR trimming area of flash memory at shipment for frequency/temperature trimming

*2: This is the time to stabilize the frequency of the High-speed CR clock after setting trimming value. During this period, it is able to use the High-speed CR clock as a source clock.

Built-In Low-speed CR

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Condition	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_{CRL}	-	50	100	150	kHz	

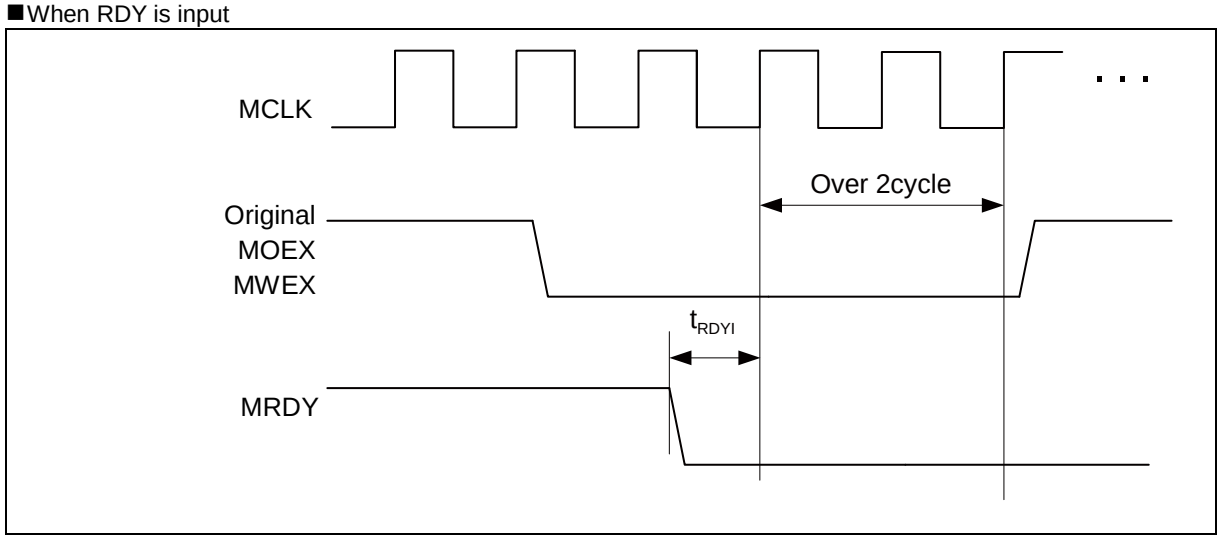

tCYCLE
MCLK
MCSX[7: 0]
tOEH-CSH
tWEH-CSH
MAD[24: 0]
tCSL-AV
tOEH-AX
tCSL-AV
tWEH-AX
Address
Address
MOEX
tCSL-OEL
tOEW
MDQM[1: 0]
tCSL-RDQML
tCSL-WDQML
MWEX
tCSL-WEL
tWEW
MADATA[15: 0]
tDS-OE
tDH-OE
tWEH-DX
RD
Invalid
WD
tCSL-DX

External Ready Input Timing

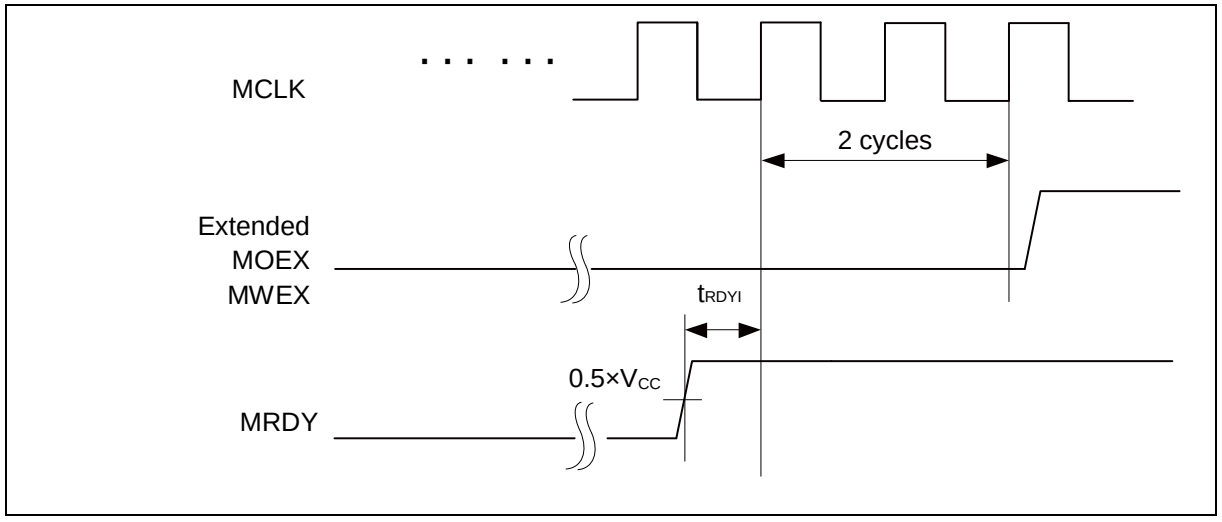
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
MCLK↑ MRDY input setup time	t_{RDYI}	MCLK, MRDY	-	19	-	ns	

■When RDY is input



■When RDY is released



Synchronous Serial (SPI = 0, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*

High-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1 card)	0	50	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rise time	t_{TLH}	S_CLK		-	3	ns
Clock fall time	t_{THL}	S_CLK		-	3	ns

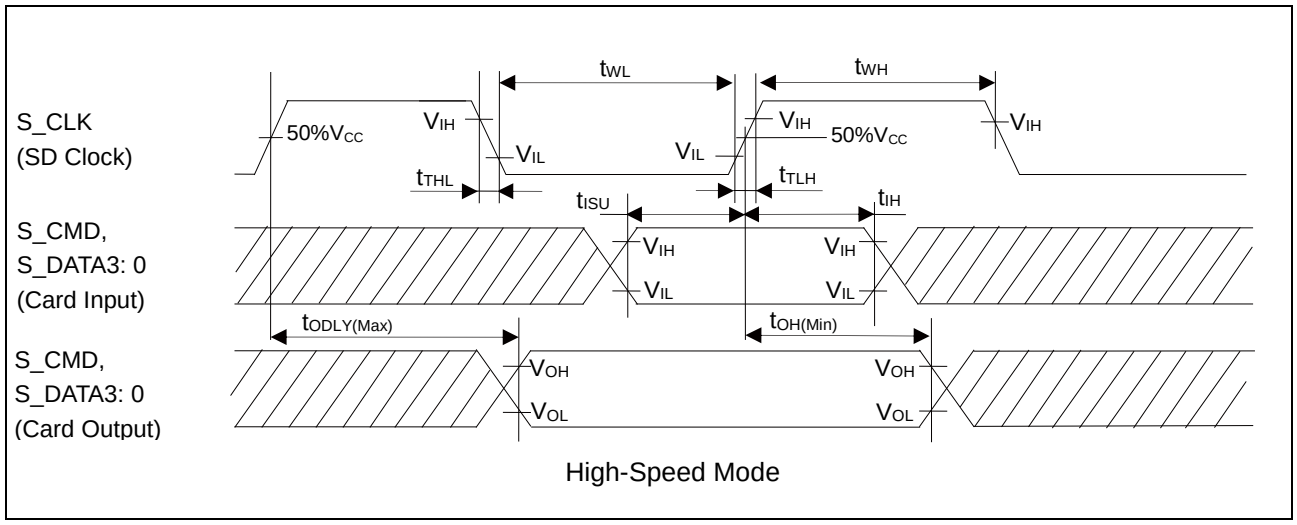
■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1 card)	6	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		2	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output delay time during data transfer mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_L ≤ 40 pF (1 card)	0	14	ns
Output hold time	t_{OH}	S_CMD, S_DATA3: 0	C_L ≥ 15 pF (1 card)	2.5	-	ns
Total system capacitance for each line*	C_L	-	1 card	-	40	pF

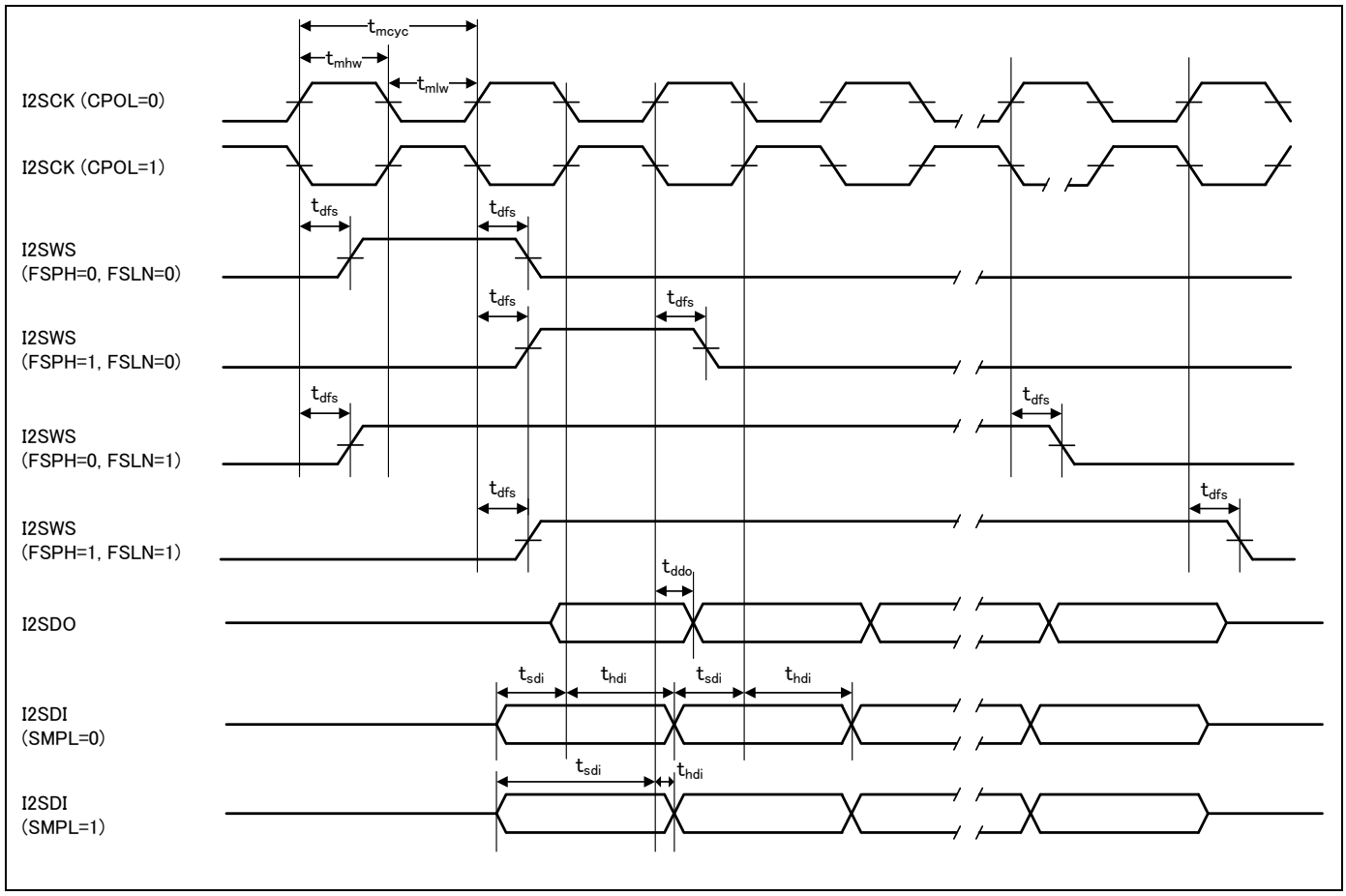
*: In order to satisfy severe timing, host shall drive only one card.



High-Speed Mode

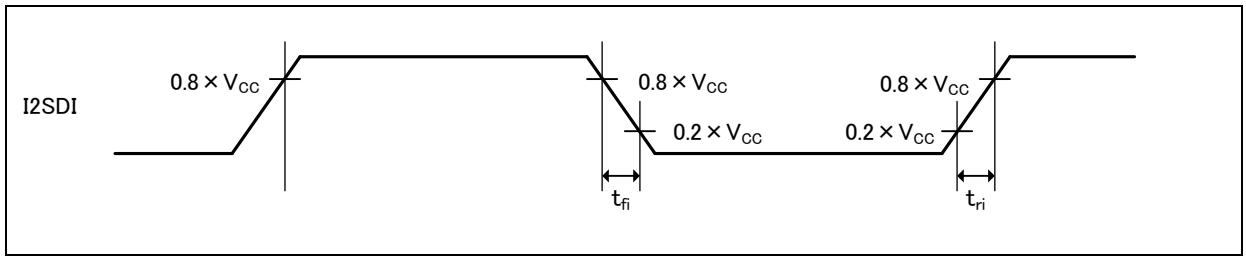
Notes:

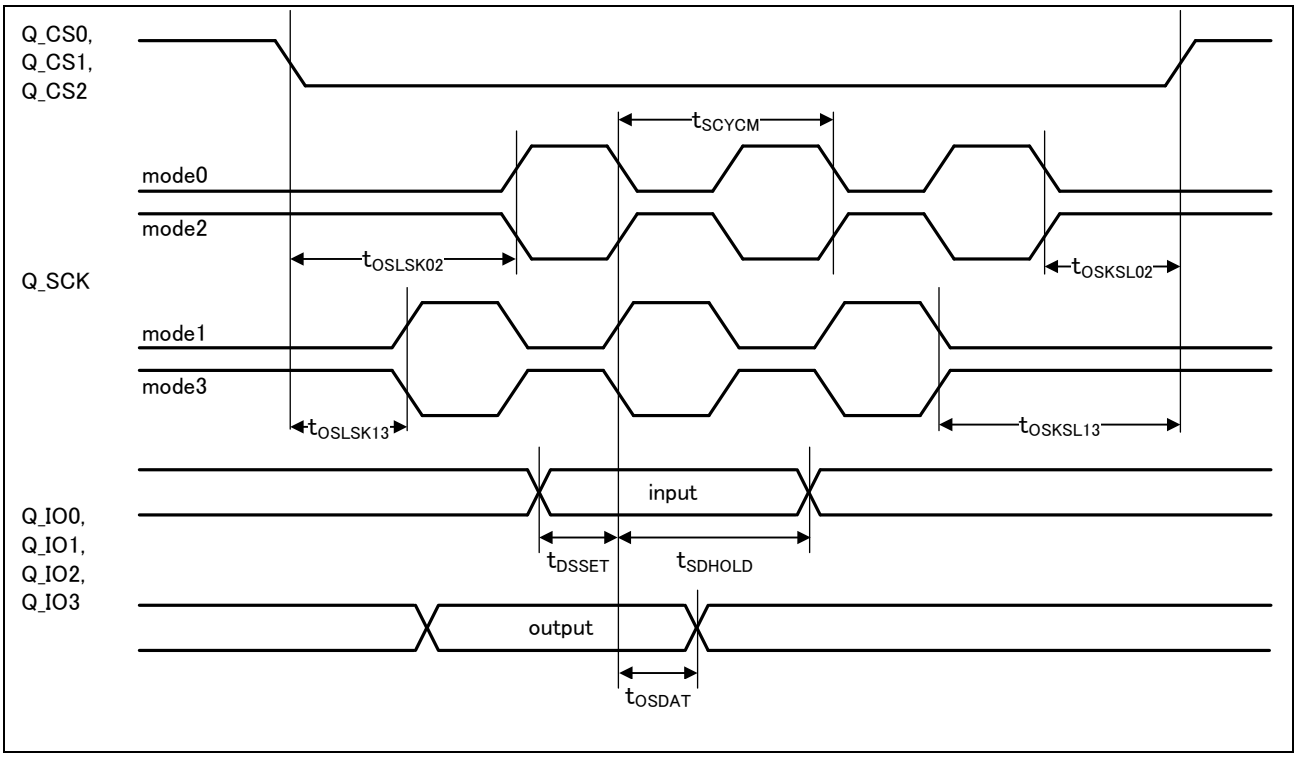
- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*



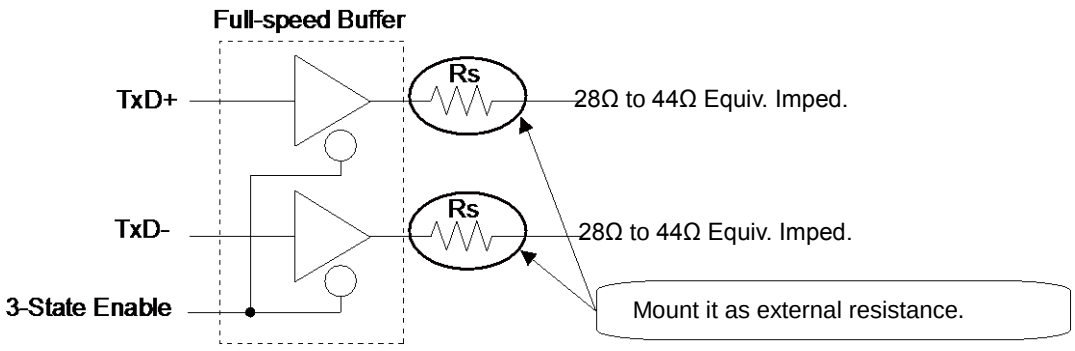
Note:

- *See Chapter7-2: I²S (Inter-IC Sound bus) Interface in FM4 Family Peripheral Manual Communication Macro Part (002-04862) for the details of CPOL, FSPH, FSLIN, and SMPL.*



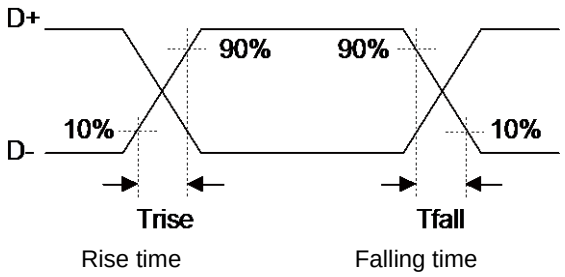

Q_CS0,
Q_CS1,
Q_CS2
tSCYCM
mode0
mode2
tOSLSK02
tOSKSL02
Q_SCK
mode1
mode3
tOSLSK13
tOSKSL13
input
Q_IO0,
Q_IO1,
Q_IO2,
Q_IO3
tDSSET
tSDHOLD
output
tOSDAT

*6: USB Full-speed connection is performed via twisted-pair cable shield with 90 Ω ± 15% characteristic impedance (differential mode).
USB standard defines that the output impedance of the USB driver must be in the range from 28 Ω to 44 Ω. So, a discrete series resistor (Rs) addition is defined in order to satisfy the above definition and keep balance.
When using this USB I/O, use it with 25 Ω to 30 Ω (recommended value 27 Ω) series resistor Rs.



Rs series resistor 25Ω to 30Ω
Series resistor of 27Ω (recommendation value) must be added.
And, use "resistance with an uncertainty of 5% by E24 sequence."

*7: They indicate rise time (Trise) and fall time (Tfall) of the low-speed differential data signal.
They are defined by the time between 10% and 90% of the output signal voltage.



Note:
- *See Low-Speed Load (Compliance Load) for conditions of external load.*

12.8 Low-Voltage Detection Characteristics

12.8.1 Low-Voltage Detection Reset

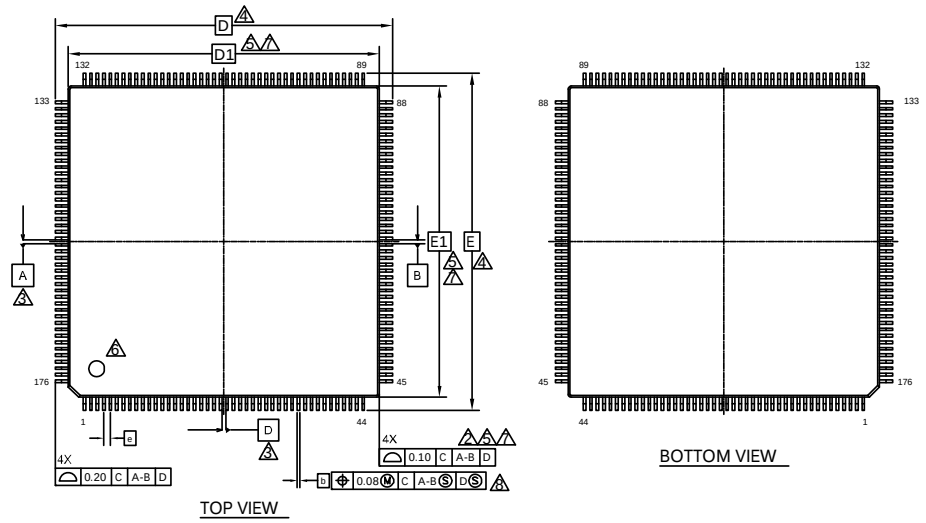
Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

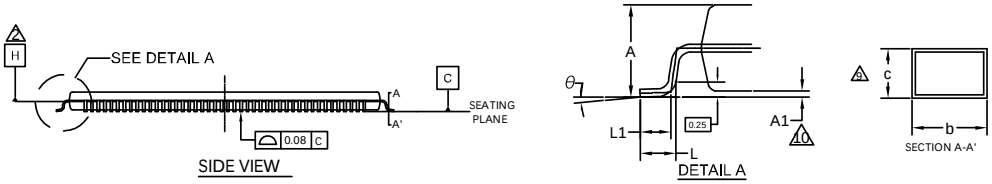
12.8.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	$6000 \times t_{CYCP}$ *	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

Package Type	Package Code
LQFP 176	LQP 176





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC		
D1	24.00 BSC		
e	0.50 BSC		
E	26.00 BSC		
E1	24.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15150 **

PACKAGE OUTLINE, 176 LEAD LQFP
24.0X24.0X1.7 MM LQP176 REV**