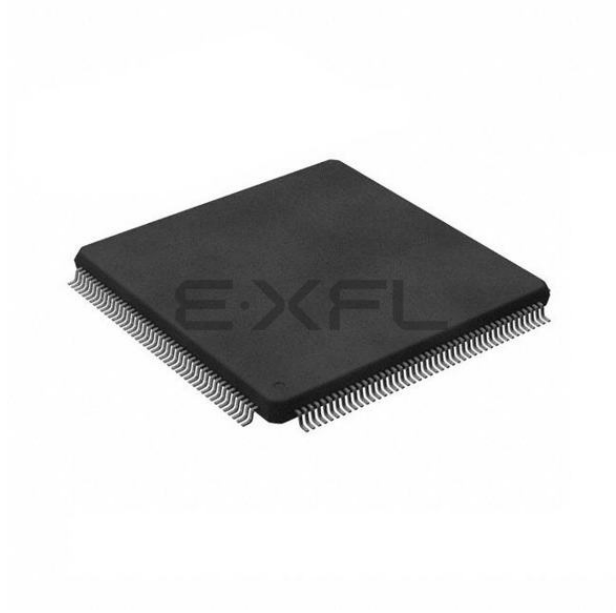

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CANbus, CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c5aj0agv2000a

Base Timer (Max 16 Channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 120 high-speed general-purpose I/O ports in 144 pin package
- Some pins 5V tolerant I/O.
  See 4. Pin Descriptions and 5. I/O Circuit Type for the corresponding pins.

Multi-function Timer (Max three Units)

The multi-function timer is composed of the following blocks:

Minimum resolution: 5.00 ns

- 16-bit free-run timer × 3 ch/unit
- Input capture × 4 ch/unit
- Output compare × 6 ch/unit
- A/D activation compare × 6 ch/unit
- Waveform generator × 3 ch/unit
- 16-bit PPG timer × 3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

Real-Time Clock (RTC)

The real-time clock can count year, month, day, hour, minute, second, or day of the week from 00 to 99.

- Interrupt function with specifying date and time (year/month/day/hour/minute) is available. This function is also available by specifying only year, month, day, hour, or minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC; Max four Channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. It is also possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The dual timer consists of two programmable 32-/16-bit down counters.

Operation mode is selectable from the following for each channel:

- Free-running
- Periodic (= Reload)
- One shot

Watch Counter

The watch counter is used for wake up from low-power consumption mode. It is possible to select the main clock, sub clock, built-in High-speed CR clock, or built-in low-speed CR clock as the clock source.

- Interval timer: up to 64 s (max) with a sub clock of 32.768 kHz

External Interrupt Controller Unit

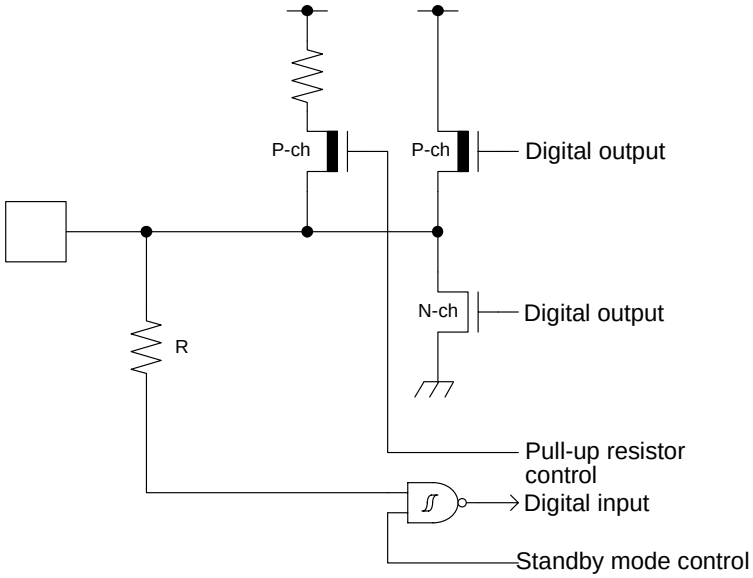
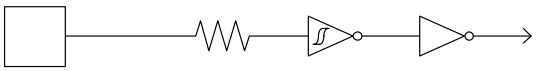
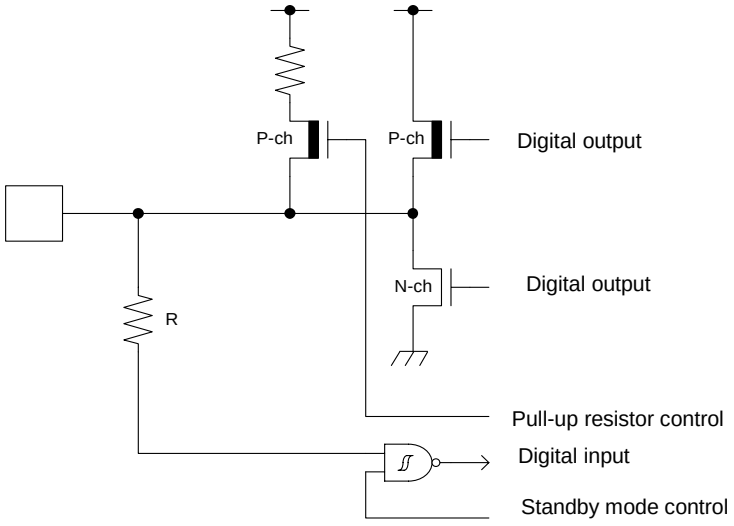
- External interrupt input pin: Max 32 pins
- Include one non-maskable interrupt (NMI)

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
106	86	70	P12	PE2 X0	A	A
107	87	71	P13	PE3 X1	A	B
108	88	72	N14	VSS	-	-
109	89	73	M14	VCC	-	-
110	90	74	M13	AVCC	-	-
111	91	75	M12	AVSS	-	-
112	92	76	L13	AVRL	-	-
113	93	77	L12	AVRH	-	-
114	94	78	L11	P10 AN00 SIN10_0 TIOA0_2 AIN0_2 INT08_0	F	M
115	95	79	K13	P11 AN01 SOT10_0 (SDA10_0) TIOB0_2 BIN0_2	F	L
116	96	80	K12	P12 AN02 SCK10_0 (SCL10_0) TIOA1_2 ZIN0_2	F	L
117	97	81	K14	P13 AN03 SIN6_1 RX1_1 INT25_1	F	M
118	98	82	K11	P14 AN04 SOT6_1 (SDA6_1) TX1_1	F	L
119	-	-	-	PB8 ADTG_6 SCS63_1 INT08_2 TRACED8	E	O
120	-	-	-	PB9 SIN9_1 AIN2_2 INT09_2 TRACED9	E	O
121	-	-	-	PBA SOT9_1 (SDA9_1) BIN2_2 TRACED10	E	N

Pin No				Pin Name	I/O circuit type	Pin state type
LQQ216	LQP176	LQS144	LBE192			
143	117	93	G9	P1F AN15 RTS5_0 TIOB8_1 INT27_1 MAD11_0	F	M
144	118	94	F10	P2A AN24 CTS5_0 MAD12_0	F	L
145	119	95	F11	P29 AN25 SCK5_0 (SCL5_0) MAD13_0	F	L
146	120	96	F12	P28 AN26 SOT5_0 (SDA5_0) MAD14_0	F	L
147	121	97	F13	P27 AN27 SIN5_0 INT24_0 MAD15_0	F	M
148	-	-	-	PBC TX1_2 TRACED12	E	N
149	-	-	-	PBD SCK0_1 (SCL0_1) RX1_2 AIN3_2 INT10_2 TRACED13	E	O
150	-	-	-	PBE SOT0_1 (SDA0_1) BIN3_2 TRACED14	E	N
151	-	-	-	PBF SIN0_1 ZIN3_2 INT11_2 TRACED15	E	O
152	122	98	E10	P26 TX1_0 MAD16_0	E	I
153	123	99	E11	P25 AN28 RX1_0 INT25_0 MAD17_0	F	M

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-function Timer 1	DTTI1X_0	Input signal controlling wave form generator outputs RTO10 to RTO15 of Multi-function timer 1.	70	55	47	L5
	DTTI1X_1		94	-	-	-
	FRCK1_0	16-bit free-run timer ch.1 external clock input pin	71	56	48	M5
	FRCK1_1		78	63	-	K5
	IC10_0	16-bit input capture input pin of Multi-function timer 1. ICxx describes channel number.	96	79	63	L10
	IC10_1		95	-	-	-
	IC11_0		97	80	64	K10
	IC11_1		101	-	-	-
	IC12_0		98	81	65	M10
	IC12_1		102	-	-	-
	IC13_0		99	82	66	N11
	IC13_1		103	-	-	-
	RTO10_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	56	46	38	N2
	RTO10_1 (PPG10_1)		85	70	-	N8
	RTO11_0 (PPG10_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	57	47	39	N3
	RTO11_1 (PPG10_1)		86	71	-	M8
	RTO12_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	58	48	40	M3
	RTO12_1 (PPG12_1)		87	72	-	N9
	RTO13_0 (PPG12_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	59	49	41	L4
	RTO13_1 (PPG12_1)		88	73	-	P9
	RTO14_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	60	50	42	M4
	RTO14_1 (PPG14_1)		89	74	-	M9
	RTO15_0 (PPG14_0)	Wave form generator output pin of Multi-function timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	61	51	43	N4
	RTO15_1 (PPG14_1)		90	75	-	L9

Module	Pin name	Function	Pin No			
			LQQ 216	LQP 176	LQS 144	LBE 192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch.0 AIN input pin	56	46	38	N2
	AIN0_1		65	-	-	-
	AIN0_2		114	94	78	L11
	BIN0_0	QPRC ch.0 BIN input pin	57	47	39	N3
	BIN0_1		66	-	-	-
	BIN0_2		115	95	79	K13
	ZIN0_0	QPRC ch.0 ZIN input pin	58	48	40	M3
	ZIN0_1		67	-	-	-
	ZIN0_2		116	96	80	K12
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch.1 AIN input pin	91	76	60	K9
	AIN1_1		94	-	-	-
	AIN1_2		123	99	83	J13
	BIN1_0	QPRC ch.1 BIN input pin	92	77	61	P10
	BIN1_1		95	-	-	-
	BIN1_2		124	100	84	J12
	ZIN1_0	QPRC ch.1 ZIN input pin	93	78	62	N10
	ZIN1_1		101	-	-	-
	ZIN1_2		125	101	85	J11
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch.2 AIN input pin	2	2	2	B2
	AIN2_1		32	23	20	G5
	AIN2_2		120	-	-	-
	BIN2_0	QPRC ch.2 BIN input pin	3	3	3	C2
	BIN2_1		36	26	21	H2
	BIN2_2		121	-	-	-
	ZIN2_0	QPRC ch.2 ZIN input pin	4	4	4	C3
	ZIN2_1		37	27	22	J1
	ZIN2_2		122	-	-	-

Type	Circuit	Remarks
I		・ CMOS level output ・ CMOS level hysteresis input ・ 5V tolerant ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA ・ Available to control of PZR registers (pseudo-open drain control) ・ For PZR registers, refer to GPIO in the “FM4 Family Peripheral Manual Main Part (002-04856)”.
J		CMOS level hysteresis input
K		・ CMOS level output ・ TTL level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4mA, I_{OL} = 4mA

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of static electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive gases, dust, or oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, including cosmic radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, flame

   CAUTION: Plastic molded devices are flammable and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Peripheral Address Map

Start Address	End Address	Bus	Peripherals
0x4000_0000	0x4000_0FFF	AHB	MainFlash I/F register
0x4000_1000	0x4000_FFFF		Reserved
0x4001_0000	0x4001_0FFF	APB0	Clock/reset control
0x4001_1000	0x4001_1FFF		Hardware watchdog timer
0x4001_2000	0x4001_2FFF		Software watchdog timer
0x4001_3000	0x4001_4FFF		Reserved
0x4001_5000	0x4001_5FFF		Dual-timer
0x4001_6000	0x4001_FFFF		Reserved
0x4002_0000	0x4002_0FFF	APB1	Multi-Function Timer unit 0
0x4002_1000	0x4002_1FFF		Multi-Function Timer unit 1
0x4002_2000	0x4002_2FFF		Multi-Function Timer unit 2
0x4002_3000	0x4002_3FFF		Reserved
0x4002_4000	0x4002_4FFF		PPG
0x4002_5000	0x4002_5FFF		Base timer
0x4002_6000	0x4002_6FFF		Quadrature position/revolution counter
0x4002_7000	0x4002_7FFF		A/D converter
0x4002_8000	0x4002_DFFF		Reserved
0x4002_E000	0x4002_EFFF		Internal CR trimming
0x4002_F000	0x4002_FFFF		Reserved
0x4003_0000	0x4003_0FFF	APB2	External interrupt controller
0x4003_1000	0x4003_1FFF		Interrupt request batch-read function
0x4003_2000	0x4003_2FFF		Reserved
0x4003_3000	0x4003_3FFF		D/A converter
0x4003_4000	0x4003_4FFF		Reserved
0x4003_5000	0x4003_57FF		Low voltage detector
0x4003_5800	0x4003_5FFF		Deep standby mode Controller
0x4003_6000	0x4003_6FFF		USB clock generator
0x4003_7000	0x4003_7FFF		CAN prescaler
0x4003_8000	0x4003_8FFF		Multi-function serial interface
0x4003_9000	0x4003_9FFF		CRC
0x4003_A000	0x4003_AFFF		Watch counter
0x4003_B000	0x4003_BFFF		RTC/port control
0x4003_C000	0x4003_C0FF		Low-speed CR prescaler
0x4003_C100	0x4003_C7FF		Peripheral clock gating
0x4003_C800	0x4003_CFFF		Reserved
0x4003_D000	0x4003_DFFF		I^2S prescaler
0x4003_E000	0x4003_EFFF		Reserved
0x4003_F000	0x4003_FFFF		External memory interface

List of Pin Behavior by Mode State

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC Mode or Deep Standby Stop mode State		Return From Deep Standby Mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
A	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Main crystal oscillator input pin/ external main clock input selected	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input Enabled
B	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	External main clock input selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous state	Hi-Z/internal input fixed at 0	Maintain previous State
	Main crystal oscillator output pin	Hi-Z/ internal input fixed at 0/ or input enable	Hi-Z/ internal input fixed at 0	Hi-Z/ internal input fixed at 0	Maintain previous state while oscillator active/ When oscillation stops*1, it will be Hi-Z/ Internal input fixed at 0					
C	INITX input pin	Pull-up/ input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled	Pull-up/ Input enabled
D	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
E	Mode input pin	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled	Input enabled
	GPIO selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/ input enabled	GPIO selected	Hi-Z/ input enabled	GPIO selected

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θja (°C/W)	Maximum Permissible Power (mW)	
			T_A = +85°C	T_A = +105°C
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645
LQQ216 (0.4-mm pitch)	Single-layered both sides	46	870	435
	4 layers	32	1250	625
LBE192 (0.8-mm pitch)	Single-layered both sides	-	-	-
	4 layers	35	1143	571

WARNING:

1. *The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.*
2. *Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.*
3. *No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet.*
4. *Users considering application outside the listed conditions are advised to contact their representatives beforehand.*

Calculation Method of Power Dissipation (Pd)

The power dissipation is shown in the following formula.

$$Pd = V_{CC} \times I_{CC} + \Sigma (I_{OL} \times V_{OL}) + \Sigma ((V_{CC}-V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current
I_{OH}: H level output current
V_{OL}: L level output voltage
V_{OH}: H level output voltage

I_{CC} is the current drawn by the device.
It can be analyzed as follows.

$$I_{CC} = I_{CC}(INT) + \Sigma I_{CC}(IO)$$

I_{CC} (INT): Current drawn by internal logic and memory, etc. through the regulator

ΣI_{CC} (IO): Sum of current (I/O switching current) drawn by the output pin

For I_{CC} (INT), it can be anticipated by (1) Current Rating in 12.3. DC Characteristics (This rating value does not include I_{CC} (IO) for a value at pin fixed).
For I_{CC} (IO), it depends on system used by customers.
The calculation formula is shown below.

$$I_{CC}(IO) = (C_{INT} + C_{EXT}) \times V_{CC} \times f_{SW}$$

C_{INT}: Pin internal load capacitance
C_{EXT}: External load capacitance of output pin
f_{SW}: Pin switching frequency

Parameter	Symbol	Conditions	Capacitance Value
Pin internal load capacitance	C_{INT}	4 mA type	1.93 pF
		8 mA type	3.45 pF
		12 mA type	3.42 pF

Calculate I_{CC} (Max) as follows when the power dissipation can be evaluated by yourself:

Measure current value I_{CC} (Typ) at normal temperature (+25°C).

Add maximum leakage current value I_{CC} (leak_max) at operating on a value in (1).

$$I_{CC}(Max) = I_{CC}(Typ) + I_{CC}(leak\_max)$$

Parameter	Symbol	Conditions	Current Value
Maximum leakage current at operating	I_{CC} (leak_max)	T_J = +125°C	79.2 mA
		T_J = +105°C	39.4 mA
		T_J = +85°C	26.5 mA

Table 12-3 Typical and Maximum Current Consumption in Normal Operation(PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7 (PLL)	*5	72 MHz	71	161	mA	*3 When all peripheral clocks are on
					60 MHz	62	150	mA	
					48 MHz	51	138	mA	
					36 MHz	40	125	mA	
					24 MHz	29	112	mA	
					12 MHz	17	98	mA	
					8 MHz	13	93	mA	
					4 MHz	8.4	88.5	mA	
				*5	72 MHz	46	132	mA	*3 When all peripheral clocks are off
					60 MHz	41	125	mA	
					48 MHz	34	118	mA	
					36 MHz	27	110	mA	
					24 MHz	20	102	mA	
					12 MHz	12	93	mA	
					8 MHz	9.4	89.7	mA	
					4 MHz	6.5	86.4	mA	

*1: T_A = +25°C, V_{CC} = 3.3 V

*2: T_J = +125°C, V_{CC} = 5.5 V

*3: When all ports are fixed

*4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

*5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

*6: With data access to a MainFlash memory.

*7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-8 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCH}	VCC	Stop mode	-	0.56	3.01	mA	*3, *4 T_A = +25°C
					-	27.03	mA	*3, *4 T_A = +85°C
					-	39.92	mA	*3, *4 T_A = +105°C
	I_{CCT}		Timer mode*5 (main oscillation)	4 MHz	1.40	3.85	mA	*3, *4 T_A = +25°C
					-	27.87	mA	*3, *4 T_A = +85°C
					-	40.76	mA	*3, *4 T_A = +105°C
			Timer mode (built-in High-speed CR)	4 MHz	0.95	3.40	mA	*3, *4 T_A = +25°C
					-	27.42	mA	*3, *4 T_A = +85°C
					-	40.31	mA	*3, *4 T_A = +105°C
			Timer mode*6 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T_A = +25°C
					-	27.04	mA	*3, *4 T_A = +85°C
					-	39.93	mA	*3, *4 T_A = +105°C
			Timer mode (built-in low-speed CR)	100 kHz	0.58	3.03	mA	*3, *4 T_A = +25°C
					-	27.05	mA	*3, *4 T_A = +85°C
					-	39.94	mA	*3, *4 T_A = +105°C
	I_{CCR}		RTC mode*6 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T_A = +25°C
					-	27.04	mA	*3, *4 T_A = +85°C
					-	39.93	mA	*3, *4 T_A = +105°C

*1: V_{CC} = 3.3V

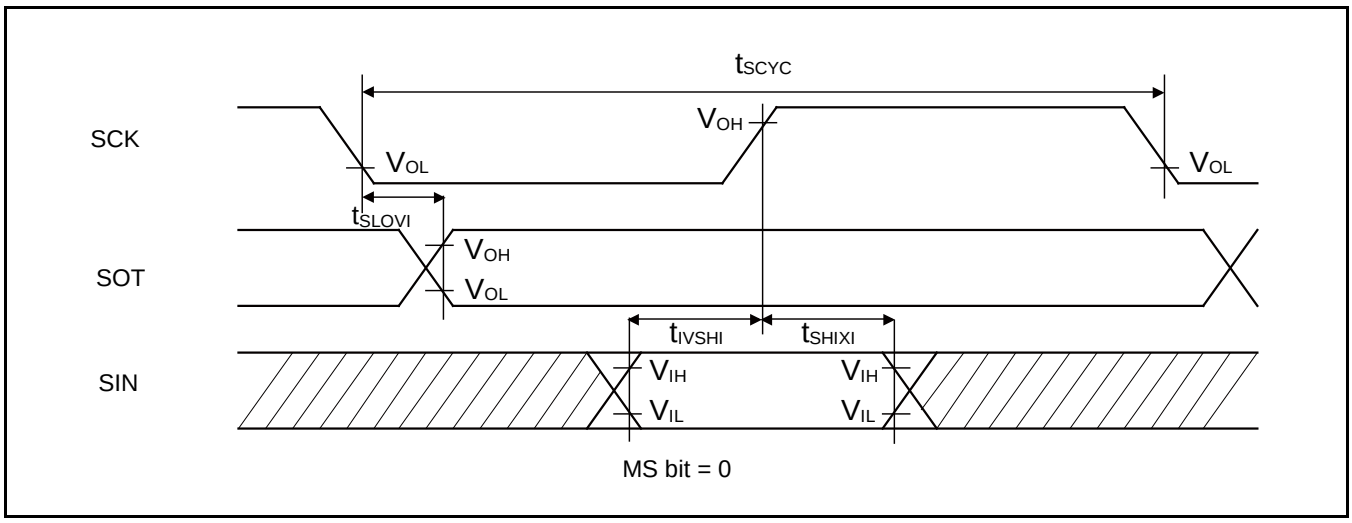
*2: V_{CC} = 5.5V

*3: When all ports are fixed

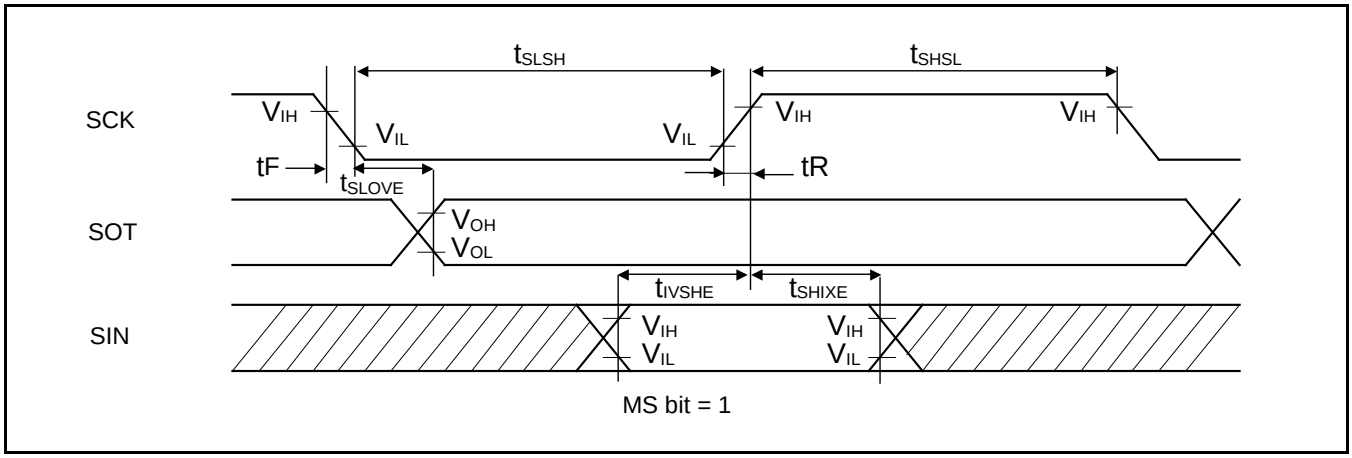
*4: When LVD is off

*5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

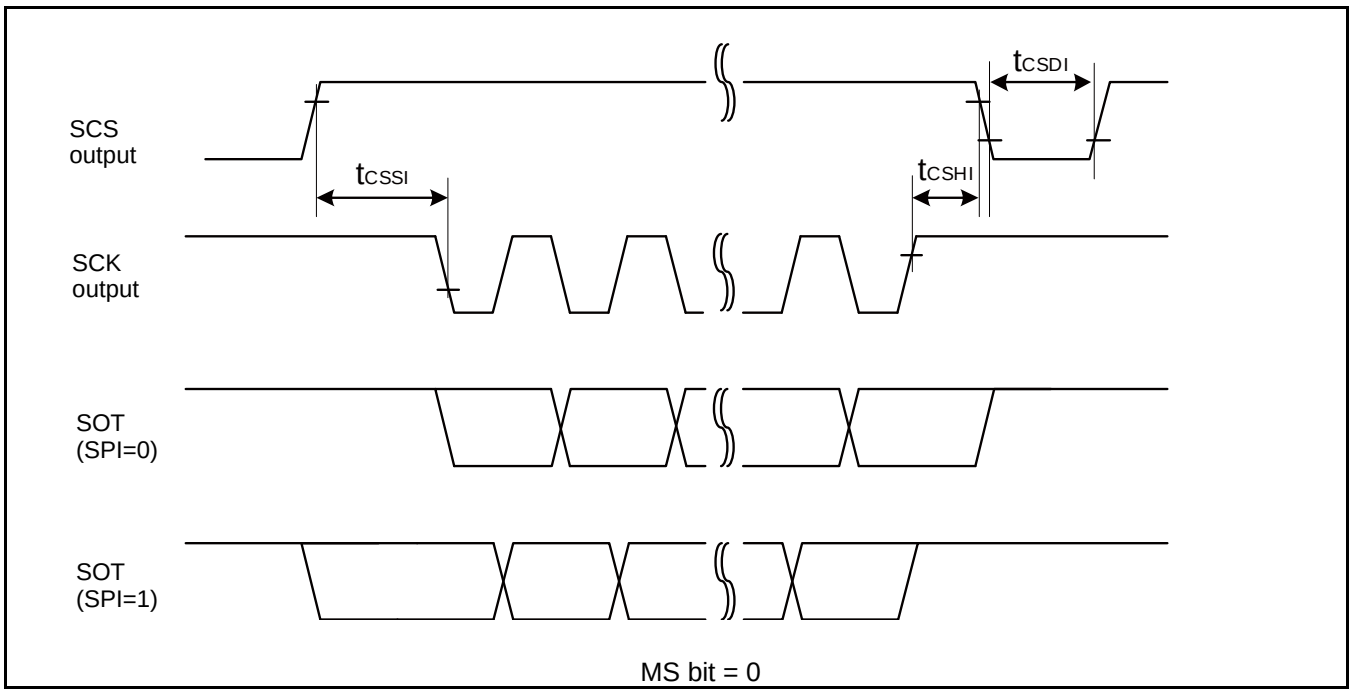
*6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)



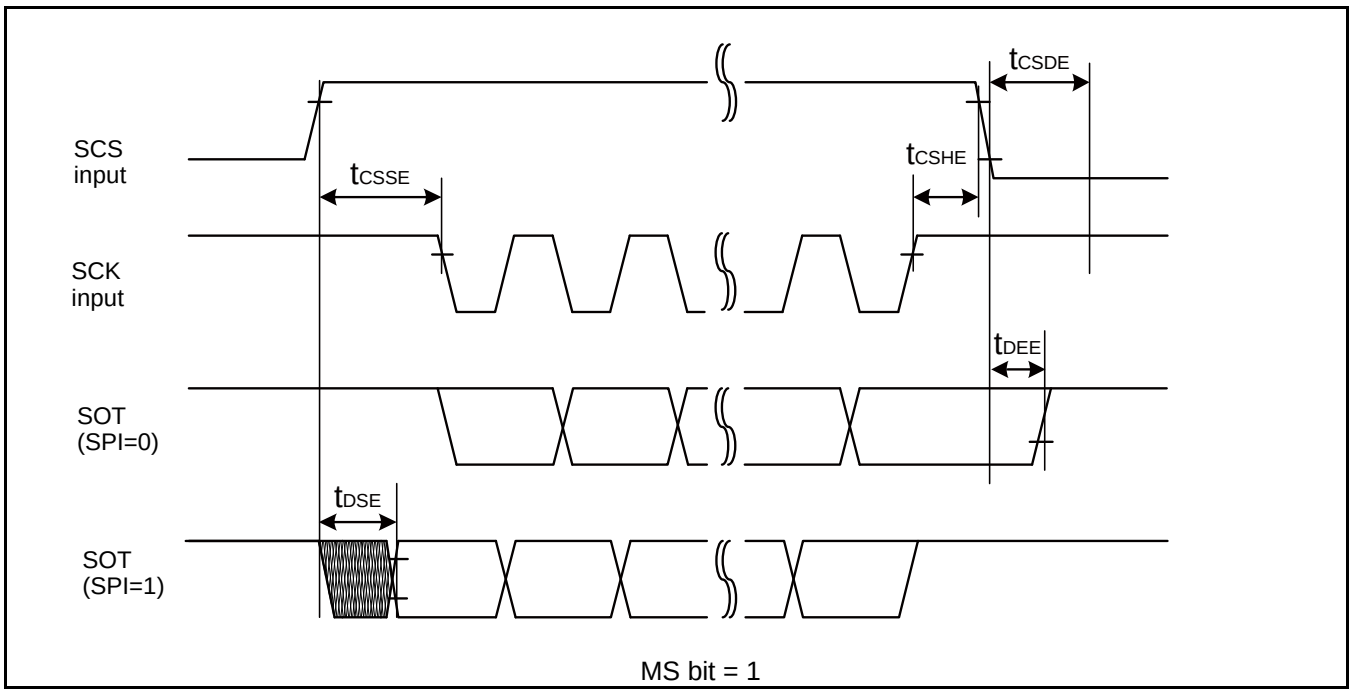
MS bit = 0



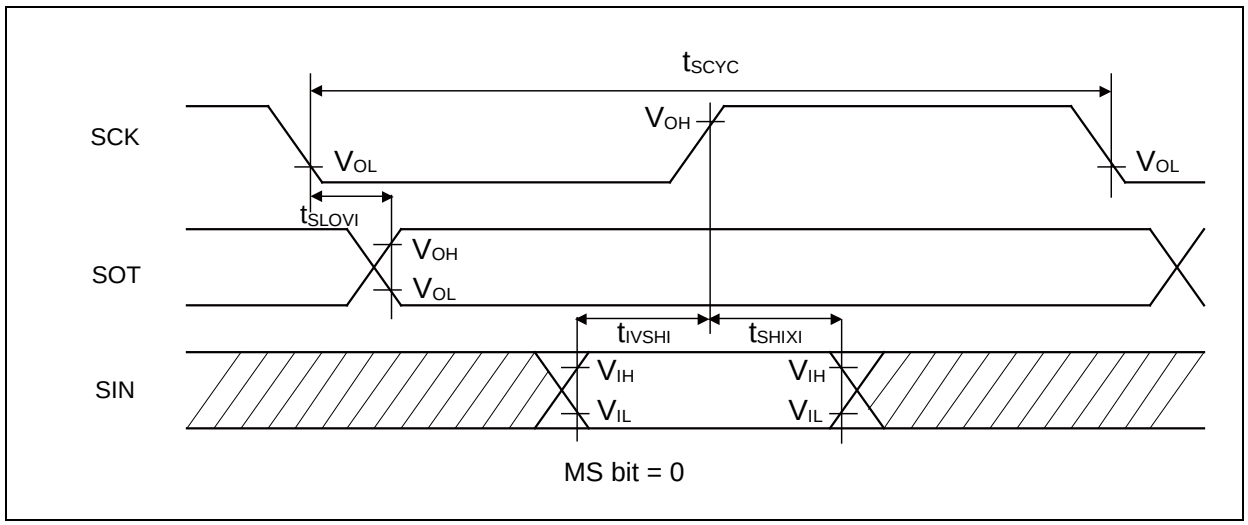
MS bit = 1



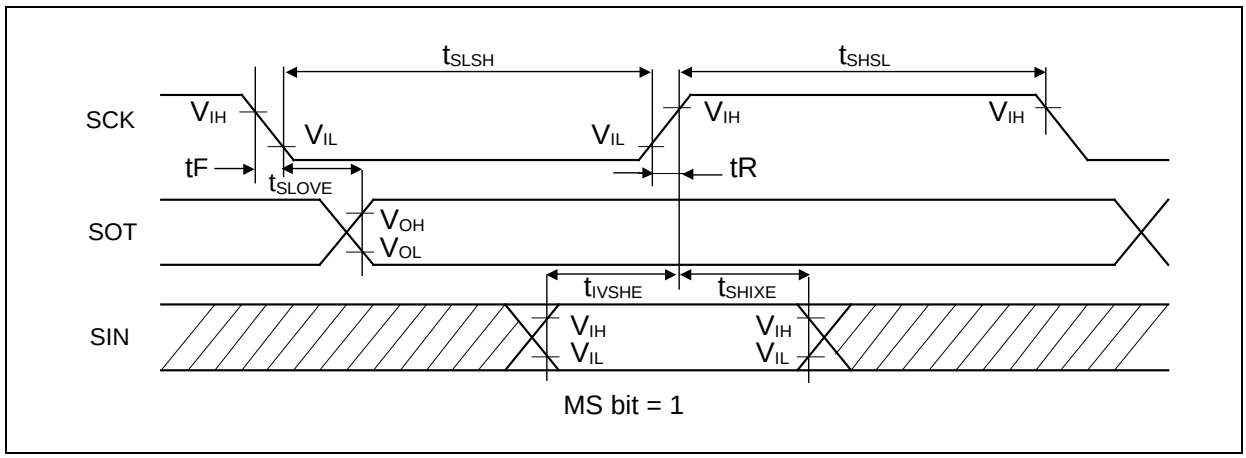
MS bit = 0



MS bit = 1



MS bit = 0



MS bit = 1

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↑→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↑→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↓ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↑→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↓→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

High-Speed Mode

■Clock CLK (All values are referred to V_{IH} and V_{IL})

(V_{CC} = 2.7V to 3.6V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Clock frequency Data Transfer Mode	f_{PP}	S_CLK	C_{CARD} ≤ 10 pF (1 card)	0	50	MHz
Clock low time	t_{WL}	S_CLK		7	-	ns
Clock high time	t_{WH}	S_CLK		7	-	ns
Clock rise time	t_{TLH}	S_CLK		-	3	ns
Clock fall time	t_{THL}	S_CLK		-	3	ns

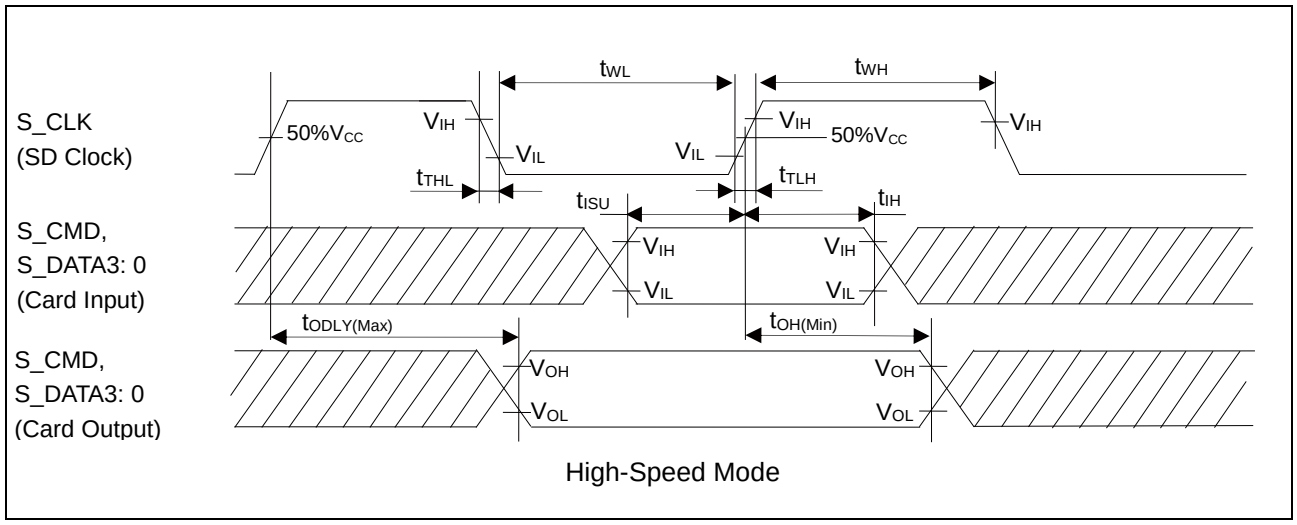
■Card Inputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Input set-up time	t_{ISU}	S_CMD, S_DATA3: 0	C_{CARD} ≤ 10 pF (1 card)	6	-	ns
Input hold time	t_{IH}	S_CMD, S_DATA3: 0		2	-	ns

■Card Outputs CMD, DAT (referenced to Clock CLK)

Parameter	Symbol	Pin Name	Conditions	Value		Remarks
				Min	Max	
Output delay time during data transfer mode	t_{ODLY}	S_CMD, S_DATA3: 0	C_L ≤ 40 pF (1 card)	0	14	ns
Output hold time	t_{OH}	S_CMD, S_DATA3: 0	C_L ≥ 15 pF (1 card)	2.5	-	ns
Total system capacitance for each line*	C_L	-	1 card	-	40	pF

*: In order to satisfy severe timing, host shall drive only one card.



High-Speed Mode

Notes:

- *The Card Input corresponds to the Host Output and the Card Output corresponds to the Host Input because this model is the Host.*
- *For more information about clock frequency (f_{PP}), see Chapter 15: SD card Interface in FM4 Family Peripheral Manual Main Part (002-04856).*

12.6 12-bit D/A Converter

Electrical Characteristics for the D/A Converter

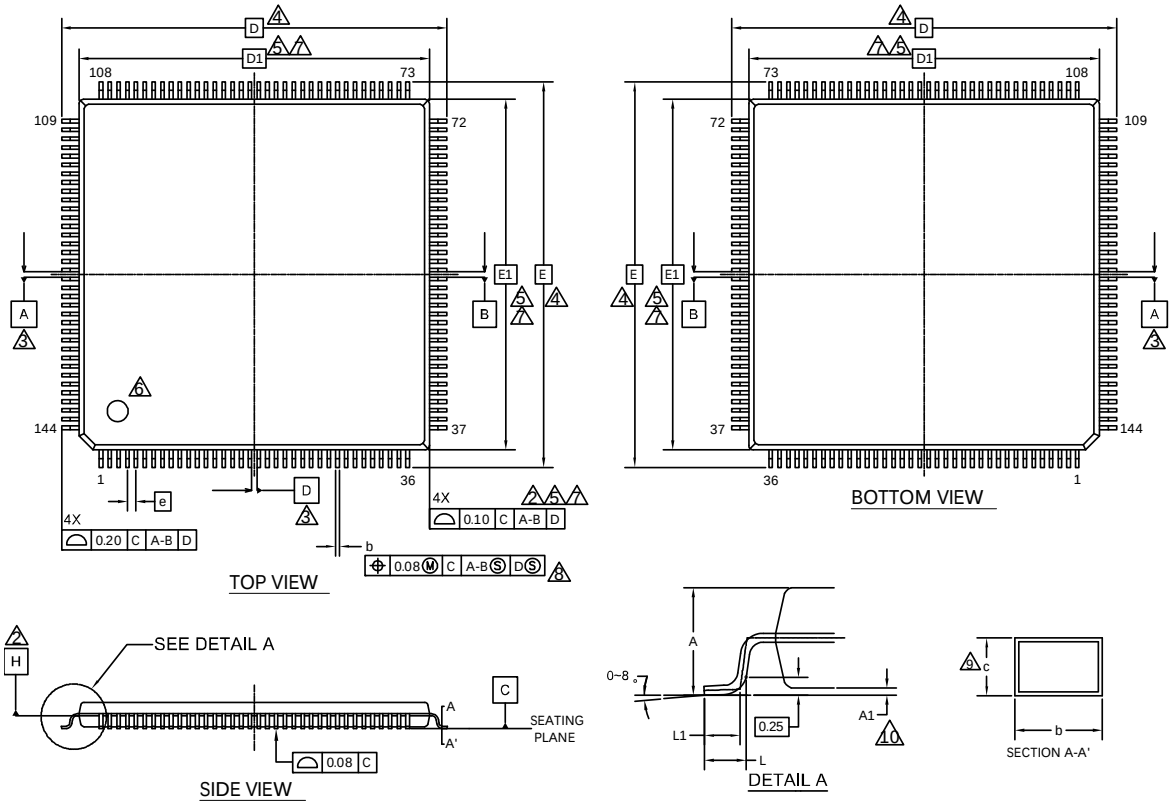
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	DAx	-	-	12	bit	
Conversion time	t_{C20}		0.56	0.69	0.81	µs	Load 20 pF
	t_{C100}		2.79	3.42	4.06	µs	Load 100 pF
Integral nonlinearity*	INL		- 16	-	+ 16	LSB	
Differential nonlinearity*	DNL		- 0.98	-	+ 1.5	LSB	
Output voltage offset	V_{OFF}		-	-	+ 10	mV	When setting 0x000
			- 20.0	-	+ 1.4	mV	When setting 0xFFF
Analog output impedance	R_O		3.10	3.80	4.50	kΩ	D/A operation
			2.0	-	-	MΩ	When D/A stop
Power supply current*	IDDA	AVCC	260	330	410	µs	D/A 1ch operation AV_{CC} = 3.3 V
			400	510	620	µs	D/A 1ch operation AV_{CC} = 5.0 V
	IDSA		-	-	14	µs	When D/A stop

*: During no load

14. Package Dimensions

Package Type	Package Code
LQFP 144	LQS 144



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.00	——	0.20
b	0.17	0.22	0.27
c	0.09	——	0.20
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13015 **

PACKAGE OUTLINE, 144 LEAD LQFP
20.0X20.0X1.7 MM LQS144 Rev**