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## What is "Embedded - Microcontrollers"?

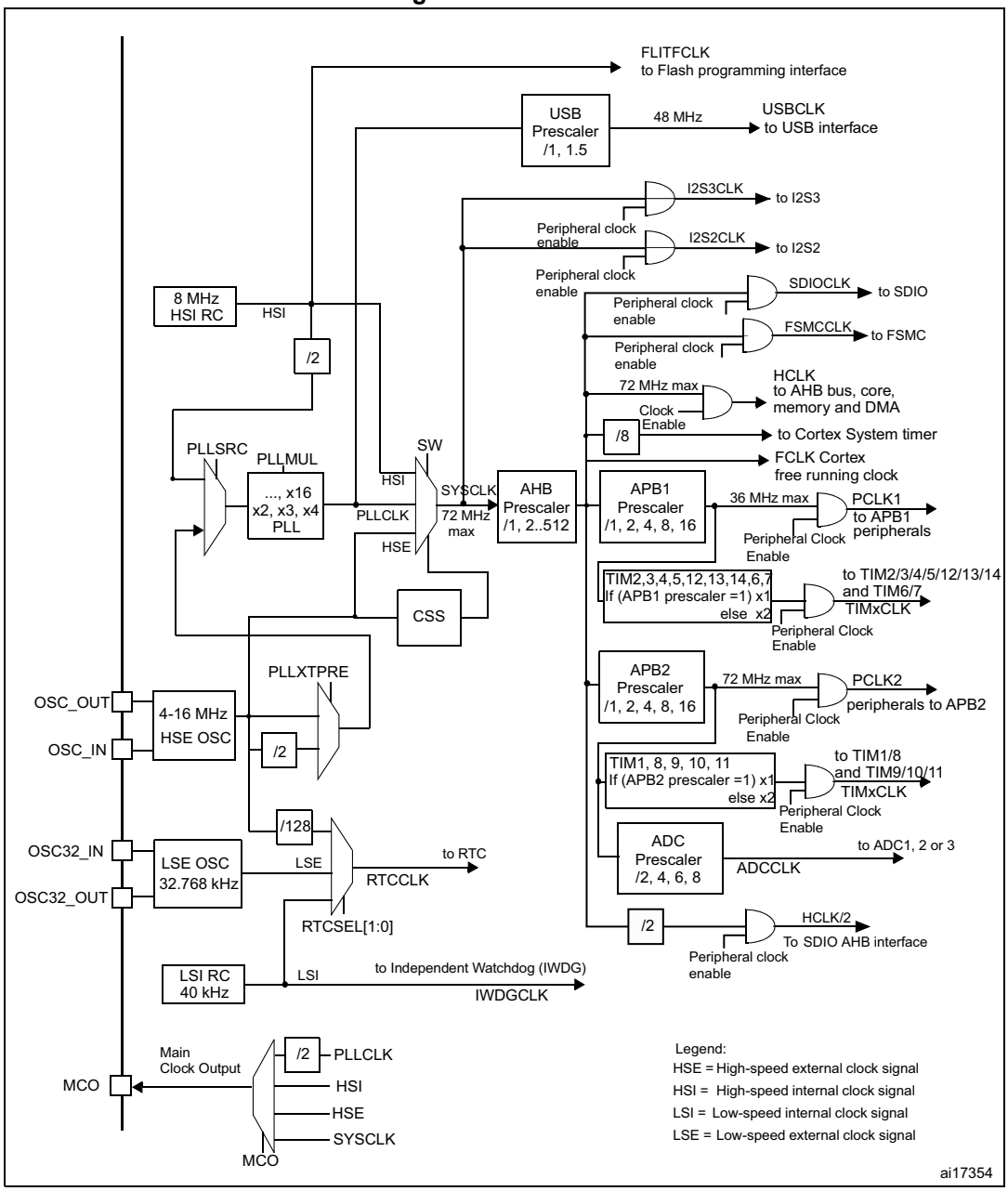
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 51 |
| Program Memory Size | 768KB (768K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rft6jtr |

# List of tables

**Figure 2. Clock tree**




1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the USBCLK at 48 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

### 2.3.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

### 2.3.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

### 2.3.12 Power supply schemes

- $V_{DD}$ = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to VDDA is 2.4 V when the ADC or DAC is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

### 2.3.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and $V_{PVD}$.

### 2.3.14 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

### 2.3.15 Low-power modes

The STM32F103xF and STM32F103xG performance line supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

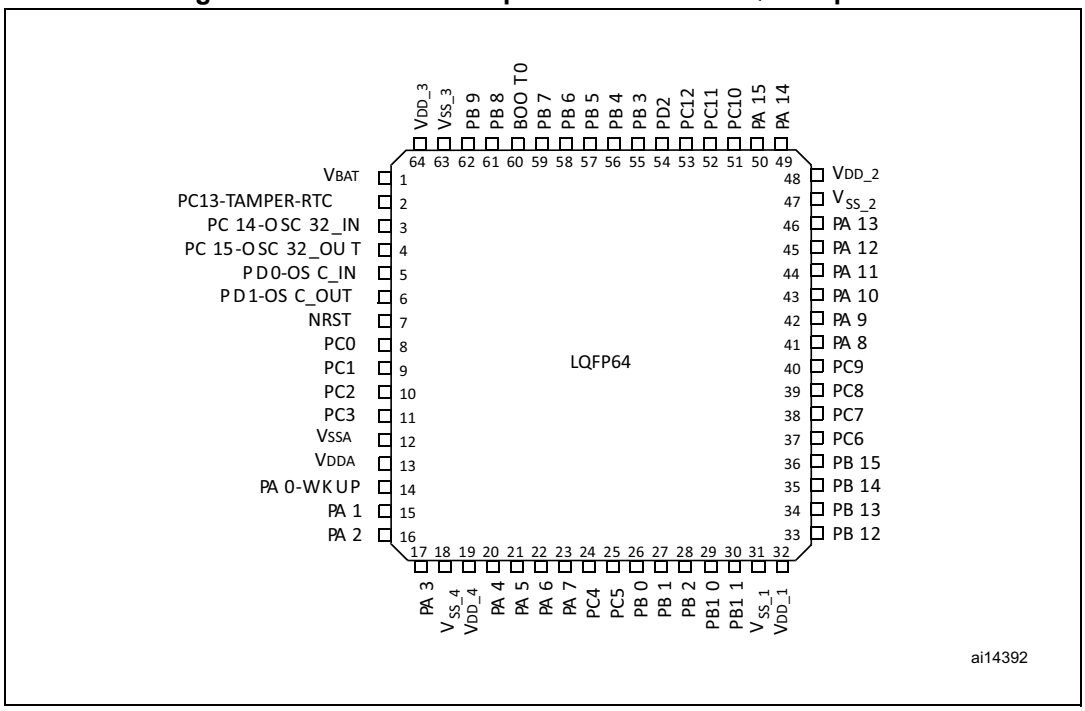
*Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.*

### 2.3.16 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

**Figure 6. STM32F103xF/G performance line LQFP64 pinout**




1. The above figure shows the package top view.

**Table 5. STM32F103xF and STM32F103xG pin definitions (continued)**

| Pins | | | | Pin name | Type(1) | I / O level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|---|
| LFBGA144 | LQFP64 | LQFP100 | LQFP144 | | | | | Default | Remap |
| A9 | - | 88 | 123 | PD7 | I/O | FT | PD7 | FSMC_NE1 / FSMC_NCE2 | USART2_CK |
| E8 | - | - | 124 | PG9 | I/O | FT | PG9 | FSMC_NE2 / FSMC_NCE3 | - |
| D8 | - | - | 125 | PG10 | I/O | FT | PG10 | FSMC_NCE4_1 / FSMC_NE3 | - |
| C8 | - | - | 126 | PG11 | I/O | FT | PG11 | FSMC_NCE4_2 | - |
| B8 | - | - | 127 | PG12 | I/O | FT | PG12 | FSMC_NE4 | - |
| D7 | - | - | 128 | PG13 | I/O | FT | PG13 | FSMC_A24 | - |
| C7 | - | - | 129 | PG14 | I/O | FT | PG14 | FSMC_A25 | - |
| E6 | - | - | 130 | $V_{SS\_11}$ | S | | $V_{SS\_11}$ | - | - |
| F6 | - | - | 131 | $V_{DD\_11}$ | S | | $V_{DD\_11}$ | - | - |
| B7 | - | - | 132 | PG15 | I/O | FT | PG15 | - | - |
| A7 | 55 | 89 | 133 | PB3 | I/O | FT | JTDO | SPI3_SCK / I2S3_CK/ | PB3/TRACESWO TIM2_CH2 / SPI1_SCK |
| A6 | 56 | 90 | 134 | PB4 | I/O | FT | NJTRST | SPI3_MISO | PB4/ TIM3_CH1 SPI1_MISO |
| B6 | 57 | 91 | 135 | PB5 | I/O | | PB5 | I2C1_SMBA / SPI3_MOSI / I2S3_SD | TIM3_CH2 / SPI1_MOSI |
| C6 | 58 | 92 | 136 | PB6 | I/O | FT | PB6 | I2C1_SCL(8)/ TIM4_CH1(8) | USART1_TX |
| D6 | 59 | 93 | 137 | PB7 | I/O | FT | PB7 | I2C1_SDA(8) / FSMC_NADV / TIM4_CH2(8) | USART1_RX |
| D5 | 60 | 94 | 138 | BOOT0 | I | | BOOT0 | - | - |
| C5 | 61 | 95 | 139 | PB8 | I/O | FT | PB8 | TIM4_CH3(8) / SDIO_D4 / TIM10_CH1 | I2C1_SCL/ CAN_RX |
| B5 | 62 | 96 | 140 | PB9 | I/O | FT | PB9 | TIM4_CH4(8) / SDIO_D5 / TIM11_CH1 | I2C1_SDA / CAN_TX |
| A5 | - | 97 | 141 | PE0 | I/O | FT | PE0 | TIM4_ETR / FSMC_NBL0 | - |
| A4 | - | 98 | 142 | PE1 | I/O | FT | PE1 | FSMC_NBL1 | - |
| E5 | 63 | 99 | 143 | $V_{SS\_3}$ | S | | $V_{SS\_3}$ | - | - |
| F5 | 64 | 100 | 144 | $V_{DD\_3}$ | S | | $V_{DD\_3}$ | - | - |

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.

4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
9. For devices delivered in LQFP64 packages, the FSMC function is not available.

**Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(2), all peripherals enabled | 72 MHz | 47.5 | 48.5 | mA |
| | | | 48 MHz | 34 | 35 | |
| | | | 36 MHz | 27.5 | 27.5 | |
| | | | 24 MHz | 20 | 20.5 | |
| | | | 16 MHz | 15 | 16 | |
| | | | 8 MHz | 9 | 11 | |
| | | External clock(2), all peripherals disabled | 72 MHz | 9.5 | 11.2 | |
| | | | 48 MHz | 7.7 | 9.5 | |
| | | | 36 MHz | 6.9 | 8.5 | |
| | | | 24 MHz | 5.9 | 7.8 | |
| | | | 16 MHz | 5.4 | 7.2 | |
| | | | 8 MHz | 4.7 | 6.4 | |

1. Guaranteed by characterization results, not tested in production at $V_{DD}$ max, $f_{HCLK}$ max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 20. Peripheral current consumption(1) (continued)**

| Peripheral | | Current consumption |
|---|---|---|
| APB1 (up to 36 MHz) | APB1-Bridge | 8,61 |
| | TIM2 | 37,22 |
| | TIM3 | 36,39 |
| | TIM4 | 35,56 |
| | TIM5 | 33,61 |
| | TIM6 | 7,78 |
| | TIM7 | 7,78 |
| | TIM12 | 19,17 |
| | TIM13 | 12,22 |
| | TIM14 | 13,33 |
| | SPI2/I2S2(3) | 8,33 |
| | SPI3/I2S3(3) | 8,33 |
| | USART2 | 12,22 |
| | USART3 | 12,22 |
| | UART4 | 12,22 |
| | UART5 | 12,22 |
| | I2C1 | 10,28 |
| | I2C2 | 10,28 |
| | USB | 18,89 |
| | CAN1 | 18,89 |
| | DAC(4) | 9,17 |
| | WWDG | 3,06 |
| | PWR | 2,50 |
| | BKP | 2,78 |
| | IWDG | 4,44 |

**Table 37. Synchronous multiplexed PSRAM write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(CLK)}$ | FSMC_CLK period | 27.5 | - | ns |
| $t_{d(CLKL-NExL)}$ | FSMC_CLK low to FSMC_Nex low (x = 0...2) | - | 0 | ns |
| $t_{d(CLKL-NExH)}$ | FSMC_CLK low to FSMC_NEx high (x = 0...2) | 1 | - | ns |
| $t_{d(CLKL-NADVL)}$ | FSMC_CLK low to FSMC_NADV low | - | 1 | ns |
| $t_{d(CLKL-NADVH)}$ | FSMC_CLK low to FSMC_NADV high | 1 | - | ns |
| $t_{d(CLKL-AV)}$ | FSMC_CLK low to FSMC_Ax valid (x = 16...25) | - | 0 | ns |
| $t_{d(CLKL-AIV)}$ | FSMC_CLK low to FSMC_Ax invalid (x = 16...25) | 1 | - | ns |
| $t_{d(CLKL-NWEL)}$ | FSMC_CLK low to FSMC_NWE low | - | 1 | ns |
| $t_{d(CLKL-NWEH)}$ | FSMC_CLK low to FSMC_NWE high | 1.5 | - | ns |
| $t_{d(CLKL-ADV)}$ | FSMC_CLK low to FSMC_AD[15:0] valid | - | 10 | ns |
| $t_{d(CLKL-ADIV)}$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 1 | - | ns |
| $t_{d(CLKL-Data)}$ | FSMC_A/D[15:0] valid after FSMC_CLK low | - | 6 | ns |
| $t_{d(CLKL-NBLH)}$ | FSMC_CLK low to FSMC_NBL high | 1 | - | ns |
| $t_{su(NWAITV-CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | 7 | - | ns |
| $t_{h(CLKH-NWAITV)}$ | FSMC_NWAIT valid after FSMC_CLK high | 2 | - | ns |

1. $C_L$ = 15 pF.

**Figure 35. PC Card/CompactFlash controller waveforms for I/O space write access**

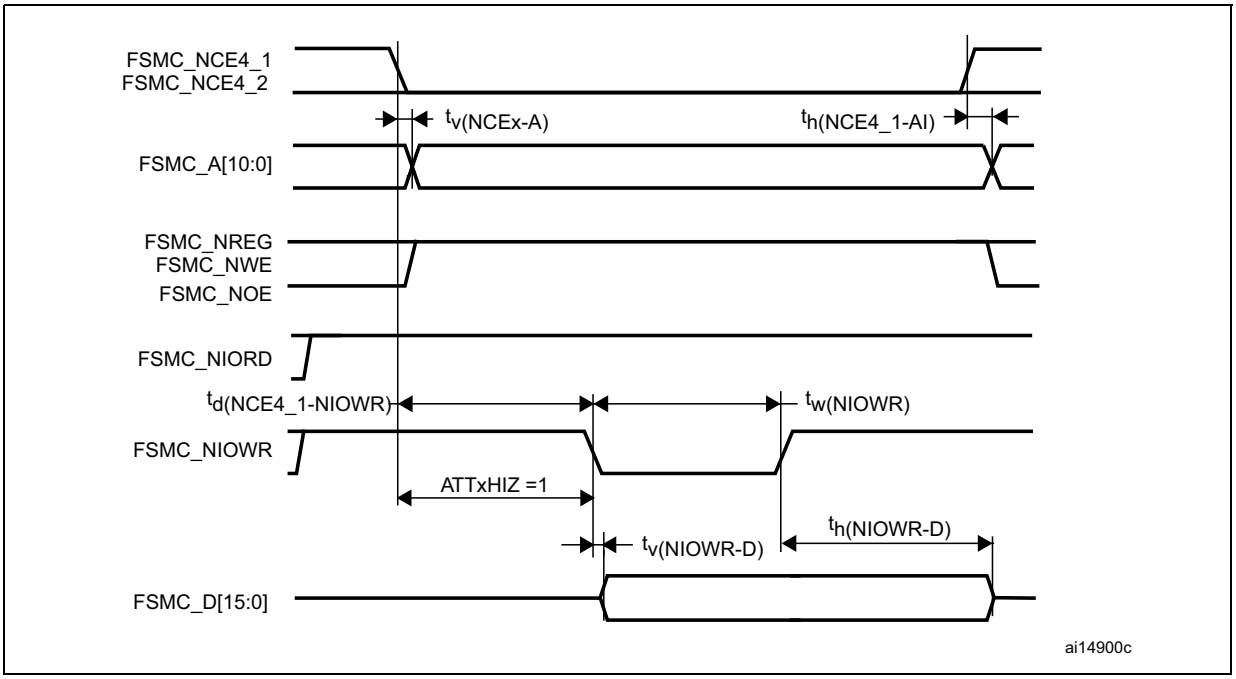



**Table 40. Switching characteristics for PC Card/CF read and write cycles in attribute/common space**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{v(NCEx-A)}$ | FSMC_NCEx low to FSMC_Ay valid | - | 0 | ns |
| $t_{h(NCEx-AI)}$ | FSMC_NCEx high to FSMC_Ax invalid | 0 | - | |
| $t_{d(NREG-NCEx)}$ | FSMC_NCEx low to FSMC_NREG valid | - | 2 | |
| $t_{h(NCEx-NREG)}$ | FSMC_NCEx high to FSMC_NREG invalid | $t_{HCLK}$ + 4 | - | |
| $t_{d(NCEx\_NWE)}$ | FSMC_NCEx low to FSMC_NWE low | - | $5t_{HCLK}$ + 1 | |
| $t_{d(NCEx\_NOE)}$ | FSMC_NCEx low to FSMC_NOE low | - | $5t_{HCLK}$ + 1 | |
| $t_{w(NOE)}$ | FSMC_NOE low width | $8t_{HCLK}$ - 0.5 | $8t_{HCLK}$ + 1 | |
| $t_{d(NOE-NCEx}$ | FSMC_NOE high to FSMC_NCEx high | $5t_{HCLK}$ - 0.5 | - | |
| $t_{su(D-NOE)}$ | FSMC_D[15:0] valid data before FSMC_NOE high | 32 | - | |
| $t_{h(NOE-D)}$ | FSMC_NOE high to FSMC_D[15:0] invalid | $t_{HCLK}$ | - | |
| $t_{w(NWE)}$ | FSMC_NWE low width | $8t_{HCLK}$ – 1 | $8t_{HCLK}$ + 4 | |
| $t_{d(NWE\_NCEx)}$ | FSMC_NWE high to FSMC_NCEx high | $5t_{HCLK}$ + 1.5 | - | |
| $t_{d(NCEx-NWE)}$ | FSMC_NCEx low to FSMC_NWE low | - | $5t_{HCLK}$ + 1 | |
| $t_{v(NWE-D)}$ | FSMC_NWE low to FSMC_D[15:0] valid | - | 0 | |
| $t_{h(NWE-D)}$ | FSMC_NWE high to FSMC_D[15:0] invalid | $11t_{HCLK}$ | - | |
| $t_{d(D-NWE)}$ | FSMC_D[15:0] valid before FSMC_NWE high | $13t_{HCLK}$ + 2.5 | - | |

## 5.3.14 I/O port characteristics

### General input/output characteristics

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under the conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

**Table 49. I/O static characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Standard IO input low level voltage | - | –0.3 | - | 0.28*($V_{DD}$-2 V)+0.8 V | V |
| | IO FT(1) input low level voltage | | –0.3 | - | 0.32*($V_{DD}$-2 V)+0.75 V | V |
| $V_{IH}$ | Standard IO input high level voltage | - | 0.41*($V_{DD}$-2 V)+1.3 V | - | $V_{DD}$+0.3 | V |
| | IO FT(1) input high level voltage | $V_{DD}$ > 2 V | 0.42*($V_{DD}$-2 V)+1 V | - | 5.5 | V |
| | | $V_{DD} \leq$ 2 V | | | 5.2 | |
| $V_{hys}$ | Standard IO Schmitt trigger voltage hysteresis(2) | - | 200 | - | - | mV |
| | IO FT Schmitt trigger voltage hysteresis(2) | | 5% $V_{DD}$(3) | - | - | mV |
| $I_{lkg}$ | Input leakage current (4) | $V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os | - | - | ±1 | µA |
| | | $V_{IN}$= 5 V, I/O FT | - | - | 3 | |
| $R_{PU}$ | Weak pull-up equivalent resistor(5) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $R_{PD}$ | Weak pull-down equivalent resistor(5) | $V_{IN} = V_{DD}$ | 30 | 40 | 50 | kΩ |
| $C_{IO}$ | I/O pin capacitance | - | - | 5 | - | pF |

1. FT = Five-volt tolerant. In order to sustain a voltage higher than $V_{DD}$+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 40* and *Figure 41* for standard I/Os, and in *Figure 42* and *Figure 43* for 5 V tolerant I/Os.

**Figure 40. Standard I/O input characteristics - CMOS port**

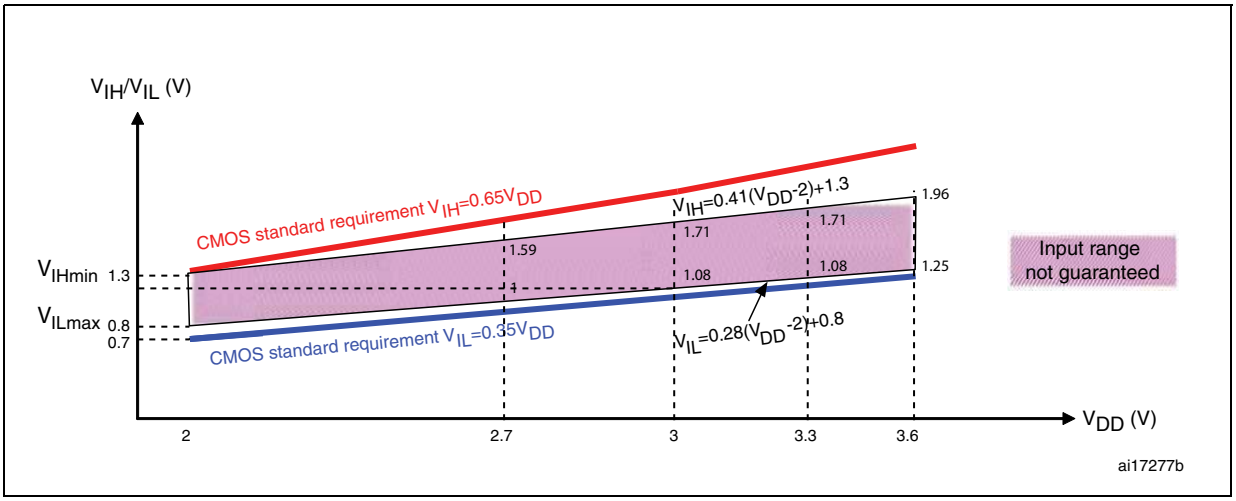



**Figure 41. Standard I/O input characteristics - TTL port**

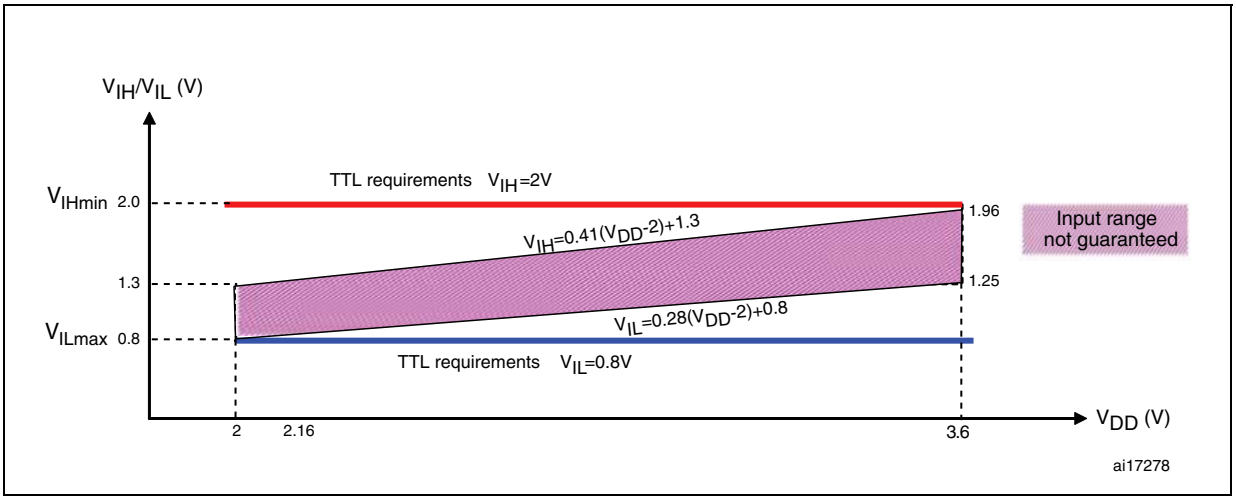



**Figure 42. 5 V tolerant I/O input characteristics - CMOS port**

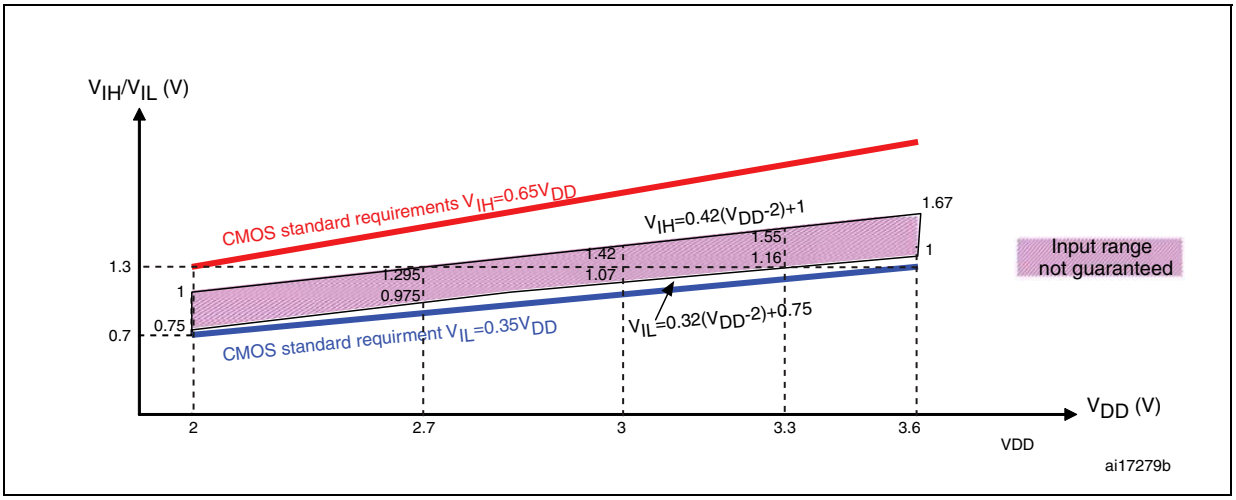
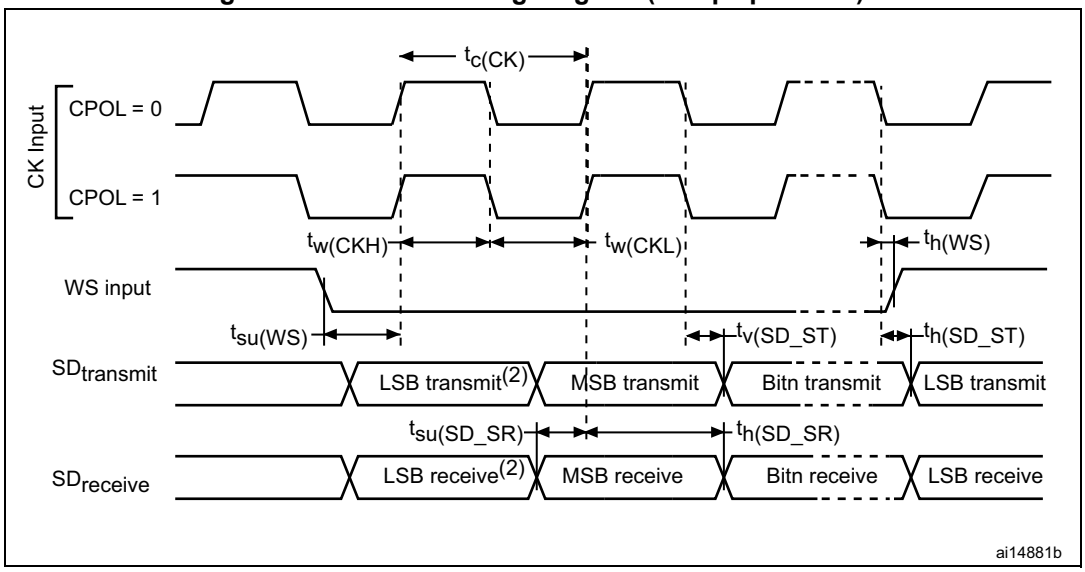
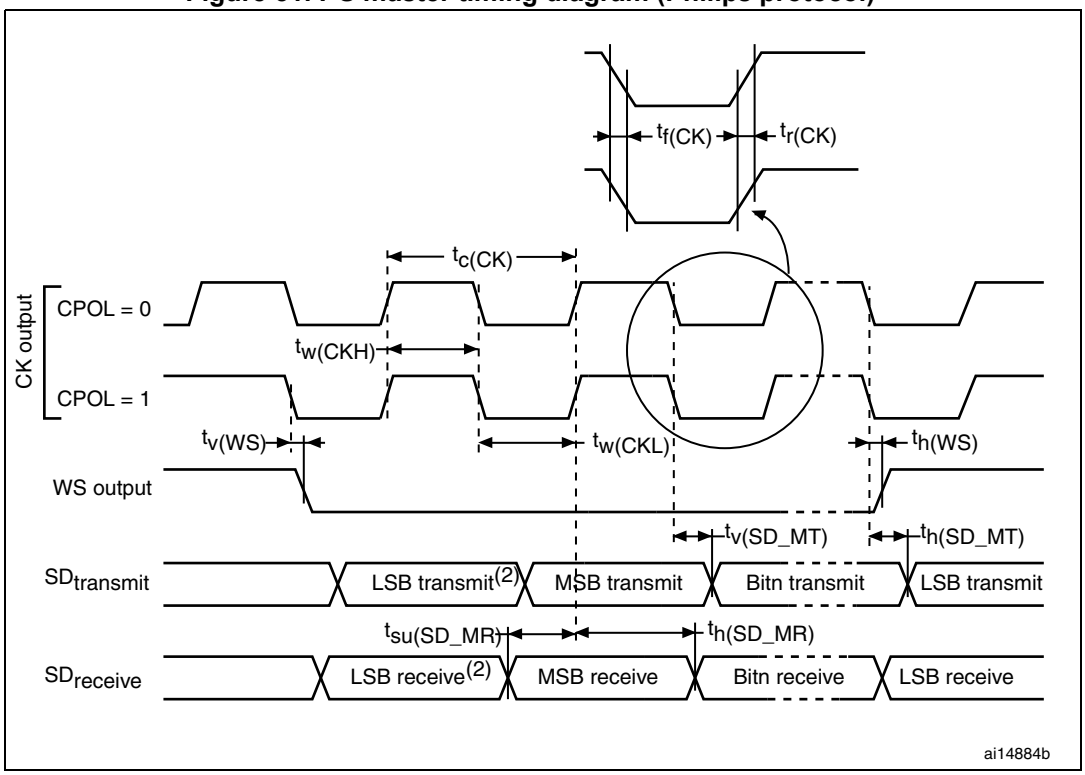


**Figure 50. I²S slave timing diagram (Philips protocol)(1)**




1. Measurement points are done at CMOS levels: $0.3 \times V_{DD}$ and $0.7 \times V_{DD}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Figure 51. I²S master timing diagram (Philips protocol)(1)**




1. Guaranteed by characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

**Table 58. SD / MMC characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| CMD, D inputs (referenced to CK) | | | | | |
| $t_{ISU}$ | Input setup time | $C_L \leq 30$ pF | 2 | - | ns |
| $t_{IH}$ | Input hold time | $C_L \leq 30$ pF | 0 | - | |
| CMD, D outputs (referenced to CK) in MMC and SD HS mode | | | | | |
| $t_{OV}$ | Output valid time | $C_L \leq 30$ pF | - | 6 | ns |
| $t_{OH}$ | Output hold time | $C_L \leq 30$ pF | 0 | - | |
| **CMD, D outputs (referenced to CK) i**n SD default mode(1) | | | | | |
| $t_{OVD}$ | Output valid default time | $C_L \leq 30$ pF | - | 7 | ns |
| $t_{OHD}$ | Output hold default time | $C_L \leq 30$ pF | 0.5 | - | |

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

## USB characteristics

The USB interface is USB-IF certified (Full Speed).

**Table 59. USB startup time**

| Symbol | Parameter | Max | Unit |
|---|---|---|---|
| $t_{STARTUP}$(1) | USB transceiver startup time | 1 | µs |

1. Guaranteed by design, not tested in production.

2. Guaranteed by design, not tested in production.
3. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Section 3: Pinouts and pin descriptions* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 62*.

**Equation 1: $R_{AIN}$ max formula**

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 63. $R_{AIN}$ max for $f_{ADC}$ = 14 MHz(1)**

| $T_s$ (cycles) | $t_S$ (µs) | $R_{AIN}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | NA |
| 239.5 | 17.1 | NA |

1. Guaranteed by design, not tested in production.

**Table 64. ADC accuracy - limited test conditions(1)(2)**

| Symbol | Parameter | Test conditions | Typ | Max(3) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 56 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 3 V to 3.6 V $T_A$ = 25 °C Measurements made after ADC calibration $V_{REF+} = V_{DDA}$ | ±1.3 | ±2 | LSB |
| EO | Offset error | | ±1 | ±1.5 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±0.7 | ±1 | |
| EL | Integral linearity error | | ±0.8 | ±1.5 | |

1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.14* does not affect the ADC accuracy.
3. Guaranteed by characterization results, not tested in production.

# 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

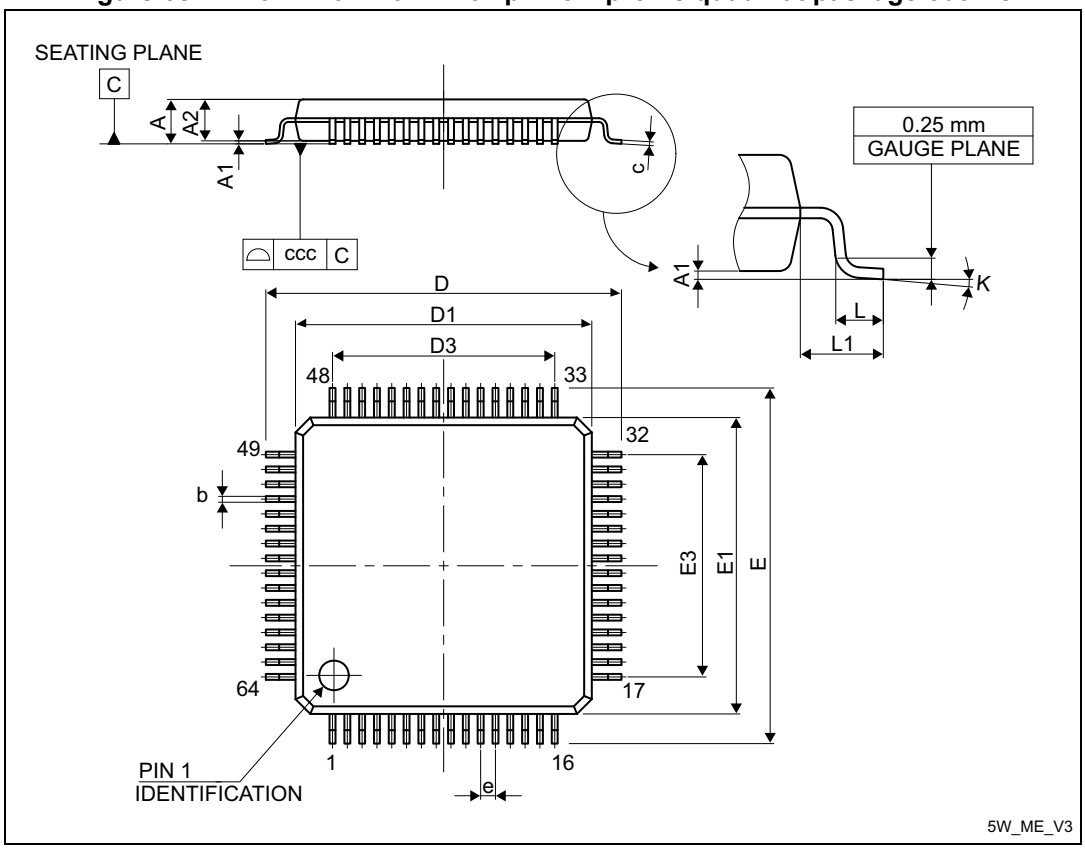
**Table 69. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches[1] | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| D1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| D3 | - | 17.500 | - | - | 0.6890 | - |
| E | 21.800 | 22.000 | 22.200 | 0.8583 | 0.8661 | 0.8740 |
| E1 | 19.800 | 20.000 | 20.200 | 0.7795 | 0.7874 | 0.7953 |
| E3 | - | 17.500 | - | - | 0.6890 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

## 6.4 LQFP64 package information

**Figure 68. LFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline**




1. Drawing is not in scale.

**Table 71. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |

### 6.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 73: STM32F103xF and STM32F103xG ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xF and STM32F103xG at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

#### Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 82 °C (measured according to JESD51-2), $I_{DDmax}$ = 50 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V and maximum 8 I/Os used at the same time in output at low level with $I_{OL}$ = 20 mA, $V_{OL}$= 1.3 V

$P_{INTmax}$ = 50 mA × 3.5 V= 175 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: $P_{INTmax}$ = 175 mW and $P_{IOmax}$ = 272 mW:

$P_{Dmax}$ = 175 + 272 = 447 mW

Thus: $P_{Dmax}$ = 447 mW

Using the values obtained in *Table 72* $T_{Jmax}$ is calculated as follows:

– For LQFP100, 46 °C/W

$T_{Jmax}$ = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < $T_J$ < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 73: STM32F103xF and STM32F103xG ordering information scheme*).

#### Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature $T_J$ remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax}$ = 115 °C (measured according to JESD51-2), $I_{DDmax}$ = 20 mA, $V_{DD}$ = 3.5 V, maximum 20 I/Os used at the same time in output at low level with $I_{OL}$ = 8 mA, $V_{OL}$= 0.4 V

$P_{INTmax}$ = 20 mA × 3.5 V= 70 mW

$P_{IOmax}$ = 20 × 8 mA × 0.4 V = 64 mW

This gives: $P_{INTmax}$ = 70 mW and $P_{IOmax}$ = 64 mW:

$P_{Dmax}$ = 70 + 64 = 134 mW

Thus: $P_{Dmax}$ = 134 mW