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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	51
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rft6tr

2.3.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

2.3.12 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to VDDA is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

2.3.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic and advanced-control timers TIMx, DAC, I^2S, SDIO and ADC.

2.3.17 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.18 Timers and watchdogs

The XL-density STM32F103xF/G performance line devices include up to two advanced-control timers, up to ten general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. STM32F103xF and STM32F103xG timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9, TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM10, TIM11 TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Table 6. FSMC pin definition (continued)

Pins	FSMC					LQFP100(1)
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11	-	-	A16	A16	CLE	Yes
PD12	-	-	A17	A17	ALE	Yes
PD13	-	-	A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2	-	-	A12	-	-	-
PG3	-	-	A13	-	-	-
PG4	-	-	A14	-	-	-
PG5	-	-	A15	-	-	-
PG6	-	-	-	-	INT2	-
PG7	-	-	-	-	INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3	-	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	-	NE1	NE1	NCE2	Yes
PG9	-	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	NCE4_2	-	-	-	-
PG12	-	-	NE4	NE4	-	-
PG13	-	-	A24	A24	-	-
PG14	-	-	A25	A25	-	-
PB7	-	-	NADV	NADV	-	Yes
PE0	-	-	NBL0	NBL0	-	Yes
PE1	-	-	NBL1	NBL1	-	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

5.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 11* are derived from tests performed under the ambient temperature condition summarized in *Table 10*.

Table 11. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	¥	µs/V
	V_{DD} fall time rate		20	¥	

5.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 12* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 12. Embedded reset and power control block characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (rising edge)	2.1	2.18	2.26	V
		PLS[2:0]=000 (falling edge)	2	2.08	2.16	V
		PLS[2:0]=001 (rising edge)	2.19	2.28	2.37	V
		PLS[2:0]=001 (falling edge)	2.09	2.18	2.27	V
		PLS[2:0]=010 (rising edge)	2.28	2.38	2.48	V
		PLS[2:0]=010 (falling edge)	2.18	2.28	2.38	V
		PLS[2:0]=011 (rising edge)	2.38	2.48	2.58	V
		PLS[2:0]=011 (falling edge)	2.28	2.38	2.48	V
		PLS[2:0]=100 (rising edge)	2.47	2.58	2.69	V
		PLS[2:0]=100 (falling edge)	2.37	2.48	2.59	V
		PLS[2:0]=101 (rising edge)	2.57	2.68	2.79	V
		PLS[2:0]=101 (falling edge)	2.47	2.58	2.69	V
		PLS[2:0]=110 (rising edge)	2.66	2.78	2.9	V
		PLS[2:0]=110 (falling edge)	2.56	2.68	2.8	V
		PLS[2:0]=111 (rising edge)	2.76	2.88	3	V
		PLS[2:0]=111 (falling edge)	2.66	2.78	2.9	V
$V_{PVDhyst}$[2]	PVD hysteresis	-	-	100	-	mV
$V_{POR/PDR}$	Power on/power down reset threshold	Falling edge	1.8[1]	1.88	1.96	V
		Rising edge	1.84	1.92	2.0	V
$V_{PDRhyst}$[2]	PDR hysteresis	-	-	40	-	mV
$T_{RSTTEMPO}$[2]	Reset temporization	-	1	2.5	4.5	mS

1. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
2. Guaranteed by design, not tested in production.

Table 14. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	68	69	mA
			48 MHz	51	51	
			36 MHz	41	41	
			24 MHz	29	30	
			16 MHz	22	22.5	
			8 MHz	12.5	14	
		External clock(2), all peripherals disabled	72 MHz	39	39	
			48 MHz	29.5	30	
			36 MHz	24	24.5	
			24 MHz	17.5	19	
			16 MHz	14	15	
			8 MHz	8.5	10.5	

1. Guaranteed by characterization results, not tested in production.
2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

Table 15. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	65	65.5	mA
			48 MHz	46.5	47	
			36 MHz	37	37	
			24 MHz	26.5	27	
			16 MHz	19	20	
			8 MHz	11.5	13	
		External clock(2), all peripherals disabled	72 MHz	34.5	36	
			48 MHz	25	26	
			36 MHz	20.5	21	
			24 MHz	15	16	
			16 MHz	11	13	
			8 MHz	7.5	9	

1. Guaranteed by characterization results, not tested in production at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when $f_{HCLK} > 8$ MHz.

5.3.8 PLL characteristics

The parameters given in *Table 28* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 28. PLL characteristics

Symbol	Parameter	Value			Unit
		Min	Typ	Max(1)	
f_{PLL_IN}	PLL input clock(2)	1	8.0	25	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	72	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

1. Guaranteed by characterization results, not tested in production.
2. Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

5.3.9 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

Table 29. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max(1)	Unit
t_{prog}	16-bit programming time	T_A = –40 to +105 °C	40	52.5	70	µs
t_{ERASE}	Page (2 KB) erase time	T_A = –40 to +105 °C	20	-	40	ms
t_{ME}	Mass erase time	T_A = –40 to +105 °C	20	-	40	ms
I_{DD}	Supply current	Read mode f_{HCLK} = 72 MHz with 2 wait states, V_{DD} = 3.3 V	-	-	28	mA
		Write mode f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	7	mA
		Erase mode f_{HCLK} = 72 MHz, V_{DD} = 3.3 V	-	-	5	mA
		Power-down mode / Halt, V_{DD} = 3.0 to 3.6 V	-	-	50	µA
V_{prog}	Programming voltage	-	2	-	3.6	V

1. Guaranteed by design, not tested in production.

Figure 24. Asynchronous multiplexed PSRAM/NOR read waveforms

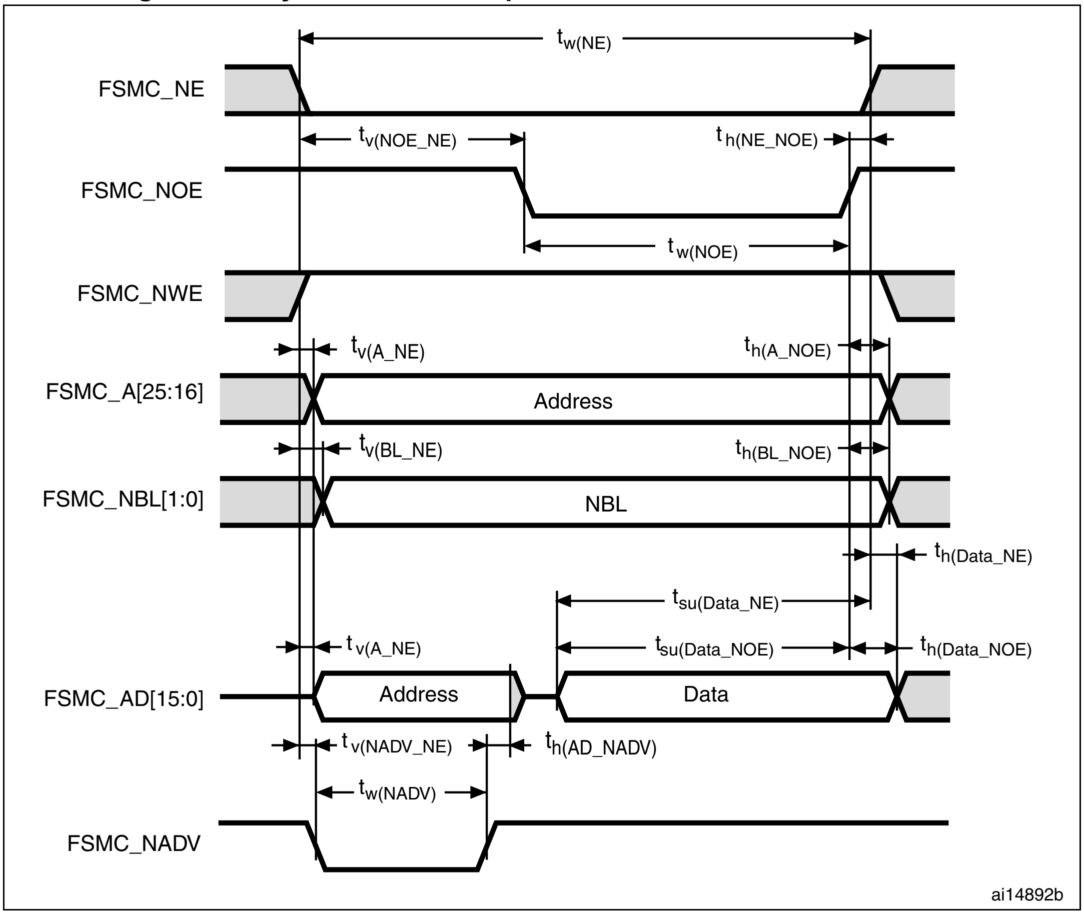
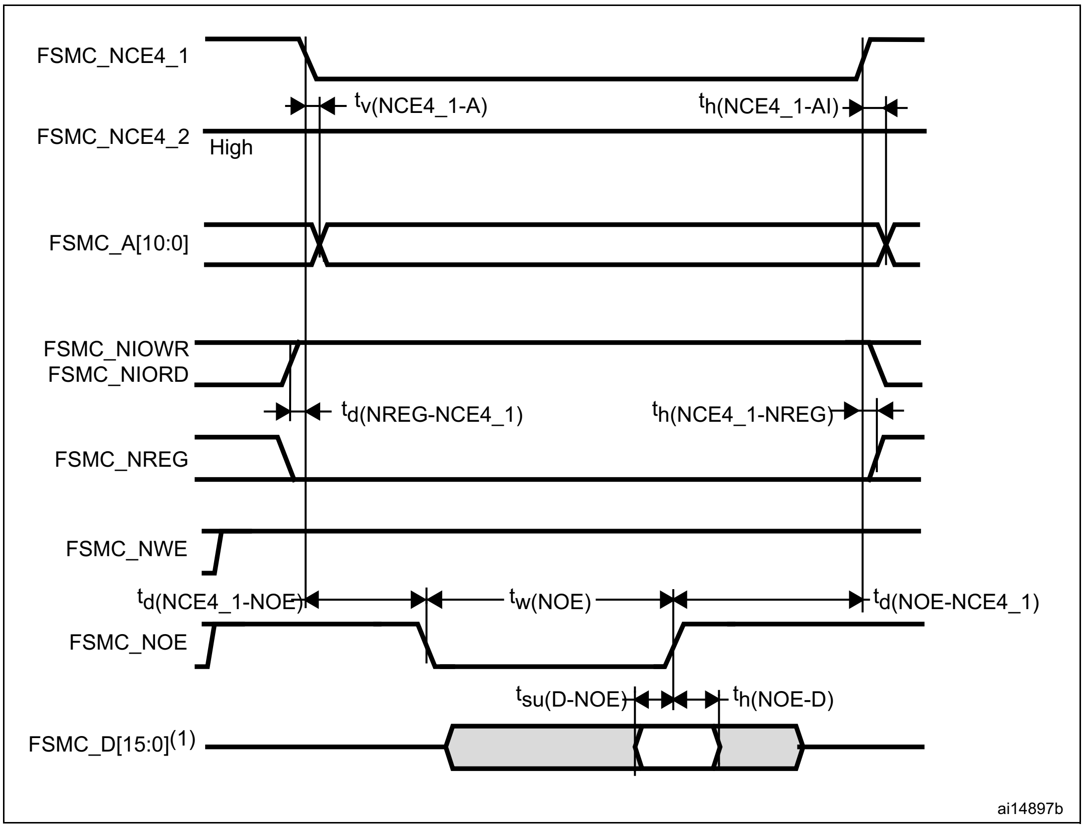


Table 34. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7t_{HCLK} + 0.5$	$7t_{HCLK} + 2$	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK} + 0.5$	$3t_{HCLK} + 1.5$	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK} - 1$	$4t_{HCLK} + 1$	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	0	1	ns
$t_{w(NADV)}$	FSMC_NADV low time	$t_{HCLK} + 0.5$	$t_{HCLK} + 2$	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	t_{HCLK} -2	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0.5	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$4t_{HCLK}$ - 0.5	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$4t_{HCLK}$ - 1	-	ns

Figure 32. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 35. PC Card/CompactFlash controller waveforms for I/O space write access

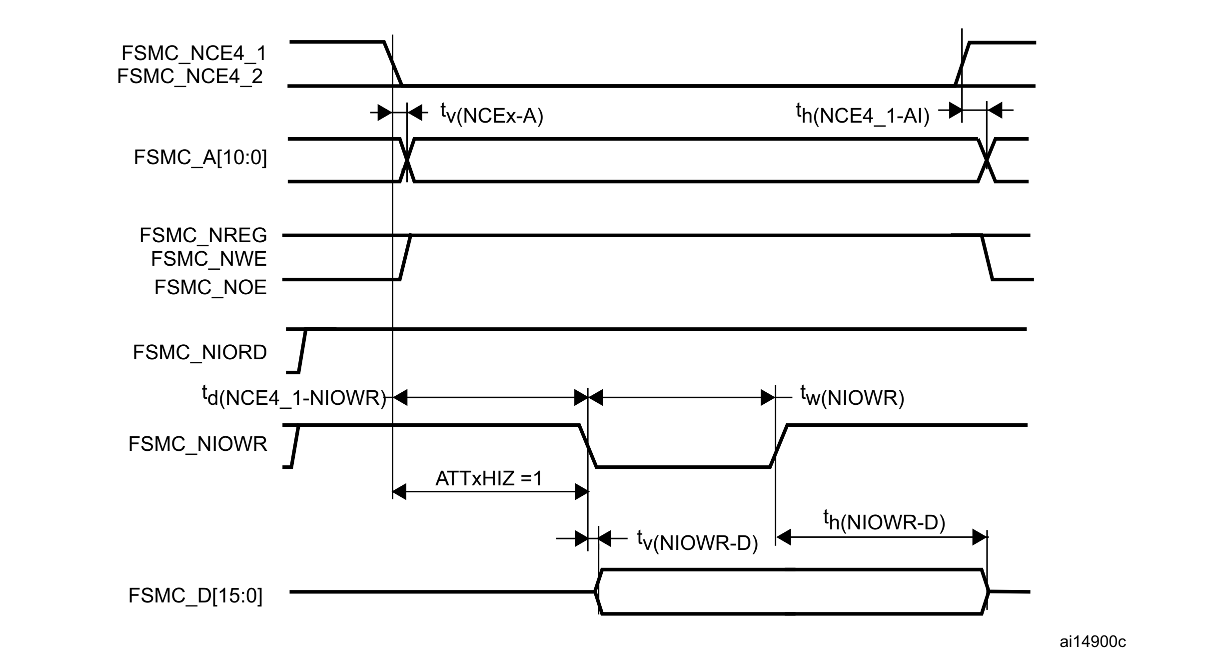


Table 40. Switching characteristics for PC Card/CF read and write cycles in attribute/common space

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FSMC_NCEx low to FSMC_Ay valid	-	0	ns
$t_{h(NCEx-AI)}$	FSMC_NCEx high to FSMC_Ax invalid	0	-	
$t_{d(NREG-NCEx)}$	FSMC_NCEx low to FSMC_NREG valid	-	2	
$t_{h(NCEx-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid	t_{HCLK} + 4	-	
$t_{d(NCEx\_NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5t_{HCLK}$ + 1	
$t_{d(NCEx\_NOE)}$	FSMC_NCEx low to FSMC_NOE low	-	$5t_{HCLK}$ + 1	
$t_{w(NOE)}$	FSMC_NOE low width	$8t_{HCLK}$ - 0.5	$8t_{HCLK}$ + 1	
$t_{d(NOE-NCEx}$	FSMC_NOE high to FSMC_NCEx high	$5t_{HCLK}$ - 0.5	-	
$t_{su(D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	32	-	
$t_{h(NOE-D)}$	FSMC_NOE high to FSMC_D[15:0] invalid	t_{HCLK}	-	
$t_{w(NWE)}$	FSMC_NWE low width	$8t_{HCLK}$ – 1	$8t_{HCLK}$ + 4	
$t_{d(NWE\_NCEx)}$	FSMC_NWE high to FSMC_NCEx high	$5t_{HCLK}$ + 1.5	-	
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5t_{HCLK}$ + 1	
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$11t_{HCLK}$	-	
$t_{d(D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	$13t_{HCLK}$ + 2.5	-	

Table 43. Switching characteristics for NAND Flash write cycles[1]

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$3t_{HCLK}$	$3t_{HCLK}$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$2t_{HCLK} + 2$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3t_{HCLK} + 1.5$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK} + 8$	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$2t_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$2t_{HCLK}$	-	ns

1. C_L = 15 pF.

Figure 40. Standard I/O input characteristics - CMOS port

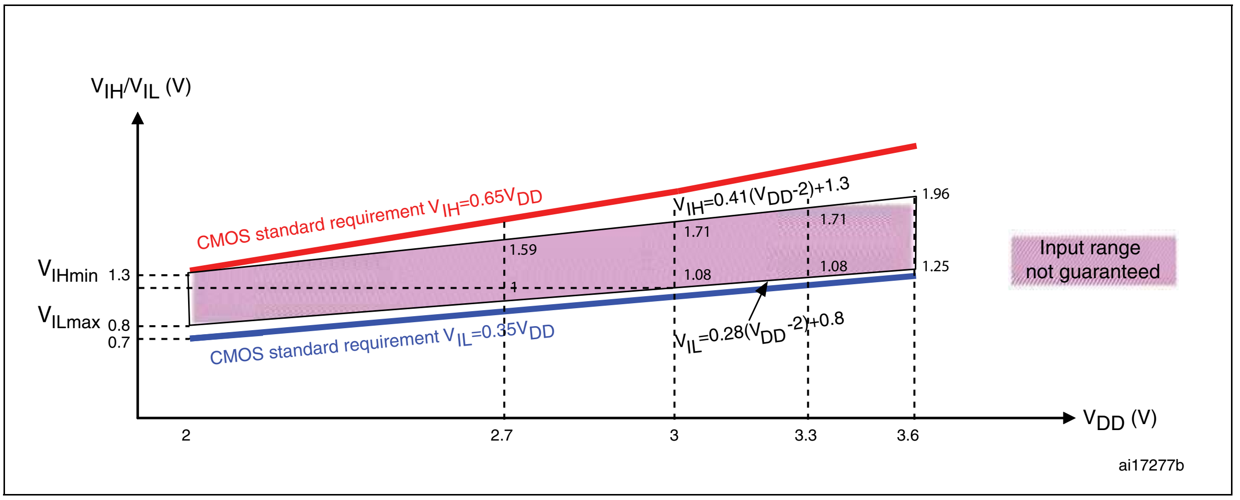


Figure 41. Standard I/O input characteristics - TTL port

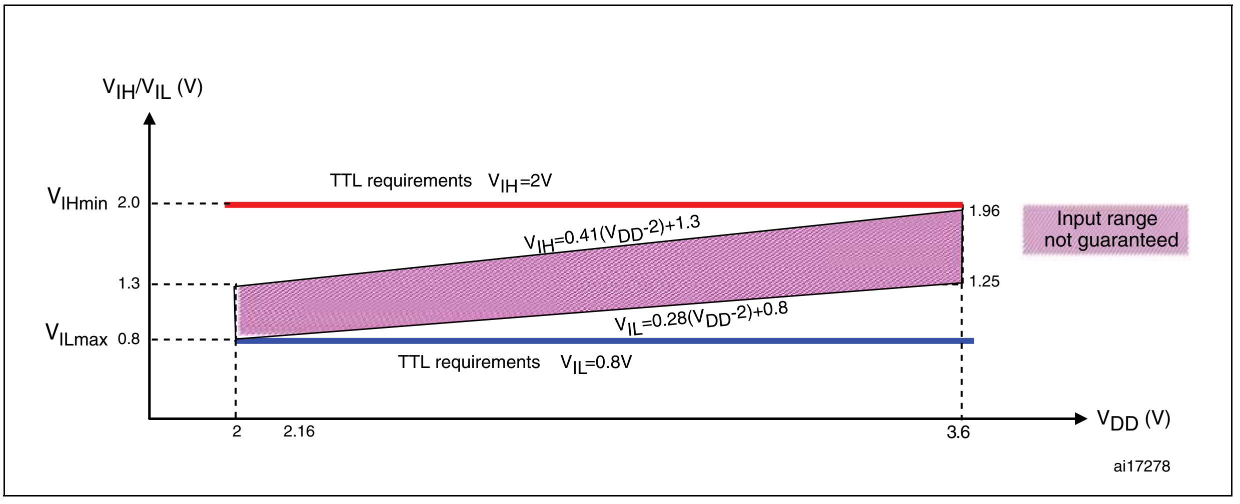
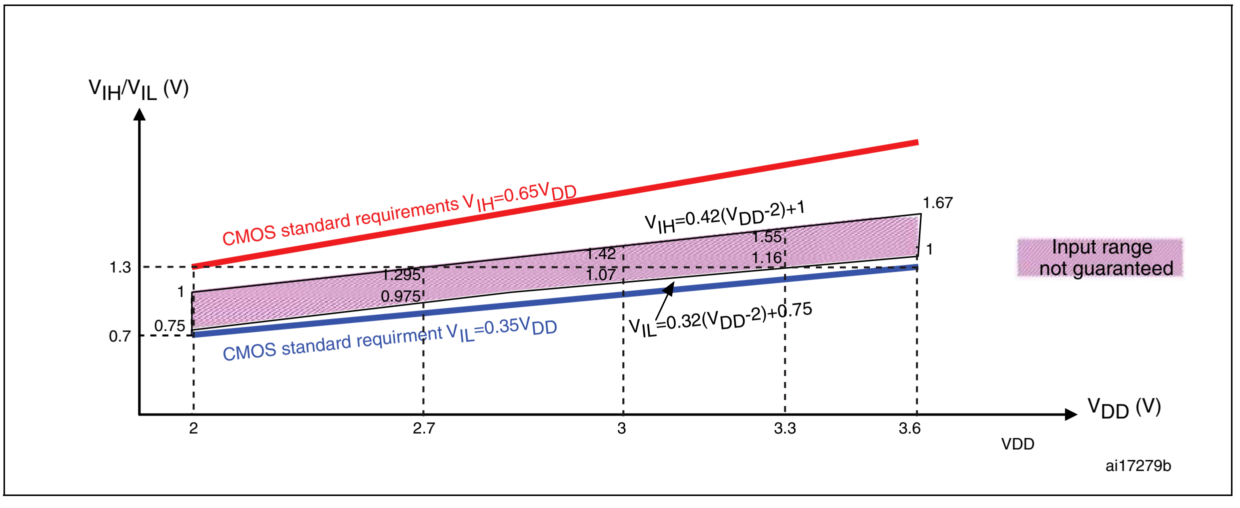


Figure 42. 5 V tolerant I/O input characteristics - CMOS port



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 44* and *Table 51*, respectively.

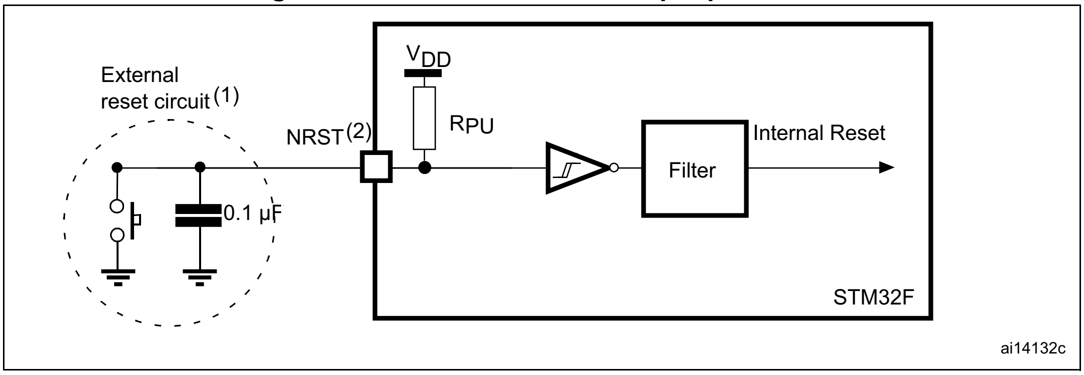
Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 51. I/O AC characteristics[(1)]

MODEx[1:0] bit value[(1)]	Symbol	Parameter	Conditions	Min	Max	Unit
10	$f_{max(IO)out}$	Maximum frequency[(2)]	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	2	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	125[(3)]	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	125[(3)]	
01	$f_{max(IO)out}$	Maximum frequency[(2)]	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	10	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 50 pF, V_{DD} = 2 V to 3.6 V	-	25[(3)]	ns
	$t_{r(IO)out}$	Output low to high level rise time		-	25[(3)]	
11	$F_{max(IO)out}$	Maximum frequency[(2)]	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	50	MHz
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	30	MHz
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	20	MHz
	$t_{f(IO)out}$	Output high to low level fall time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5[(3)]	ns
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8[(3)]	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12[(3)]	
	$t_{r(IO)out}$	Output low to high level rise time	C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V	-	5[(3)]	
			C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V	-	8[(3)]	
			C_L = 50 pF, V_{DD} = 2 V to 2.7 V	-	12[(3)]	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller	-	10	-	ns

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 44*.
3. Guaranteed by design, not tested in production.

Figure 45. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 52*. Otherwise the reset will not be taken into account by the device.

5.3.16 TIM timer characteristics

The parameters given in *Table 53* are guaranteed by design.

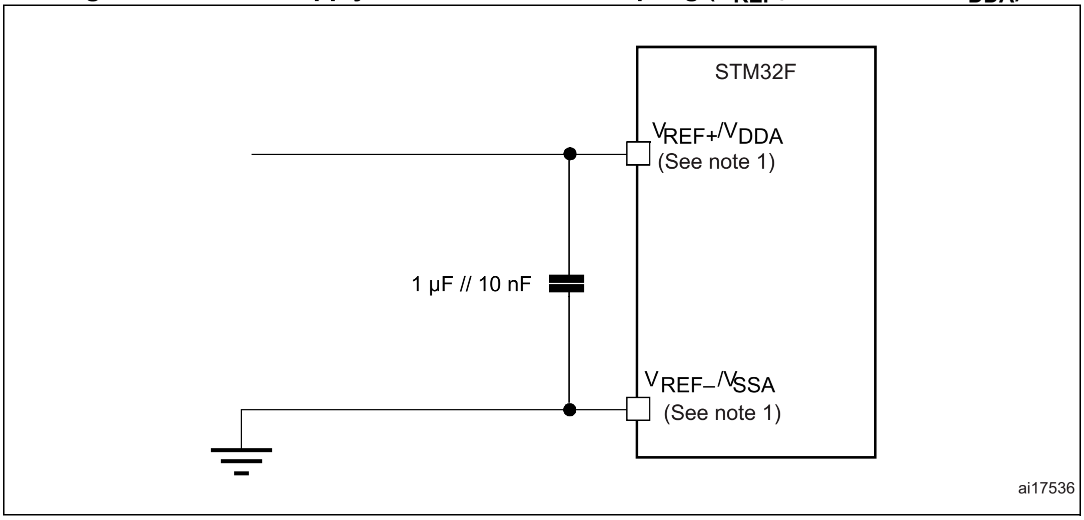
Refer to *Section 5.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 53. TIMx[1] characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.6	s

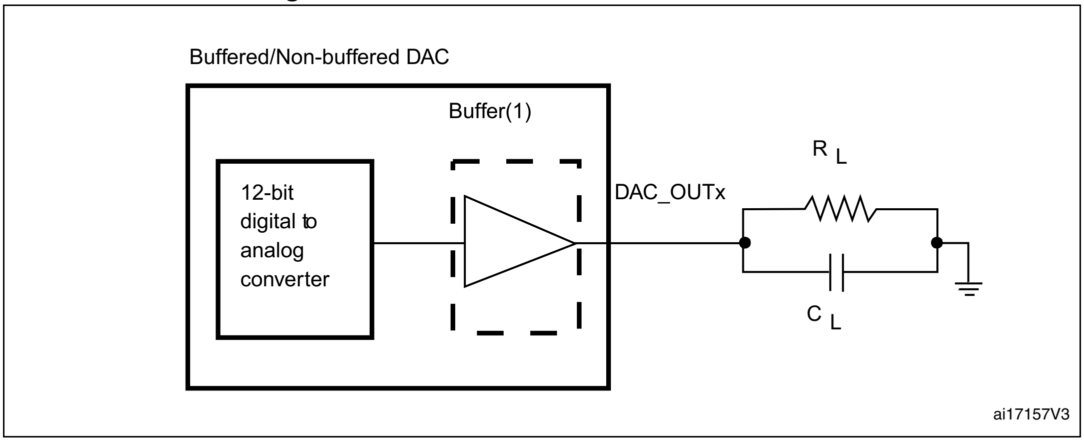
1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

Figure 58. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Figure 59. 12-bit buffered /non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

5.3.21 Temperature sensor characteristics

Table 67. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	4.0	4.3	4.6	mV/°C
V_{25}(1)	Voltage at 25 °C	1.34	1.43	1.52	V
t_{START}(2)	Startup time	4	-	10	µs
T_{S_temp}(3)(2)	ADC sampling time when reading the temperature	-	-	17.1	µs

1. Guaranteed on characterization results, not tested in production.
2. Guaranteed by design, not tested in production.
3. Shortest sampling time can be determined in the application by multiple iterations.

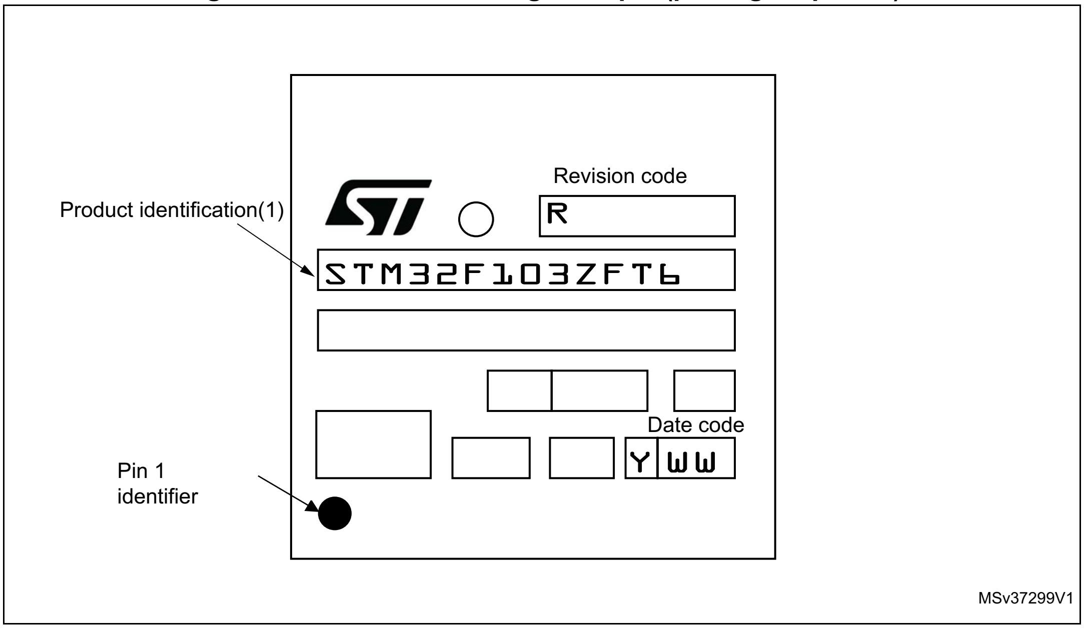
6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Device marking for LQFP144 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 64. LQFP144 marking example (package top view)



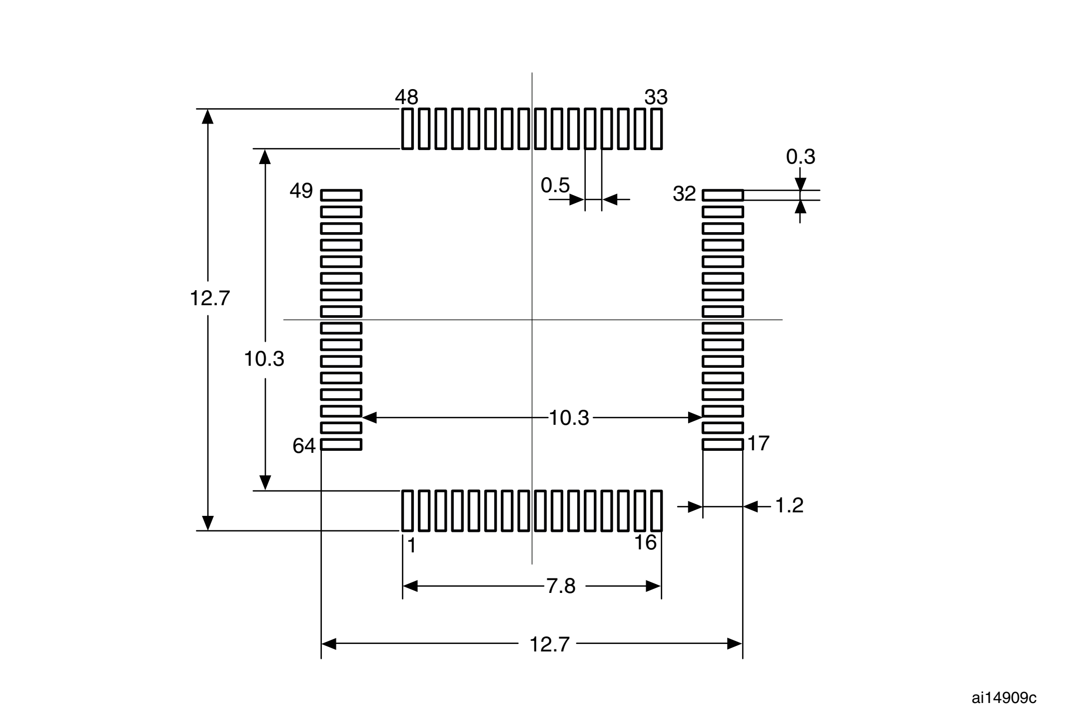
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 71. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 69. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



1. Dimensions are in millimeters.

Table 74. Document revision history

Date	Revision	Changes
18-Jan-2012	3	*Asynchronous waveforms and timings*: added notes about t_{HCLK} clock period and FSMC_BusTurnAroundDuration; updated conditions, modified *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings*, *Table 32: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings*, *Table 34: Asynchronous multiplexed PSRAM/NOR read timings*, and *Table 35: Asynchronous multiplexed PSRAM/NOR write timings*; added *Table 33: Asynchronous multiplexed read timings*. *Synchronous waveforms and timings*: updated *Figure 27: Synchronous multiplexed PSRAM write timings*; updated *Table 36: Synchronous multiplexed NOR/PSRAM read timings*, *Table 37: Synchronous multiplexed PSRAM write timings*, *Table 38: Synchronous non-multiplexed NOR/PSRAM read timings*, and *Table 39: Synchronous non-multiplexed PSRAM write timings*. *PC Card/CompactFlash controller waveforms and timings*: updated *Figure 35: PC Card/CompactFlash controller waveforms for I/O space write access*; split switching characteristics into *Table 40: Switching characteristics for PC Card/CF read and write cycles in attribute/common space* and *Table 41: Switching characteristics for PC Card/CF read and write cycles in I/O space*, modified values, and removed footnote concerning preliminary values. *NAND controller waveforms and timings*: updated conditions, split switching characteristics into *Table 42: Switching characteristics for NAND Flash read cycles* and *Table 43: Switching characteristics for NAND Flash write cycles*, and values modified. *Section 5.3.14: I/O port characteristics*: updated footnote*1* of *Table 49: I/O static characteristics*; updated *Output driving current*. *Table 50: Output voltage characteristics*: swapped “TTL and “CMOS” ports in the conditions column. *Table 54: I^2C characteristics*: updated footnote *2*. Updated *Table 58: SD / MMC characteristics*. *Table 62: ADC characteristics*: updated footnote *1*. *Table 64: ADC accuracy - limited test conditions*: updated footnote *3*. *Table 67: TS characteristics*: updated footnote *1*.

Table 74. Document revision history

Date	Revision	Changes
15-May-2015	4	Added document status on first page. Replace DAC1_OUT/DAC2_OUT by DAC_OUT1/DAC_OUT2, and updated TIM5 in *Figure 1: STM32F103xF and STM32F103xG performance line block diagram on page 12*. Replaced USBDP/USBDM by USB_DP/USB_DM in the whole document. Updated notes related to electrical values guaranteed by characterization results. Updated *Table 20: Peripheral current consumption*. Updated *Table 36: Synchronous multiplexed NOR/PSRAM read timings* to *Table 39: Synchronous non-multiplexed PSRAM write timings*(added FSMC_NWAIT timings). Updated *Figure 26: Synchronous multiplexed NOR/PSRAM read timings on page 73* and *Figure 28: Synchronous non-multiplexed NOR/PSRAM read timings on page 77* and *Figure 35: PC Card/CompactFlash controller waveforms for I/O space write access on page 83*. Updated CDM class in *Table 46: ESD absolute maximum ratings*. Updated *Figure 44: I/O AC characteristics definition on page 96* and *Figure 45: Recommended NRST pin protection on page 97*. Updated *Figure 49: SPI timing diagram - master mode(1) on page 96*. Modified note 3 in *Table 56: SPI characteristics*. *Section : I2C interface characteristics*: Updated introduction, updated *Table 54: I^2C characteristics* and *Figure 46: I^2C bus AC waveforms and measurement circuit on page 99*. Modified note 2 in *Table 64: ADC accuracy - limited test conditions*, *Figure 55: ADC accuracy characteristics on page 110* and *Figure 56: Typical connection diagram using the ADC on page 111*. Updated *Figure 57: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) on page 111* and *Figure 58: Power supply and reference decoupling (V_{REF+} connected to V_{DDA}) on page 112*. Updated I_{DDA} description and Offset comment in *Table 66: DAC characteristics*. Updated *Section 6.1: LFBGA144 package information* and added *Section : Device marking for LFBGA144 package*. Updated *Section 6.2: LQFP144 package information* and added *Section : Device marking for LQFP144 package*. Updated *Section 6.3: LQFP100 package information* and added *Section : Device marking for LQFP100 package*. Updated *Section 6.4: LQFP64 package information* and added *Section : Device marking for LQFP64 package*.