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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 51 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 16x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-LQFP |
| Supplier Device Package | 64-LQFP (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103rgt7 |

# List of figures

### 2.3.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

### 2.3.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

### 2.3.12 Power supply schemes

- $V_{DD}$ = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to VDDA is 2.4 V when the ADC or DAC is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

### 2.3.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and $V_{PVD}$.

### 2.3.21 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

### 2.3.22 Inter-integrated sound ($I^2S$)

Two standard $I^2S$ interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the $I^2S$ interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

### 2.3.23 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.
The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

### 2.3.24 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

### 2.3.25 Universal serial bus (USB)

The STM32F103xF and STM32F103xG performance line embed a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

### 2.3.26 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

| Pins | | | | Pin name | Type(1) | I / O level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|---|
| LFBGA144 | LQFP64 | LQFP100 | LQFP144 | | | | | Default | Remap |
| E11 | 40 | 66 | 99 | PC9 | I/O | FT | PC9 | TIM8_CH4 / SDIO_D1 | TIM3_CH4 |
| E12 | 41 | 67 | 100 | PA8 | I/O | FT | PA8 | USART1_CK / TIM1_CH1(7) / MCO | - |
| D12 | 42 | 68 | 101 | PA9 | I/O | FT | PA9 | USART1_TX(7) / TIM1_CH2(7) | - |
| D11 | 43 | 69 | 102 | PA10 | I/O | FT | PA10 | USART1_RX(7) / TIM1_CH3(7) | - |
| C12 | 44 | 70 | 103 | PA11 | I/O | FT | PA11 | USART1_CTS / USB_DM / CAN_RX(7) / TIM1_CH4(7) | - |
| B12 | 45 | 71 | 104 | PA12 | I/O | FT | PA12 | USART1_RTS / USB_DP / CAN_TX(7) / TIM1_ETR(7) | - |
| A12 | 46 | 72 | 105 | PA13 | I/O | FT | JTMS-SWDIO | - | PA13 |
| C11 | - | 73 | 106 | Not connected | | | | | |
| G9 | 47 | 74 | 107 | $V_{SS\_2}$ | S | | $V_{SS\_2}$ | - | - |
| F9 | 48 | 75 | 108 | $V_{DD\_2}$ | S | | $V_{DD\_2}$ | - | - |
| A11 | 49 | 76 | 109 | PA14 | I/O | FT | JTCK-SWCLK | - | PA14 |
| A10 | 50 | 77 | 110 | PA15 | I/O | FT | JTDI | SPI3_NSS / I2S3_WS | TIM2_CH1_ETR PA15/ SPI1_NSS |
| B11 | 51 | 78 | 111 | PC10 | I/O | FT | PC10 | UART4_TX / SDIO_D2 | USART3_TX |
| B10 | 52 | 79 | 112 | PC11 | I/O | FT | PC11 | UART4_RX / SDIO_D3 | USART3_RX |
| C10 | 53 | 80 | 113 | PC12 | I/O | FT | PC12 | UART5_TX / SDIO_CK | USART3_CK |
| E10 | - | 81 | 114 | PD0 | I/O | FT | PD0 | FSMC_D2(9) | CAN_RX |
| D10 | - | 82 | 115 | PD1 | I/O | FT | PD1 | FSMC_D3(9) | CAN_TX |
| E9 | 54 | 83 | 116 | PD2 | I/O | FT | PD2 | TIM3_ETR / UART5_RX / SDIO_CMD | - |
| D9 | - | 84 | 117 | PD3 | I/O | FT | PD3 | FSMC_CLK | USART2_CTS |
| C9 | - | 85 | 118 | PD4 | I/O | FT | PD4 | FSMC_NOE | USART2_RTS |
| B9 | - | 86 | 119 | PD5 | I/O | FT | PD5 | FSMC_NWE | USART2_TX |
| E7 | - | - | 120 | $V_{SS\_10}$ | S | | $V_{SS\_10}$ | - | - |
| F7 | - | - | 121 | $V_{DD\_10}$ | S | | $V_{DD\_10}$ | - | - |
| A8 | - | 87 | 122 | PD6 | I/O | FT | PD6 | FSMC_NWAIT | USART2_RX |

**Table 5. STM32F103xF and STM32F103xG pin definitions (continued)**

| Pins | | | | Pin name | Type(1) | I / O level(2) | Main function(3) (after reset) | Alternate functions(4) | |
|---|---|---|---|---|---|---|---|---|---|
| LFBGA144 | LQFP64 | LQFP100 | LQFP144 | | | | | Default | Remap |
| A9 | - | 88 | 123 | PD7 | I/O | FT | PD7 | FSMC_NE1 / FSMC_NCE2 | USART2_CK |
| E8 | - | - | 124 | PG9 | I/O | FT | PG9 | FSMC_NE2 / FSMC_NCE3 | - |
| D8 | - | - | 125 | PG10 | I/O | FT | PG10 | FSMC_NCE4_1 / FSMC_NE3 | - |
| C8 | - | - | 126 | PG11 | I/O | FT | PG11 | FSMC_NCE4_2 | - |
| B8 | - | - | 127 | PG12 | I/O | FT | PG12 | FSMC_NE4 | - |
| D7 | - | - | 128 | PG13 | I/O | FT | PG13 | FSMC_A24 | - |
| C7 | - | - | 129 | PG14 | I/O | FT | PG14 | FSMC_A25 | - |
| E6 | - | - | 130 | $V_{SS\_11}$ | S | | $V_{SS\_11}$ | - | - |
| F6 | - | - | 131 | $V_{DD\_11}$ | S | | $V_{DD\_11}$ | - | - |
| B7 | - | - | 132 | PG15 | I/O | FT | PG15 | - | - |
| A7 | 55 | 89 | 133 | PB3 | I/O | FT | JTDO | SPI3_SCK / I2S3_CK/ | PB3/TRACESWO TIM2_CH2 / SPI1_SCK |
| A6 | 56 | 90 | 134 | PB4 | I/O | FT | NJTRST | SPI3_MISO | PB4/ TIM3_CH1 SPI1_MISO |
| B6 | 57 | 91 | 135 | PB5 | I/O | | PB5 | I2C1_SMBA / SPI3_MOSI / I2S3_SD | TIM3_CH2 / SPI1_MOSI |
| C6 | 58 | 92 | 136 | PB6 | I/O | FT | PB6 | I2C1_SCL(8)/ TIM4_CH1(8) | USART1_TX |
| D6 | 59 | 93 | 137 | PB7 | I/O | FT | PB7 | I2C1_SDA(8) / FSMC_NADV / TIM4_CH2(8) | USART1_RX |
| D5 | 60 | 94 | 138 | BOOT0 | I | | BOOT0 | - | - |
| C5 | 61 | 95 | 139 | PB8 | I/O | FT | PB8 | TIM4_CH3(8) / SDIO_D4 / TIM10_CH1 | I2C1_SCL/ CAN_RX |
| B5 | 62 | 96 | 140 | PB9 | I/O | FT | PB9 | TIM4_CH4(8) / SDIO_D5 / TIM11_CH1 | I2C1_SDA / CAN_TX |
| A5 | - | 97 | 141 | PE0 | I/O | FT | PE0 | TIM4_ETR / FSMC_NBL0 | - |
| A4 | - | 98 | 142 | PE1 | I/O | FT | PE1 | FSMC_NBL1 | - |
| E5 | 63 | 99 | 143 | $V_{SS\_3}$ | S | | $V_{SS\_3}$ | - | - |
| F5 | 64 | 100 | 144 | $V_{DD\_3}$ | S | | $V_{DD\_3}$ | - | - |

1. I = input, O = output, S = supply.
2. FT = 5 V tolerant.
3. Function availability depends on the chosen device.

**Table 6. FSMC pin definition**

| Pins | FSMC | | | | | LQFP100[1] |
|---|---|---|---|---|---|---|
| | CF | CF/IDE | NOR/PSRAM/ SRAM | NOR/PSRAM Mux | NAND 16 bit | |
| PE2 | - | - | A23 | A23 | - | Yes |
| PE3 | - | - | A19 | A19 | - | Yes |
| PE4 | - | - | A20 | A20 | - | Yes |
| PE5 | - | - | A21 | A21 | - | Yes |
| PE6 | - | - | A22 | A22 | - | Yes |
| PF0 | A0 | A0 | A0 | - | - | - |
| PF1 | A1 | A1 | A1 | - | - | - |
| PF2 | A2 | A2 | A2 | - | - | - |
| PF3 | A3 | - | A3 | - | - | - |
| PF4 | A4 | - | A4 | - | - | - |
| PF5 | A5 | - | A5 | - | - | - |
| PF6 | NIORD | NIORD | | - | - | - |
| PF7 | NREG | NREG | | - | - | - |
| PF8 | NIOWR | NIOWR | | - | - | - |
| PF9 | CD | CD | | - | - | - |
| PF10 | INTR | INTR | | - | - | - |
| PF11 | NIOS16 | NIOS16 | | - | - | - |
| PF12 | A6 | - | A6 | - | - | - |
| PF13 | A7 | - | A7 | - | - | - |
| PF14 | A8 | - | A8 | - | - | - |
| PF15 | A9 | - | A9 | - | - | - |
| PG0 | A10 | - | A10 | - | - | - |
| PG1 | - | - | A11 | - | - | - |
| PE7 | D4 | D4 | D4 | DA4 | D4 | Yes |
| PE8 | D5 | D5 | D5 | DA5 | D5 | Yes |
| PE9 | D6 | D6 | D6 | DA6 | D6 | Yes |
| PE10 | D7 | D7 | D7 | DA7 | D7 | Yes |
| PE11 | D8 | D8 | D8 | DA8 | D8 | Yes |
| PE12 | D9 | D9 | D9 | DA9 | D9 | Yes |
| PE13 | D10 | D10 | D10 | DA10 | D10 | Yes |
| PE14 | D11 | D11 | D11 | DA11 | D11 | Yes |
| PE15 | D12 | D12 | D12 | DA12 | D12 | Yes |
| PD8 | D13 | D13 | D13 | DA13 | D13 | Yes |

### 5.3.4 Embedded reference voltage

The parameters given in *Table 13* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 10*.

**Table 13. Embedded internal reference voltage**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Internal reference voltage | –40 °C < $T_A$ < +105 °C | 1.16 | 1.20 | 1.26 | V |
| | | –40 °C < $T_A$ < +85 °C | 1.16 | 1.20 | 1.24 | V |
| $T_{S\_vrefint}$(1) | ADC sampling time when reading the internal reference voltage | - | - | 5.1 | 17.1(2) | µs |
| $V_{RERINT}$(2) | Internal reference voltage spread over the temperature range | $V_{DD}$ = 3 V ±10 mV | - | - | 10 | mV |
| $T_{Coeff}$(2) | Temperature coefficient | - | - | - | 100 | ppm/°C |

1. Shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design, not tested in production.

### 5.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.
The current consumption is measured as described in *Figure 11: Current consumption measurement scheme*.
All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to Dhrystone 2.1 code.

#### Maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at $V_{DD}$ or $V_{SS}$ (no load)
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the $f_{HCLK}$ frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHz and 2 wait states above)
- Prefetch in ON (reminder: this bit must be set before clock setting and bus prescaling)
- When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/2$, $f_{PCLK2} = f_{HCLK}$

The parameters given in *Table 14*, *Table 15* and *Table 16* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 10*.

**Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Max(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(2), all peripherals enabled | 72 MHz | 47.5 | 48.5 | mA |
| | | | 48 MHz | 34 | 35 | |
| | | | 36 MHz | 27.5 | 27.5 | |
| | | | 24 MHz | 20 | 20.5 | |
| | | | 16 MHz | 15 | 16 | |
| | | | 8 MHz | 9 | 11 | |
| | | External clock(2), all peripherals disabled | 72 MHz | 9.5 | 11.2 | |
| | | | 48 MHz | 7.7 | 9.5 | |
| | | | 36 MHz | 6.9 | 8.5 | |
| | | | 24 MHz | 5.9 | 7.8 | |
| | | | 16 MHz | 5.4 | 7.2 | |
| | | | 8 MHz | 4.7 | 6.4 | |

1. Guaranteed by characterization results, not tested in production at $V_{DD}$ max, $f_{HCLK}$ max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 19. Typical current consumption in Sleep mode, code running from Flash or RAM**

| Symbol | Parameter | Conditions | $f_{HCLK}$ | Typ(1) | | Unit |
|---|---|---|---|---|---|---|
| | | | | All peripherals enabled(2) | All peripherals disabled | |
| $I_{DD}$ | Supply current in Sleep mode | External clock(3) | 72 MHz | 32.5 | 7 | mA |
| | | | 48 MHz | 23 | 5 | |
| | | | 36 MHz | 17.7 | 4 | |
| | | | 24 MHz | 12.2 | 3.1 | |
| | | | 16 MHz | 8.4 | 2.3 | |
| | | | 8 MHz | 4.6 | 1.5 | |
| | | | 4 MHz | 3 | 1.3 | |
| | | | 2 MHz | 2.15 | 1.25 | |
| | | | 1 MHz | 1.7 | 1.2 | |
| | | | 500 kHz | 1.5 | 1.15 | |
| | | | 125 kHz | 1.35 | 1.15 | |
| | | Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency | 64 MHz | 28.7 | 5.7 | |
| | | | 48 MHz | 22 | 4.4 | |
| | | | 36 MHz | 17 | 3.35 | |
| | | | 24 MHz | 11.6 | 2.3 | |
| | | | 16 MHz | 7.7 | 1.6 | |
| | | | 8 MHz | 3.9 | 0.8 | |
| | | | 4 MHz | 2.3 | 0.7 | |
| | | | 2 MHz | 1.5 | 0.6 | |
| | | | 1 MHz | 1.1 | 0.5 | |
| | | | 500 kHz | 0.9 | 0.5 | |
| | | | 125 kHz | 0.7 | 0.5 | |

1. Typical values are measures at $T_A$ = 25 °C, $V_{DD}$ = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when $f_{HCLK}$ > 8 MHz.

**Table 32. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $3t_{HCLK}$ + 0.5 | $3t_{HCLK}$ + 1.5 | ns |
| $t_{v(NWE\_NE)}$ | FSMC_NEx low to FSMC_NWE low | $t_{HCLK}$ + 0.5 | $t_{HCLK}$ + 1.5 | ns |
| $t_{w(NWE)}$ | FSMC_NWE low time | $t_{HCLK}$ – 0.5 | $t_{HCLK}$ + 1 | ns |
| $t_{h(NE\_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $t_{HCLK}$ – 0.5 | - | ns |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | ns |
| $t_{h(A\_NWE)}$ | Address hold time after FSMC_NWE high | $t_{HCLK}$ | - | ns |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 1.5 | ns |
| $t_{h(BL\_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $t_{HCLK}$ – 1.5 | - | ns |
| $t_{v(Data\_NE)}$ | FSMC_NEx low to Data valid | - | $t_{HCLK}$ | ns |
| $t_{h(Data\_NWE)}$ | Data hold time after FSMC_NWE high | $t_{HCLK}$ | - | ns |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | - | 0 | ns |
| $t_{w(NADV)}$ | FSMC_NADV low time | - | $t_{HCLK}$ + 1.5 | ns |

1. $C_L$ = 15 pF.

**Table 33. Asynchronous multiplexed read timings**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NE)}$ | FSMC_NE low time | $7t_{HCLK}$ + 0.5 | $7t_{HCLK}$ + 2 | ns |
| $t_{v(NOE\_NE)}$ | FSMC_NEx low to FSMC_NOE low | $3t_{HCLK}$ + 0.5 | $3t_{HCLK}$ + 1.5 | |
| $t_{w(NOE)}$ | FSMC_NOE low time | $4t_{HCLK}$ – 1 | $4t_{HCLK}$ + 1 | |
| $t_{h(NE\_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | 0.5 | - | |
| $t_{v(A\_NE)}$ | FSMC_NEx low to FSMC_A valid | - | 0 | |
| $t_{v(NADV\_NE)}$ | FSMC_NEx low to FSMC_NADV low | 0 | 1 | |
| $t_{w(NADV)}$ | FSMC_NADV low time | $t_{HCLK}$ + 0.5 | $t_{HCLK}$ + 2 | |
| $t_{h(AD\_NADV)}$ | FSMC_AD (address) valid hold time after FSMC NADV high | $t_{HCLK}$ | - | |
| $t_{h(A\_NOE)}$ | Address hold time after FSMC_NOE high | $t_{HCLK}$ – 2 | - | |
| $t_{h(BL\_NOE)}$ | FSMC_BL time after FSMC_NOE high | 0.5 | - | |
| $t_{v(BL\_NE)}$ | FSMC_NEx low to FSMC_BL valid | - | 0 | |
| $t_{su(Data\_NE)}$ | Data to FSMC_NEx high setup time | $4t_{HCLK}$ – 0.5 | - | |
| $t_{su(Data\_NOE)}$ | Data to FSMC_NOE high setup time | $4t_{HCLK}$ – 1 | - | |
| $t_{h(Data\_NE)}$ | Data hold time after FSMC_NEx high | 0 | - | |
| $t_{h(Data\_NOE)}$ | Data hold time after FSMC_NOE high | 0 | - | |

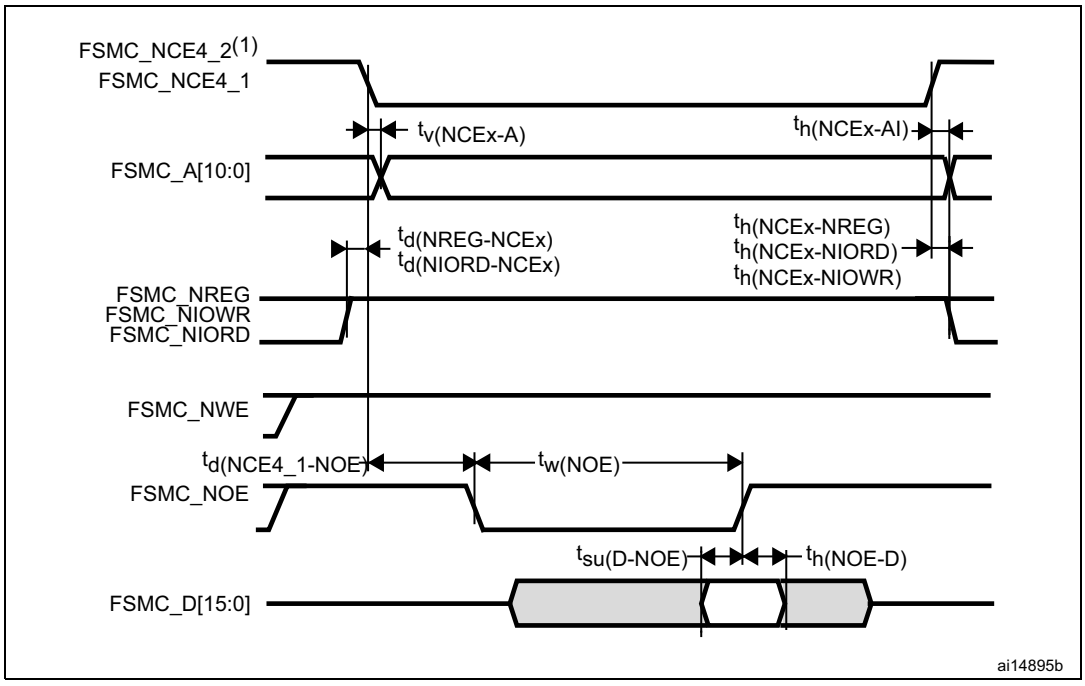
1. $C_L$ = 15 pF.

## PC Card/CompactFlash controller waveforms and timings

*Figure 30* through *Figure 35* represent synchronous waveforms and *Table 42* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

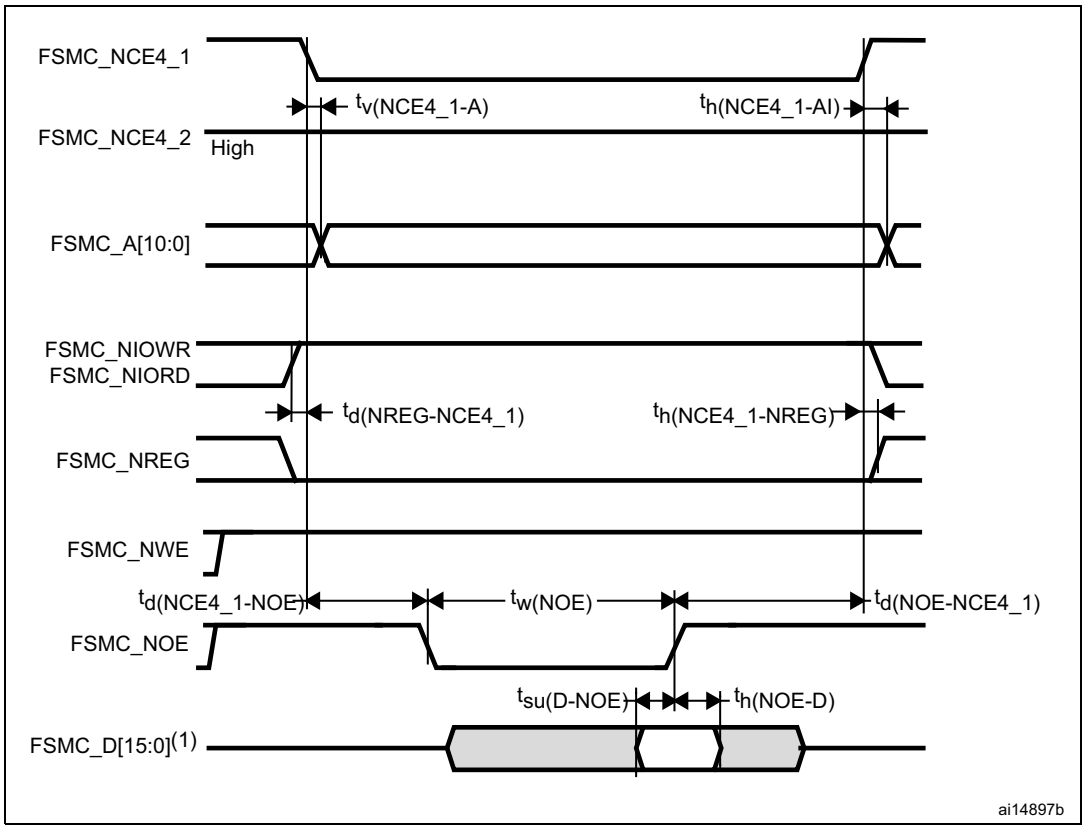
- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

**Figure 30. PC Card/CompactFlash controller waveforms for common memory read access**




1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

**Figure 32. PC Card/CompactFlash controller waveforms for attribute memory read access**




1. Only data bits 0...7 are read (bits 8...15 are disregarded).

**Table 47. Electrical sensitivities**

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

## 5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

### Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

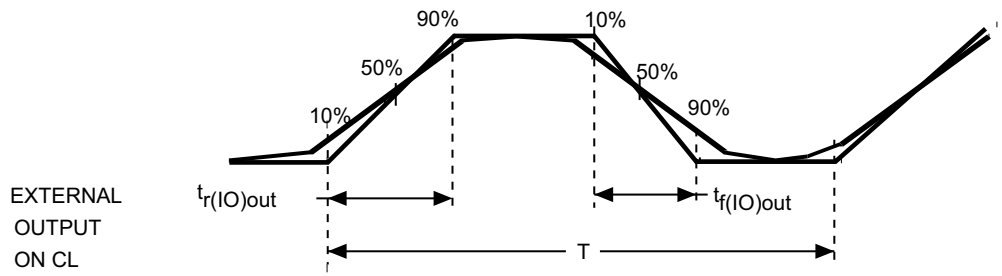
The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 48*

**Table 48. I/O current injection susceptibility**

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13 | -0 | +0 | mA |
| | Injected current on all FT pins | -5 | +0 | |
| | Injected current on any other pin | -5 | +5 | |

**Figure 44. I/O AC characteristics definition**




Maximum frequency is achieved if $(t_r + t_f) \leq (2/3)T$ and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

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## 5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, $R_{PU}$ (see *Table 49*).

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature and $V_{DD}$ supply voltage conditions summarized in *Table 10*.

**Table 52. NRST pin characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$(1) | NRST Input low level voltage | - | –0.5 | - | 0.8 | V |
| $V_{IH(NRST)}$(1) | NRST Input high level voltage | - | 2 | - | $V_{DD}$+0.5 | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | - | - | 200 | - | mV |
| $R_{PU}$ | Weak pull-up equivalent resistor(2) | $V_{IN} = V_{SS}$ | 30 | 40 | 50 | kΩ |
| $V_{F(NRST)}$(1) | NRST Input filtered pulse | - | - | - | 100 | ns |
| $V_{NF(NRST)}$(1) | NRST Input not filtered pulse | - | 300 | - | - | ns |

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

## 5.3.17 Communications interfaces

### I²C interface characteristics

The STM32F103xF, STM32F103xD and STM32F103xGSTM32F103xF and STM32F103xG performance line I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and $V_{DD}$ is disabled, but is still present.

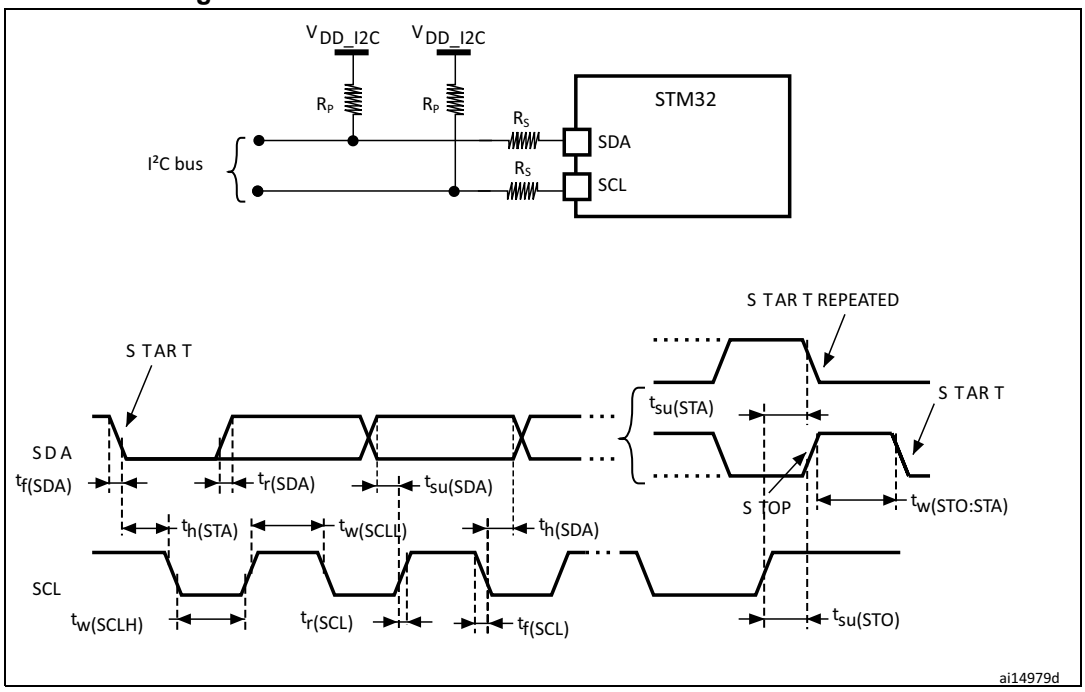
The I²C characteristics are described in *Table 54*. Refer also to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (SDA and SCL).

**Table 54. I²C characteristics**

| Symbol | Parameter | Standard mode I²C(1)(2) | | Fast mode I²C(1)(2) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | - | 1.3 | - | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | - | 0.6 | - | |
| $t_{su(SDA)}$ | SDA setup time | 250 | - | 100 | - | ns |
| $t_{h(SDA)}$ | SDA data hold time | - | 3450(3) | - | 900(3) | |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | - | 1000 | - | 300 | |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | - | 300 | - | 300 | |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | - | 0.6 | - | µs |
| $t_{su(STA)}$ | Repeated Start condition setup time | 4.7 | - | 0.6 | - | |
| $t_{su(STO)}$ | Stop condition setup time | 4.0 | - | 0.6 | - | µs |
| $t_{w(STO:STA)}$ | Stop to Start condition time (bus free) | 4.7 | - | 1.3 | - | µs |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |
| $t_{SP}$ | Pulse width of the spikes that are suppressed by the analog filter for standard and fast mode | 0 | 50(4) | 0 | 50(4) | µs |

1. Guaranteed by design, not tested in production.
2. $f_{PCLK1}$ must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve the fast mode I²C frequencies and it must be a multiple of 10 MHz in order to reach the I2C fast mode maximum clock speed of 400 kHz.
3. The device must internally provide a hold time of at least 300ns for the SDA signal in order to bridge the undefined region on the falling edge of SCL.
4. The minimum width of the spikes filtered by the analog filter is above $t_{SP}$(max).

**Figure 46. I²C bus AC waveforms and measurement circuit**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.
2. Rs: Series protection resistors.
3. Rp: Pull-up resistors.
4. VDD_I2C : I2C bus supply

**Table 55. SCL frequency ($f_{PCLK1}$= 36 MHz.,$V_{DD\_I2C}$ = 3.3 V)(1)(2)**

| $f_{SCL}$ (kHz) | I2C_CCR value |
|---|---|
| | $R_P$ = 4.7 kΩ |
| 400 | 0x801E |
| 300 | 0x8028 |
| 200 | 0x803C |
| 100 | 0x00B4 |
| 50 | 0x0168 |
| 20 | 0x0384 |

1. $R_P$ = External pull-up resistance, $f_{SCL}$ = I²C speed.
2. For speeds around 200 kHz, the tolerance on the achieved speed is of ±5%. For other speed ranges, the tolerance on the achieved speed ±2%. These variations depend on the accuracy of the external components used to design the application.

**Table 57. $I^2S$ characteristics**

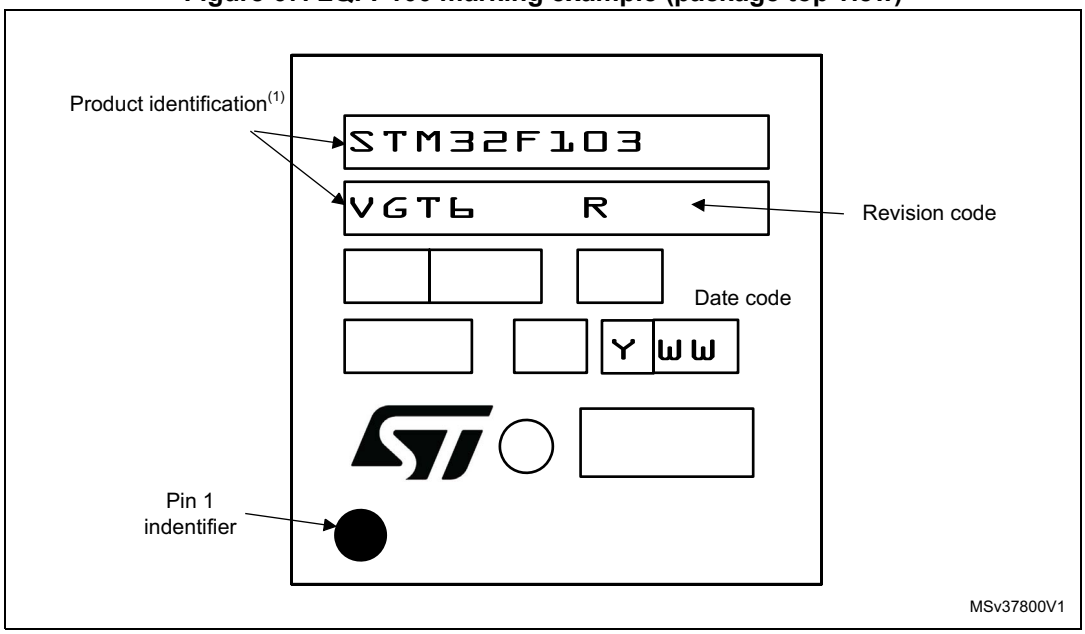
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| DuCy(SCK) | I2S slave input clock duty cycle | Slave mode | | 30 | 70 | % |
| $f_{CK}$<br>$1/t_{c(CK)}$ | $I^2S$ clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | | 1.522 | 1.525 | MHz |
| | | Slave mode | | 0 | 6.5 | |
| $t_{r(CK)}$<br>$t_{f(CK)}$ | $I^2S$ clock rise and fall time | Capacitive load $C_L$ = 50 pF | | - | 8 | ns |
| $t_{v(WS)}$ (1) | WS valid time | Master mode | | 3 | - | |
| $t_{h(WS)}$ (1) | WS hold time | Master mode | I2S2 | 2 | - | |
| | | | I2S3 | 0 | - | |
| $t_{su(WS)}$ (1) | WS setup time | Slave mode | | 4 | - | |
| $t_{h(WS)}$ (1) | WS hold time | Slave mode | | 0 | - | |
| $t_{w(CKH)}$ (1) | CK high and low time | Master $f_{PCLK}$= 16 MHz, audio frequency = 48 kHz | | 312.5 | - | |
| $t_{w(CKL)}$ (1) | | | | 345 | - | |
| $t_{su(SD\_MR)}$ (1) | Data input setup time | Master receiver | I2S2 | 2 | - | |
| | | | I2S3 | 6.5 | - | |
| $t_{su(SD\_SR)}$ (1) | Data input setup time | Slave receiver | | 1.5 | - | |
| $t_{h(SD\_MR)}$ (1)(2) | Data input hold time | Master receiver | | 0 | - | |
| $t_{h(SD\_SR)}$ (1)(2) | | Slave receiver | | 0.5 | - | |
| $t_{v(SD\_ST)}$ (1)(2) | Data output valid time | Slave transmitter (after enable edge) | | - | 18 | |
| $t_{h(SD\_ST)}$ (1) | Data output hold time | Slave transmitter (after enable edge) | | 11 | - | |
| $t_{v(SD\_MT)}$ (1)(2) | Data output valid time | Master transmitter (after enable edge) | | - | 3 | |
| $t_{h(SD\_MT)}$ (1) | Data output hold time | Master transmitter (after enable edge) | | 0 | - | |

1. Guaranteed by design and/or characterization results, not tested in production.
2. Depends on $f_{PCLK}$. For example, if $f_{PCLK}$=8 MHz, then $T_{PCLK}$ = $1/f_{PLCLK}$ =125 ns.

### Device marking for LQFP100 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 67. LQFP100 marking example (package top view)**




1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

**Table 74. Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 15-May-2015 | 4 | Added document status on first page.<br>Replace DAC1_OUT/DAC2_OUT by DAC_OUT1/DAC_OUT2, and updated TIM5 in *Figure 1: STM32F103xF and STM32F103xG performance line block diagram on page 12*.<br>Replaced USBDP/USBDM by USB_DP/USB_DM in the whole document.<br>Updated notes related to electrical values guaranteed by characterization results.<br>Updated *Table 20: Peripheral current consumption*.<br>Updated *Table 36: Synchronous multiplexed NOR/PSRAM read timings* to *Table 39: Synchronous non-multiplexed PSRAM write timings*(added FSMC_NWAIT timings). Updated *Figure 26: Synchronous multiplexed NOR/PSRAM read timings on page 73* and *Figure 28: Synchronous non-multiplexed NOR/PSRAM read timings on page 77* and *Figure 35: PC Card/CompactFlash controller waveforms for I/O space write access on page 83*.<br>Updated CDM class in *Table 46: ESD absolute maximum ratings*.<br>Updated *Figure 44: I/O AC characteristics definition on page 96* and *Figure 45: Recommended NRST pin protection on page 97*.<br>Updated *Figure 49: SPI timing diagram - master mode(1) on page 96*.<br>Modified note 3 in *Table 56: SPI characteristics*.<br>*Section : I2C interface characteristics*: Updated introduction, updated *Table 54: $I^2C$ characteristics* and *Figure 46: $I^2C$ bus AC waveforms and measurement circuit on page 99*.<br>Modified note 2 in *Table 64: ADC accuracy - limited test conditions*, *Figure 55: ADC accuracy characteristics on page 110* and *Figure 56: Typical connection diagram using the ADC on page 111*. Updated *Figure 57: Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$) on page 111* and *Figure 58: Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$) on page 112*.<br>Updated $I_{DDA}$ description and Offset comment in *Table 66: DAC characteristics*.<br>Updated *Section 6.1: LFBGA144 package information* and added *Section : Device marking for LFBGA144 package*.<br>Updated *Section 6.2: LQFP144 package information* and added *Section : Device marking for LQFP144 package*.<br>Updated *Section 6.3: LQFP100 package information* and added *Section : Device marking for LQFP100 package*.<br>Updated *Section 6.4: LQFP64 package information* and added *Section : Device marking for LQFP64 package*. |