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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vft6

List of figures

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103xF and STM32F103xG XL-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xF/G family, please refer to *Section 2.2: Full compatibility throughout the family*.

The XL-density STM32F103xF/G datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website at the following address: *http://infocenter.arm.com*.

2.1 Device overview

The STM32F103xF/G XL-density performance line family offers devices in four different package types: from 64 pins to 144 pins. Depending on the device chosen, different sets of peripherals are included, the description below gives an overview of the complete range of peripherals proposed in this family.

Figure 1 shows the general block diagram of the device family.

Table 2. STM32F103xF and STM32F103xG features and peripheral counts

Peripherals		STM32F103Rx		STM32F103Vx		STM32F103Zx	
Flash memory		768 KB	1 MB	768 KB	1 MB	768 KB	1 MB
SRAM in Kbytes		96		96		96	
FSMC		No		Yes(1)		Yes	
Timers	General-purpose	10					
	Advanced-control	2					
	Basic	2					
Comm	SPI(I^2S)(2)	3(2)					
	I^2C	2					
	USART	5					
	USB	1					
	CAN	1					
	SDIO	1					
GPIOs		51		80		112	
12-bit ADC Number of channels		3 16		3 16		3 21	
12-bit DAC Number of channels		2 2					
CPU frequency		72 MHz					
Operating voltage		2.0 to 3.6 V					
Operating temperatures		Ambient temperatures: –40 to +85 °C /–40 to +105 °C (see *Table 10*) Junction temperature: –40 to + 125 °C (see *Table 10*)					
Package		LQFP64		LQFP100		LQFP144, BGA144	

1. For the LQFP100 package, only FSMC Bank1 and Bank2 are available. Bank1 can only support a multiplexed NOR/PSRAM memory using the NE1 Chip Select. Bank2 can only support a 16- or 8-bit NAND Flash memory using the NCE2 Chip Select. The interrupt line cannot be used since Port G is not available in this package.
2. The SPI2 and SPI3 interfaces give the flexibility to work in an exclusive way in either the SPI mode or the I^2S audio mode.

2.3.5 Embedded SRAM

96 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.6 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F103xF and STM32F103xG performance line family. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- The targeted frequency, f_{CLK}, is HCLK/2, so external access is at 36 MHz when HCLK is at 72 MHz and external access is at 24 MHz when HCLK is at 48 MHz

2.3.7 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.8 Nested vectored interrupt controller (NVIC)

The STM32F103xF and STM32F103xG performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.9 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

2.3.21 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.3.22 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

2.3.23 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.
The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

2.3.24 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

2.3.25 Universal serial bus (USB)

The STM32F103xF and STM32F103xG performance line embed a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

2.3.26 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
E11	40	66	99	PC9	I/O	FT	PC9	TIM8_CH4 / SDIO_D1	TIM3_CH4
E12	41	67	100	PA8	I/O	FT	PA8	USART1_CK / TIM1_CH1(7) / MCO	-
D12	42	68	101	PA9	I/O	FT	PA9	USART1_TX(7) / TIM1_CH2(7)	-
D11	43	69	102	PA10	I/O	FT	PA10	USART1_RX(7) / TIM1_CH3(7)	-
C12	44	70	103	PA11	I/O	FT	PA11	USART1_CTS / USB_DM / CAN_RX(7) / TIM1_CH4(7)	-
B12	45	71	104	PA12	I/O	FT	PA12	USART1_RTS / USB_DP / CAN_TX(7) / TIM1_ETR(7)	-
A12	46	72	105	PA13	I/O	FT	JTMS-SWDIO	-	PA13
C11	-	73	106	Not connected					
G9	47	74	107	V_{SS_2}	S		V_{SS_2}	-	-
F9	48	75	108	V_{DD_2}	S		V_{DD_2}	-	-
A11	49	76	109	PA14	I/O	FT	JTCK-SWCLK	-	PA14
A10	50	77	110	PA15	I/O	FT	JTDI	SPI3_NSS / I2S3_WS	TIM2_CH1_ETR PA15/ SPI1_NSS
B11	51	78	111	PC10	I/O	FT	PC10	UART4_TX / SDIO_D2	USART3_TX
B10	52	79	112	PC11	I/O	FT	PC11	UART4_RX / SDIO_D3	USART3_RX
C10	53	80	113	PC12	I/O	FT	PC12	UART5_TX / SDIO_CK	USART3_CK
E10	-	81	114	PD0	I/O	FT	PD0	FSMC_D2(9)	CAN_RX
D10	-	82	115	PD1	I/O	FT	PD1	FSMC_D3(9)	CAN_TX
E9	54	83	116	PD2	I/O	FT	PD2	TIM3_ETR / UART5_RX / SDIO_CMD	-
D9	-	84	117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
C9	-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
B9	-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
E7	-	-	120	V_{SS_10}	S		V_{SS_10}	-	-
F7	-	-	121	V_{DD_10}	S		V_{DD_10}	-	-
A8	-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX

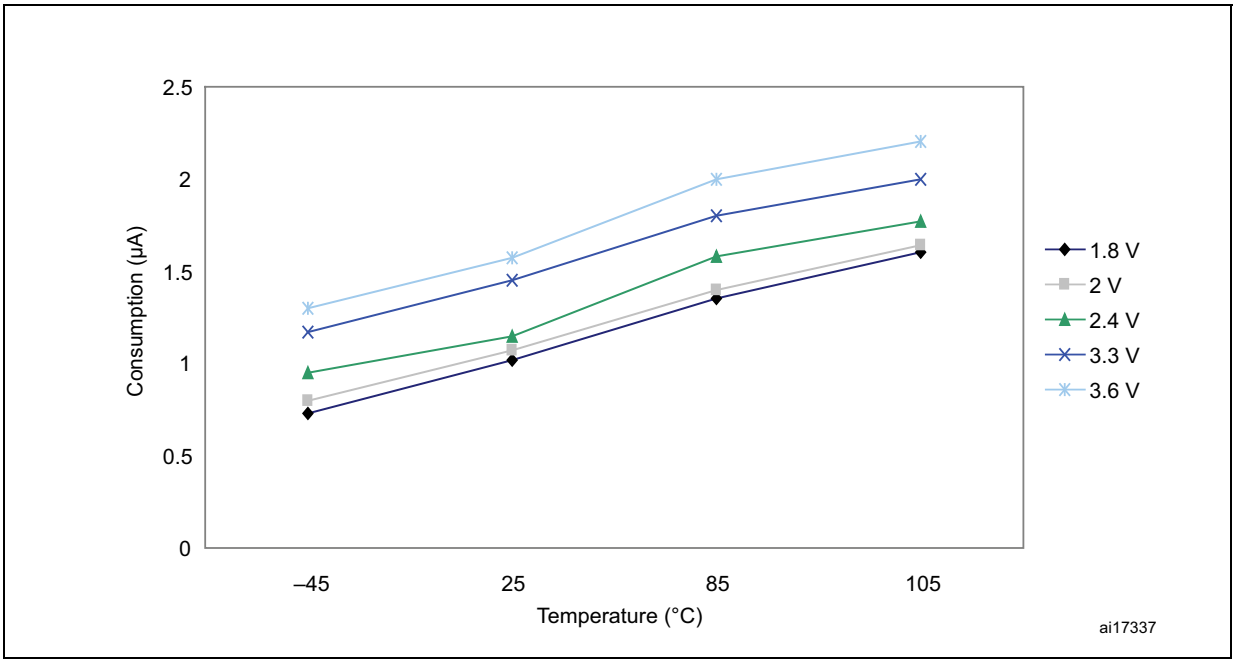
4. If several peripherals share the same I/O pin, to avoid conflict between these alternate functions only one peripheral should be enabled at a time through the peripheral clock enable bit (in the corresponding RCC peripheral clock enable register).
5. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited: the speed should not exceed 2 MHz with a maximum load of 30 pF and these IOs must not be used as a current source (e.g. to drive an LED).
6. Main function after the first backup domain power-up. Later on, it depends on the contents of the Backup registers even after reset (because these registers are not reset by the main reset). For details on how to manage these IOs, refer to the Battery backup domain and BKP register description sections in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
7. For the LQFP64 package, the pins number 5 and 6 are configured as OSC_IN/OSC_OUT after reset, however the functionality of PD0 and PD1 can be remapped by software on these pins. For the LQFP100 and LQFP144/BGA144 packages, PD0 and PD1 are available by default, so there is no need for remapping. For more details, refer to Alternate function I/O and debug configuration section in the STM32F10xxx reference manual.
8. This alternate function can be remapped by software to some other port pins (if available on the used package). For more details, refer to the Alternate function I/O and debug configuration section in the STM32F10xxx reference manual, available from the STMicroelectronics website: www.st.com.
9. For devices delivered in LQFP64 packages, the FSMC function is not available.

Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog), f_{CK}=8 MHz	44.8	45.3	46.4	810	1680	µA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	37.4	37.8	38.7	790	1660	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.8	2.0	2.5	5(2)	8(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.05	1.1	1.4	2(2)	2.3(2)	

1. Typical values are measured at T_A = 25 °C.
2. Guaranteed by characterization results, not tested in production..

Figure 14. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 20*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 7*

Table 20. Peripheral current consumption(1)

Peripheral		Current consumption
AHB (up to 72 MHz)	DMA1	23,06
	DMA2	18,47
	FSMC	55,14
	CRC	2,08
	SDIO	32,22
	BusMatrix(2)	11,67

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 24*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 24. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor	-		-	5	-	MΩ
C(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 kΩ		-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}		-	-	1.4	µA
g_m	Oscillator transconductance	-		5	-	-	µA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Guaranteed by characterization results, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer, PCB layout and humidity.

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 21). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq$ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then C_{L1} = C_{L2} = 8 pF.

Table 30. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

Table 34. Asynchronous multiplexed PSRAM/NOR read timings(1) (continued)

Symbol	Parameter	Min	Max	Unit
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns

1. C_L = 15 pF.

Figure 25. Asynchronous multiplexed PSRAM/NOR write waveforms

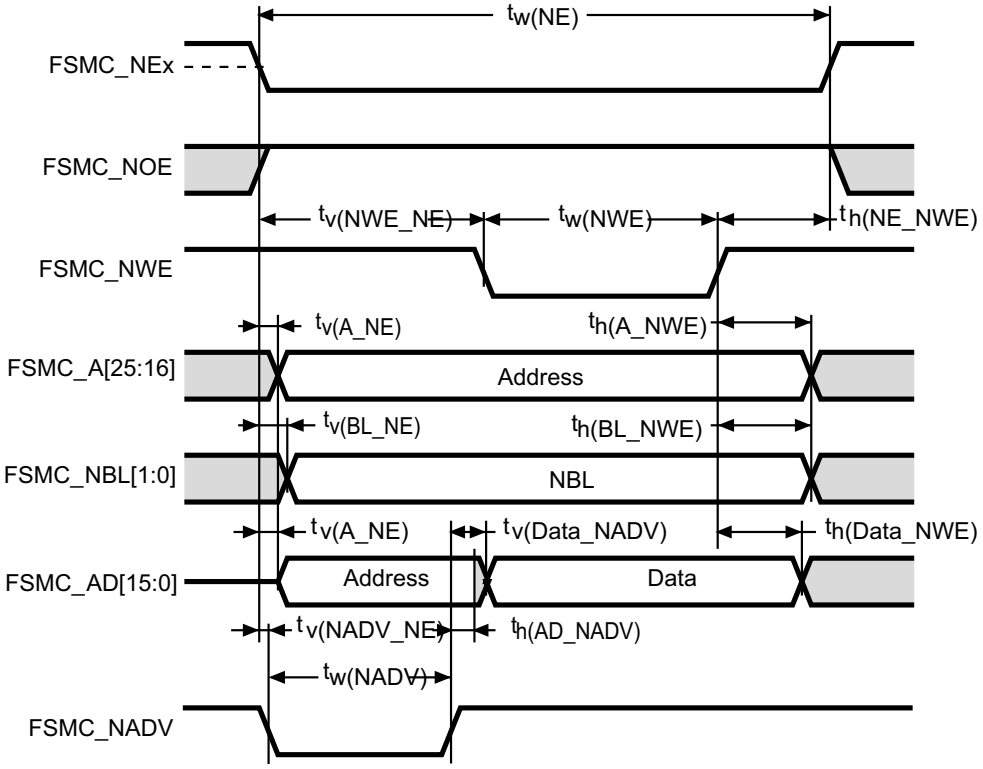


Table 35. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK}$ + 0.5	$5t_{HCLK}$ + 2	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	t_{HCLK} + 1	t_{HCLK} + 1.5	ns
$t_{w(NWE)}$	FSMC_NWE low time	$3t_{HCLK}$ + 0.5	$3t_{HCLK}$ + 1	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK} – 0.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	3.5	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	0	1	ns
$t_{w(NADV)}$	FSMC_NADV low time	t_{HCLK} + 0.5	t_{HCLK} + 1.5	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK} – 0.5	-	ns

Figure 40. Standard I/O input characteristics - CMOS port

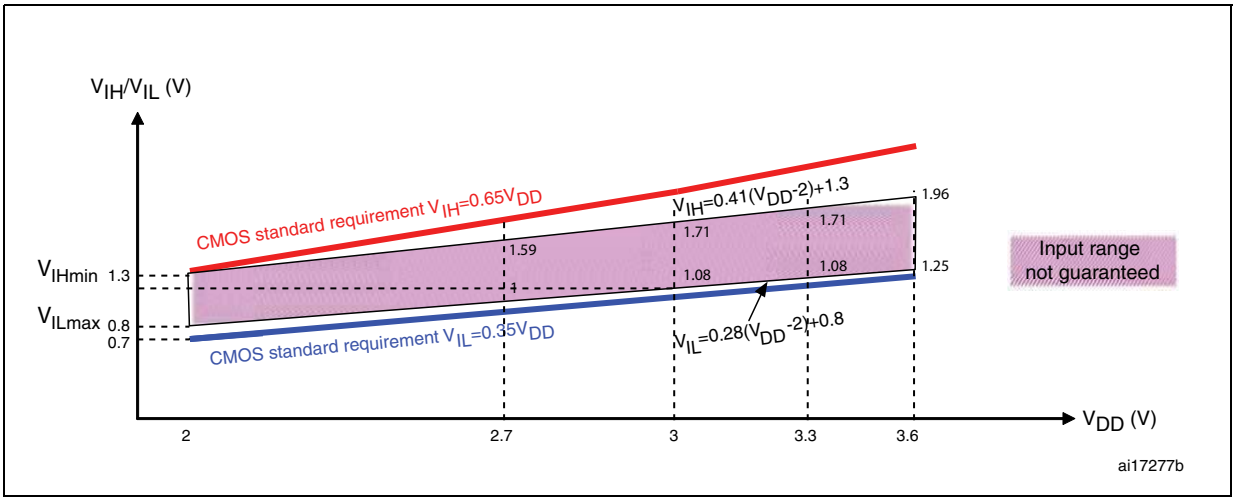


Figure 41. Standard I/O input characteristics - TTL port

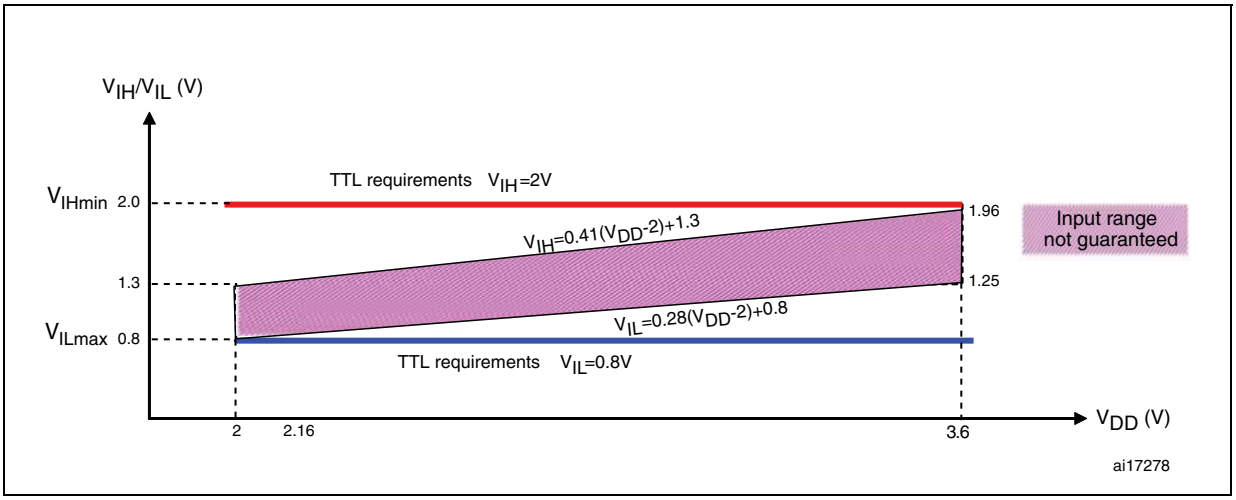


Figure 42. 5 V tolerant I/O input characteristics - CMOS port

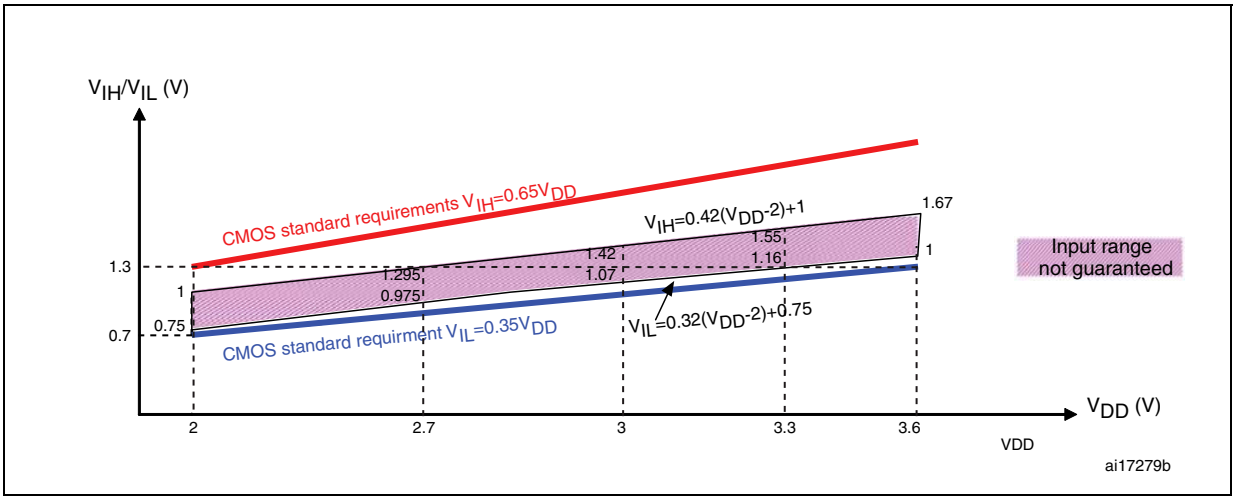
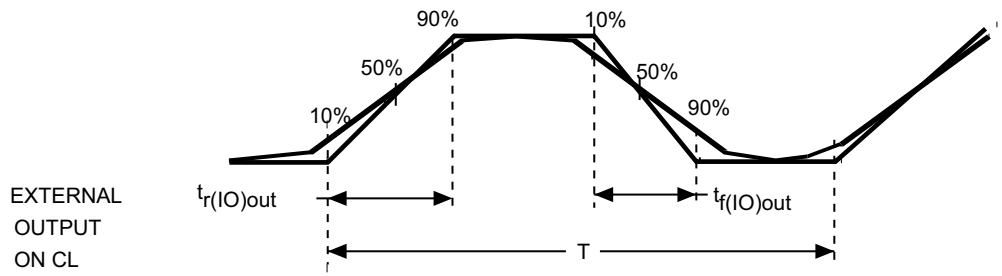


Table 50. Output voltage characteristics (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +20 mA 2.7 V < V_{DD} < 3.6 V	-	1.3	V
V_{OH}(2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–1.3	-	
V_{OL}(1)(4)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	I_{IO} = +6 mA 2 V < V_{DD} < 2.7 V	-	0.4	V
V_{OH}(2)(4)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 8* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
3. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
4. Guaranteed by characterization results, not tested in production.

Figure 44. I/O AC characteristics definition



Maximum frequency is achieved if $(t_r + t_f) \leq (2/3)T$ and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

ai14131d

5.3.15 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 49*).

Unless otherwise specified, the parameters given in *Table 52* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 52. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST Input low level voltage	-	–0.5	-	0.8	V
$V_{IH(NRST)}$(1)	NRST Input high level voltage	-	2	-	V_{DD}+0.5	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	-	200	-	mV
R_{PU}	Weak pull-up equivalent resistor(2)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(1)	NRST Input filtered pulse	-	-	-	100	ns
$V_{NF(NRST)}$(1)	NRST Input not filtered pulse	-	300	-	-	ns

1. Guaranteed by design, not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).

Table 58. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 59. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

5.3.18 CAN (controller area network) interface

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 62* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 10*.

Note: It is recommended to perform a calibration after each power-up.

Table 62. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 63* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

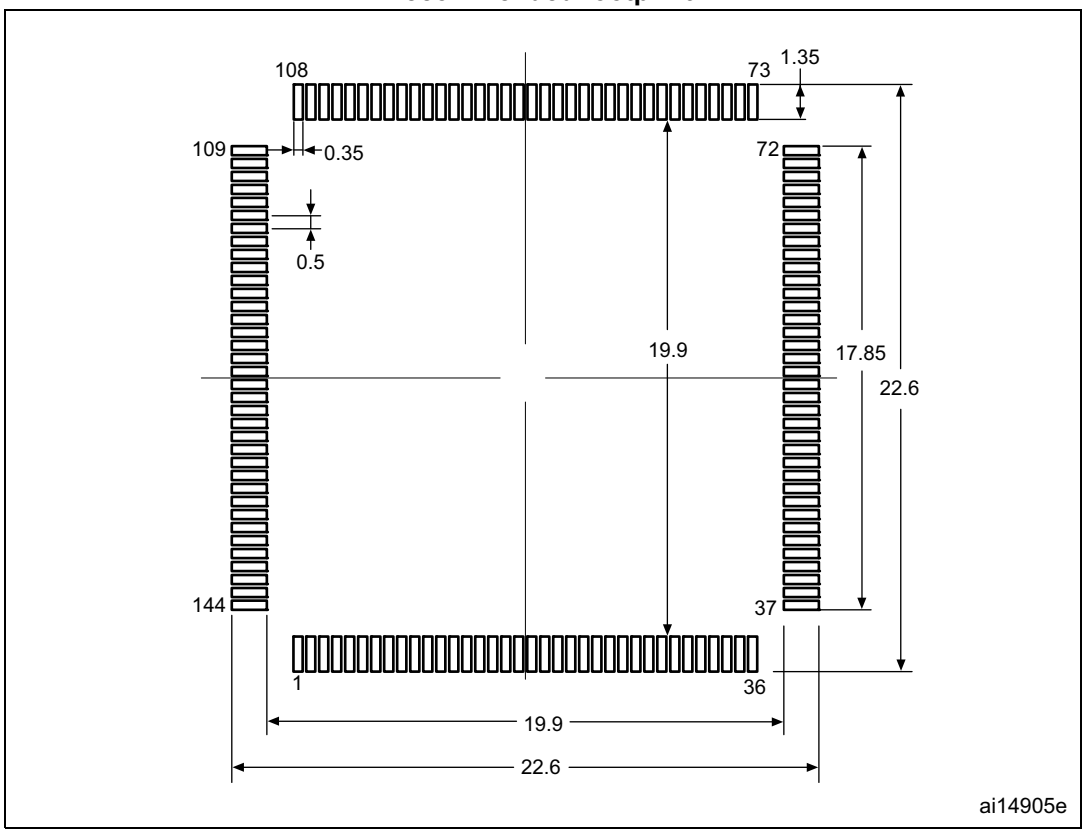
1. Guaranteed by characterization results, not tested in production.

Table 69. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 63. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Table 74. Document revision history

Date	Revision	Changes
15-May-2015	4	Added document status on first page. Replace DAC1_OUT/DAC2_OUT by DAC_OUT1/DAC_OUT2, and updated TIM5 in *Figure 1: STM32F103xF and STM32F103xG performance line block diagram on page 12*. Replaced USBDP/USBDM by USB_DP/USB_DM in the whole document. Updated notes related to electrical values guaranteed by characterization results. Updated *Table 20: Peripheral current consumption*. Updated *Table 36: Synchronous multiplexed NOR/PSRAM read timings* to *Table 39: Synchronous non-multiplexed PSRAM write timings*(added FSMC_NWAIT timings). Updated *Figure 26: Synchronous multiplexed NOR/PSRAM read timings on page 73* and *Figure 28: Synchronous non-multiplexed NOR/PSRAM read timings on page 77* and *Figure 35: PC Card/CompactFlash controller waveforms for I/O space write access on page 83*. Updated CDM class in *Table 46: ESD absolute maximum ratings*. Updated *Figure 44: I/O AC characteristics definition on page 96* and *Figure 45: Recommended NRST pin protection on page 97*. Updated *Figure 49: SPI timing diagram - master mode(1) on page 96*. Modified note 3 in *Table 56: SPI characteristics*. *Section : I2C interface characteristics*: Updated introduction, updated *Table 54: I^2C characteristics* and *Figure 46: I^2C bus AC waveforms and measurement circuit on page 99*. Modified note 2 in *Table 64: ADC accuracy - limited test conditions*, *Figure 55: ADC accuracy characteristics on page 110* and *Figure 56: Typical connection diagram using the ADC on page 111*. Updated *Figure 57: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) on page 111* and *Figure 58: Power supply and reference decoupling (V_{REF+} connected to V_{DDA}) on page 112*. Updated I_{DDA} description and Offset comment in *Table 66: DAC characteristics*. Updated *Section 6.1: LFBGA144 package information* and added *Section : Device marking for LFBGA144 package*. Updated *Section 6.2: LQFP144 package information* and added *Section : Device marking for LQFP144 package*. Updated *Section 6.3: LQFP100 package information* and added *Section : Device marking for LQFP100 package*. Updated *Section 6.4: LQFP64 package information* and added *Section : Device marking for LQFP64 package*.