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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vft6tr

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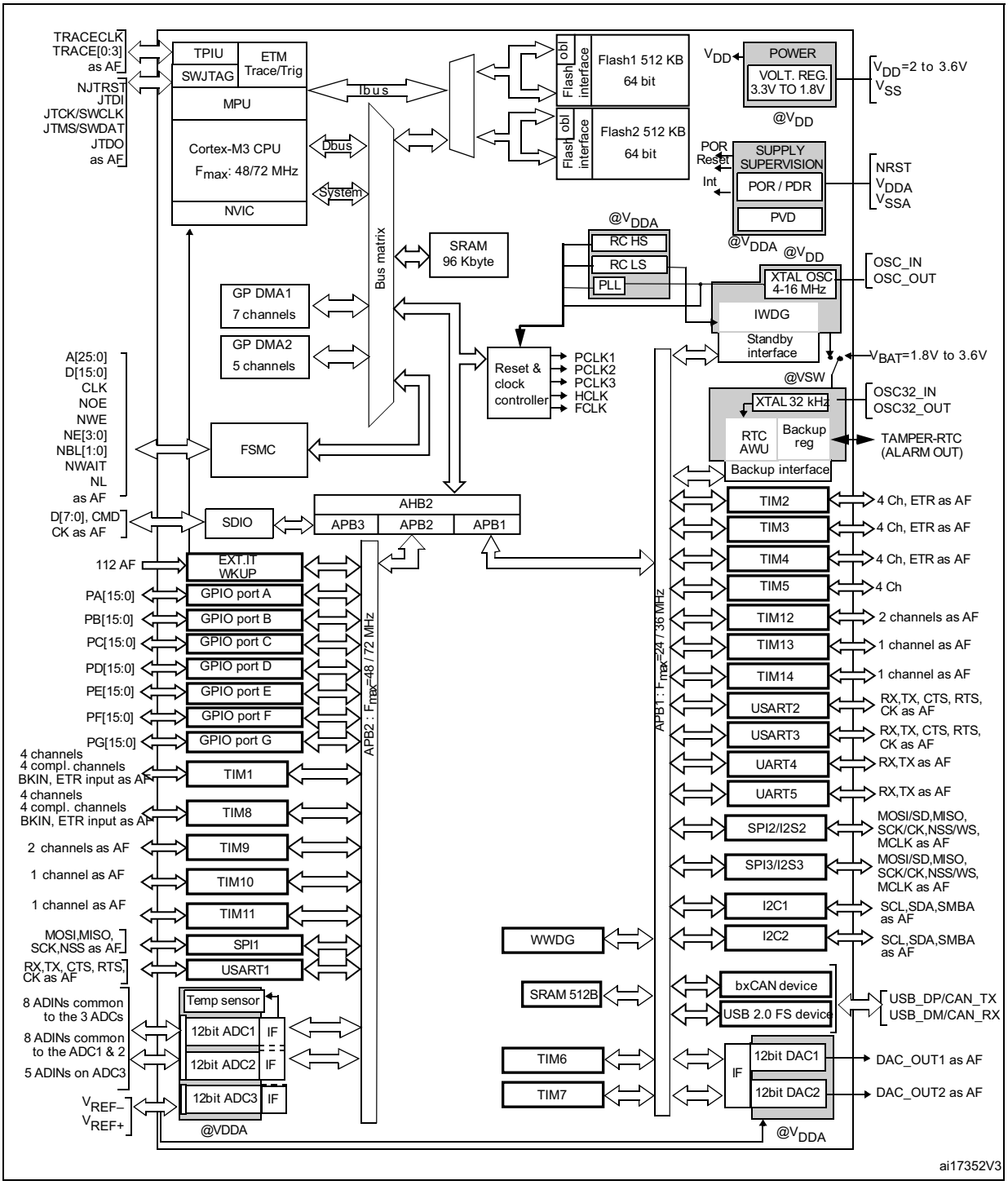
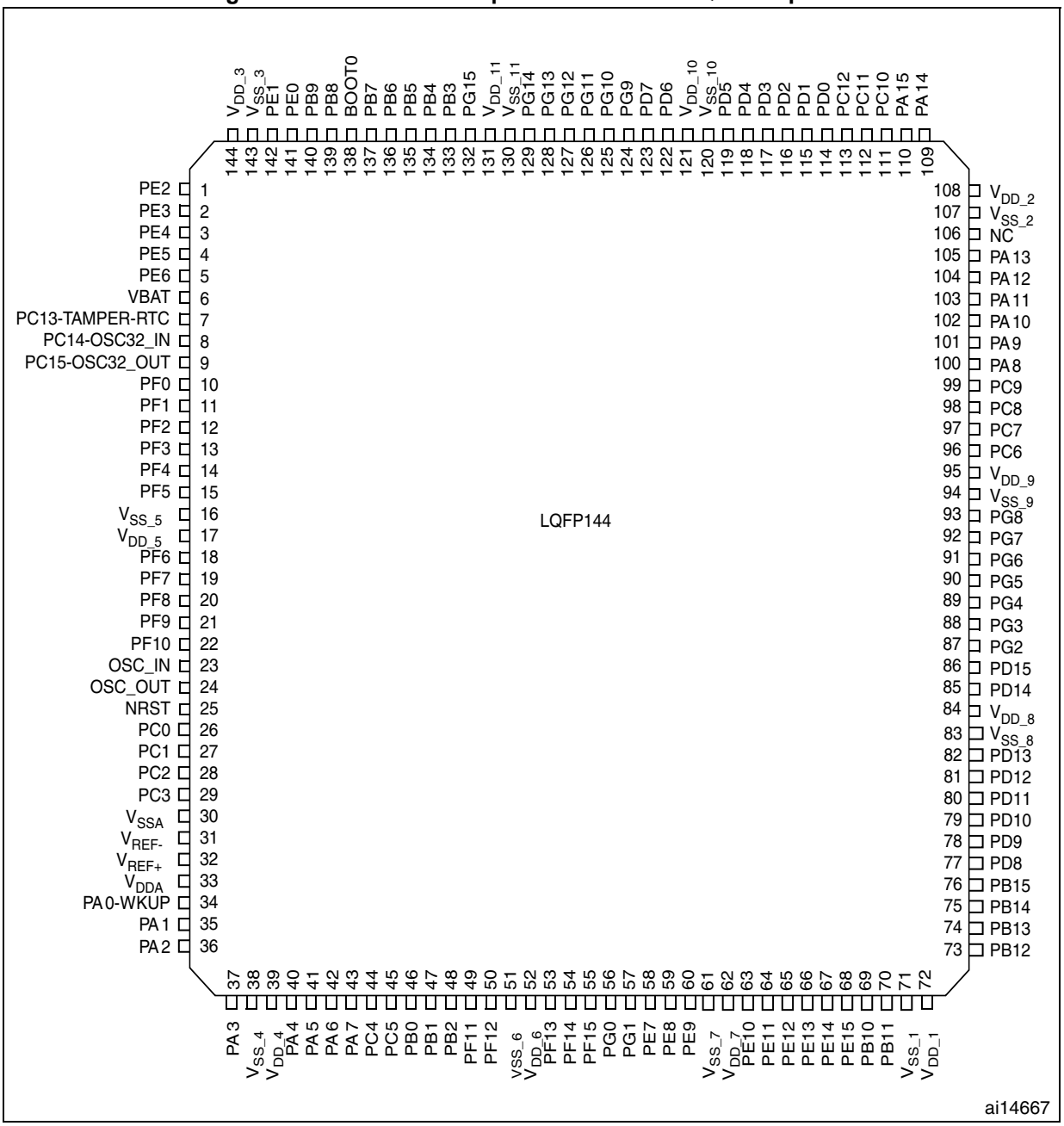
Figure 1. STM32F103xF and STM32F103xG performance line block diagram



1. T_A = –40 °C to +85 °C (suffix 6, see *Table 73*) or –40 °C to +105 °C (suffix 7, see *Table 73*), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.9

Figure 4. STM32F103xF/G performance line LQFP144 pinout



1. The above figure shows the package top view.

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
H3	10	17	28	PC2	I/O		PC2	ADC123_IN12	-
H4	11	18	29	PC3	I/O		PC3	ADC123_IN13	-
J1	12	19	30	V_{SSA}	S		V_{SSA}	-	-
K1	-	20	31	V_{REF-}	S		V_{REF-}	-	-
L1	-	21	32	V_{REF+}	S		V_{REF+}	-	-
M1	13	22	33	V_{DDA}	S		V_{DDA}	-	-
J2	14	23	34	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS(8) / ADC123_IN0 / TIM2_CH1_ETR / TIM5_CH1 / TIM8_ETR	-
K2	15	24	35	PA1	I/O		PA1	USART2_RTS(7) / ADC123_IN1 / TIM5_CH2 / TIM2_CH2(7)	-
L2	16	25	36	PA2	I/O		PA2	USART2_TX(7) / TIM5_CH3 / ADC123_IN2 / TIM9_CH1 / TIM2_CH3 (7)	-
M2	17	26	37	PA3	I/O		PA3	USART2_RX(7) / TIM5_CH4 / ADC123_IN3 / TIM2_CH4(7)/ TIM9_CH2	-
G4	18	27	38	V_{SS_4}	S		V_{SS_4}	-	-
F4	19	28	39	V_{DD_4}	S		V_{DD_4}	-	-
J3	20	29	40	PA4	I/O		PA4	SPI1_NSS(7) / USART2_CK(7) / DAC_OUT1 / ADC12_IN4	-
K3	21	30	41	PA5	I/O		PA5	SPI1_SCK(7) / DAC_OUT2 / ADC12_IN5	-
L3	22	31	42	PA6	I/O		PA6	SPI1_MISO(7) / TIM8_BKIN / ADC12_IN6 / TIM3_CH1(7)/ TIM13_CH1	TIM1_BKIN
M3	23	32	43	PA7	I/O		PA7	SPI1_MOSI(7)/ TIM8_CH1N / ADC12_IN7 / TIM3_CH2(7) / TIM14_CH1	TIM1_CH1N
J4	24	33	44	PC4	I/O		PC4	ADC12_IN14	-
K4	25	34	45	PC5	I/O		PC5	ADC12_IN15	-
L4	26	35	46	PB0	I/O		PB0	ADC12_IN8 / TIM3_CH3 / TIM8_CH2N	TIM1_CH2N

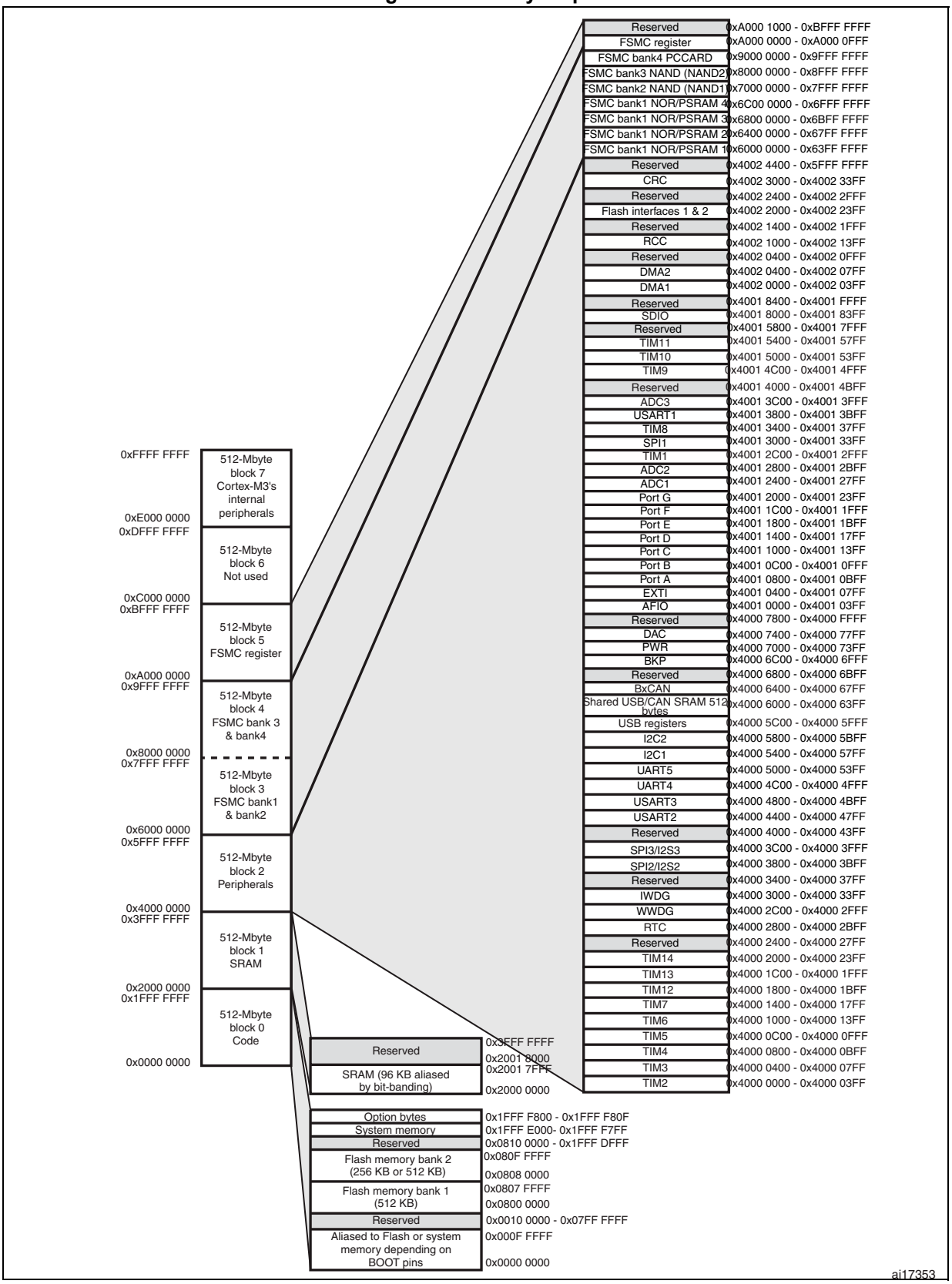
Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
M4	27	36	47	PB1	I/O		PB1	ADC12_IN9 / TIM3_CH4(7) / TIM8_CH3N	TIM1_CH3N
J5	28	37	48	PB2	I/O	FT	PB2/BOOT1	-	-
M5	-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	-
L5	-	-	50	PF12	I/O	FT	PF12	FSMC_A6	-
H5	-	-	51	V_{SS_6}	S		V_{SS_6}	-	-
G5	-	-	52	V_{DD_6}	S		V_{DD_6}	-	-
K5	-	-	53	PF13	I/O	FT	PF13	FSMC_A7	-
M6	-	-	54	PF14	I/O	FT	PF14	FSMC_A8	-
L6	-	-	55	PF15	I/O	FT	PF15	FSMC_A9	-
K6	-	-	56	PG0	I/O	FT	PG0	FSMC_A10	-
J6	-	-	57	PG1	I/O	FT	PG1	FSMC_A11	-
M7	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	-	61	V_{SS_7}	S		V_{SS_7}	-	-
G6	-	-	62	V_{DD_7}	S		V_{DD_7}	-	-
J7	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL / USART3_TX(7)	TIM2_CH3
M10	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA / USART3_RX(7)	TIM2_CH4
H7	31	49	71	V_{SS_1}	S		V_{SS_1}	-	-
G7	32	50	72	V_{DD_1}	S		V_{DD_1}	-	-
M11	33	51	73	PB12	I/O	FT	PB12	SPI2_NSS / I2S2_WS / I2C2_SMBA / USART3_CK(7) / TIM1_BKIN(7)	-

4 Memory mapping

The memory map is shown in *Figure 7*.

Figure 7. Memory map



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHZ and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)

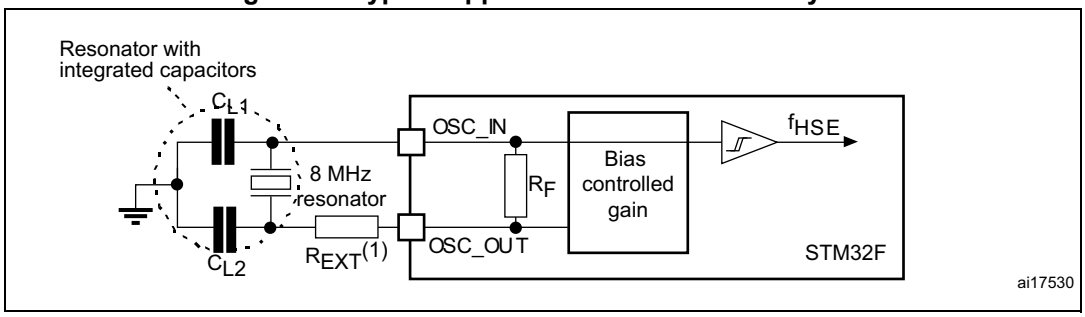
When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK}2 = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

Table 18. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	52.5	33.5	mA
			48 MHz	36.6	23.8	
			36 MHz	28.5	18.7	
			24 MHz	24.1	12.8	
			16 MHz	14	9.2	
			8 MHz	7.7	5.4	
			4 MHz	4.6	3.4	
			2 MHz	3	2.3	
			1 MHz	2.2	1.8	
			500 kHz	1.7	1.5	
			125 kHz	1.4	1.3	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	45.5	28.6	mA
			48 MHz	35.1	22.4	
			36 MHz	27.5	17.5	
			24 MHz	18.9	11.6	
			16 MHz	12.2	8.2	
			8 MHz	7.2	4.8	
			4 MHz	4	2.7	
			2 MHz	2.3	1.7	
			1 MHz	1.5	1.2	
			500 kHz	1.1	0.9	
			125 kHz	0.75	0.7	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 20. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 24*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 24. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)(2)

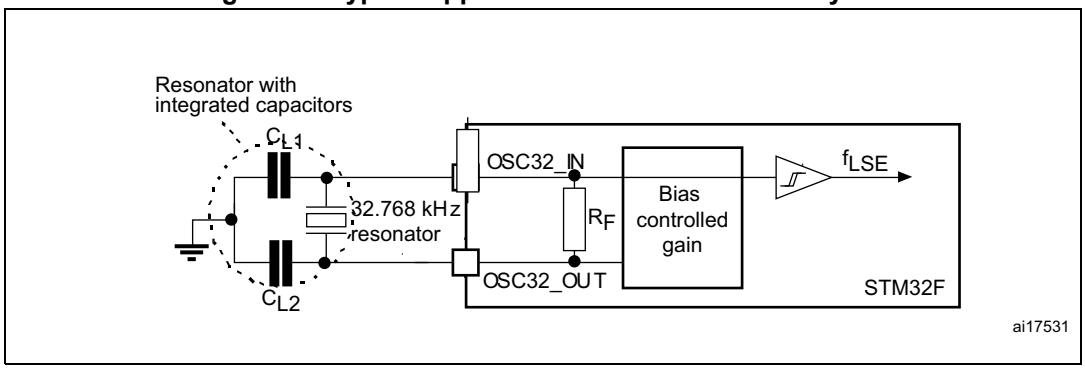
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor	-		-	5	-	MΩ
C(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 kΩ		-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}		-	-	1.4	µA
g_m	Oscillator transconductance	-		5	-	-	µA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Guaranteed by characterization results, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer, PCB layout and humidity.

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 21). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq$ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then C_{L1} = C_{L2} = 8 pF.

Figure 21. Typical application with a 32.768 kHz crystal



5.3.7 Internal clock source characteristics

The parameters given in *Table 25* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

High-speed internal (HSI) RC oscillator

Table 25. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{HSI}	Frequency	-		-	8		MHz
$DuCy_{(HSI)}$	Duty cycle	-		45	-	55	%
ACC_{HSI}	Accuracy of the HSI oscillator	User-trimmed with the RCC_CR register(2)		-	-	1(3)	%
		Factory-calibrated(4)	T_A = –40 to 105 °C	–2	-	2.5	%
			T_A = –10 to 85 °C	–1.5	-	2.2	%
			T_A = 0 to 70 °C	–1.3	-	2	%
			T_A = 25 °C	–1.1	-	1.8	%
$t_{su(HSI)}$(4)	HSI oscillator startup time	-		1	-	2	µs
$I_{DD(HSI)}$(4)	HSI oscillator power consumption	-		-	80	100	µA

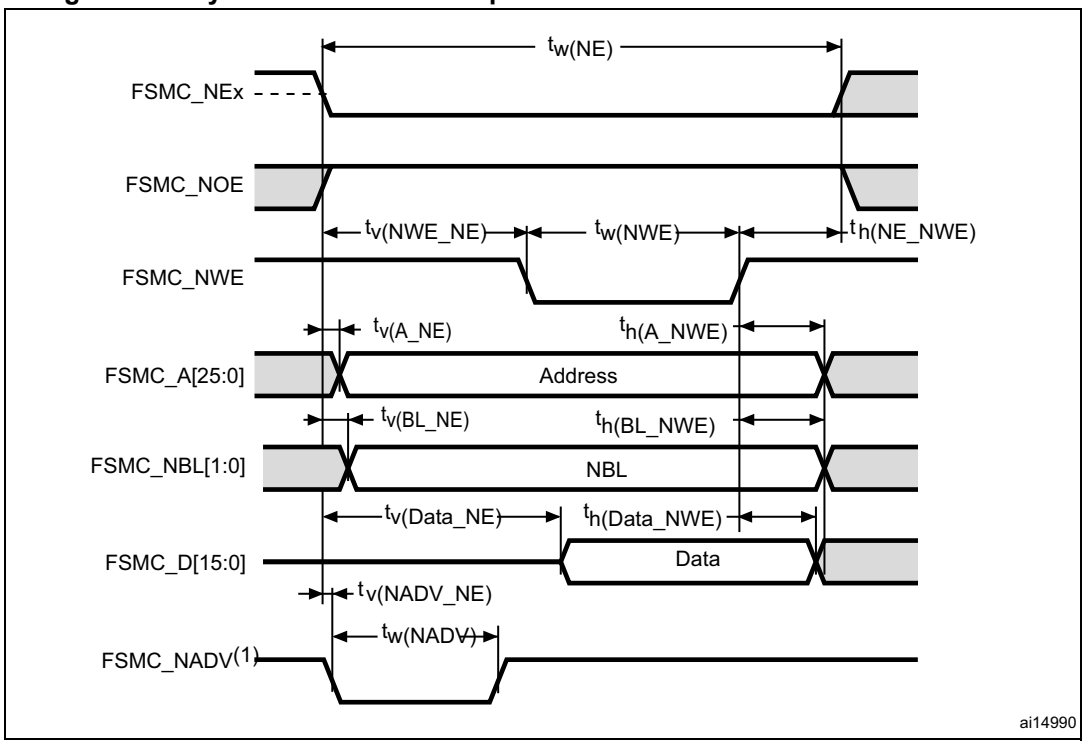
1. V_{DD} = 3.3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Refer to application note AN2868 “STM32F10xxx internal RC oscillator (HSI) calibration” available from the ST website *www.st.com*.
3. Guaranteed by design, not tested in production.
4. Guaranteed by characterization results, not tested in production.

Table 31. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$5t_{HCLK}$ + 0.5	$5t_{HCLK}$ + 2	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	0.5	1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$5t_{HCLK}$ – 1	$5t_{HCLK}$ + 1	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	3	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	0	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0.5	-	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$2t_{HCLK}$ - 1	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOEx high setup time	$2t_{HCLK}$ - 1	-	ns
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	0	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	t_{HCLK} + 2	ns

1. C_L = 15 pF.

Figure 23. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Table 35. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$4t_{HCLK} - 2$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$t_{HCLK} - 1.5$	-	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	$t_{HCLK} + 6$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$t_{HCLK} - 0.5$	-	ns

1. C_L = 15 pF.

Synchronous waveforms and timings

Figure 26 through *Figure 29* represent synchronous waveforms and *Table 37* through *Table 39* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

Figure 31. PC Card/CompactFlash controller waveforms for common memory write access

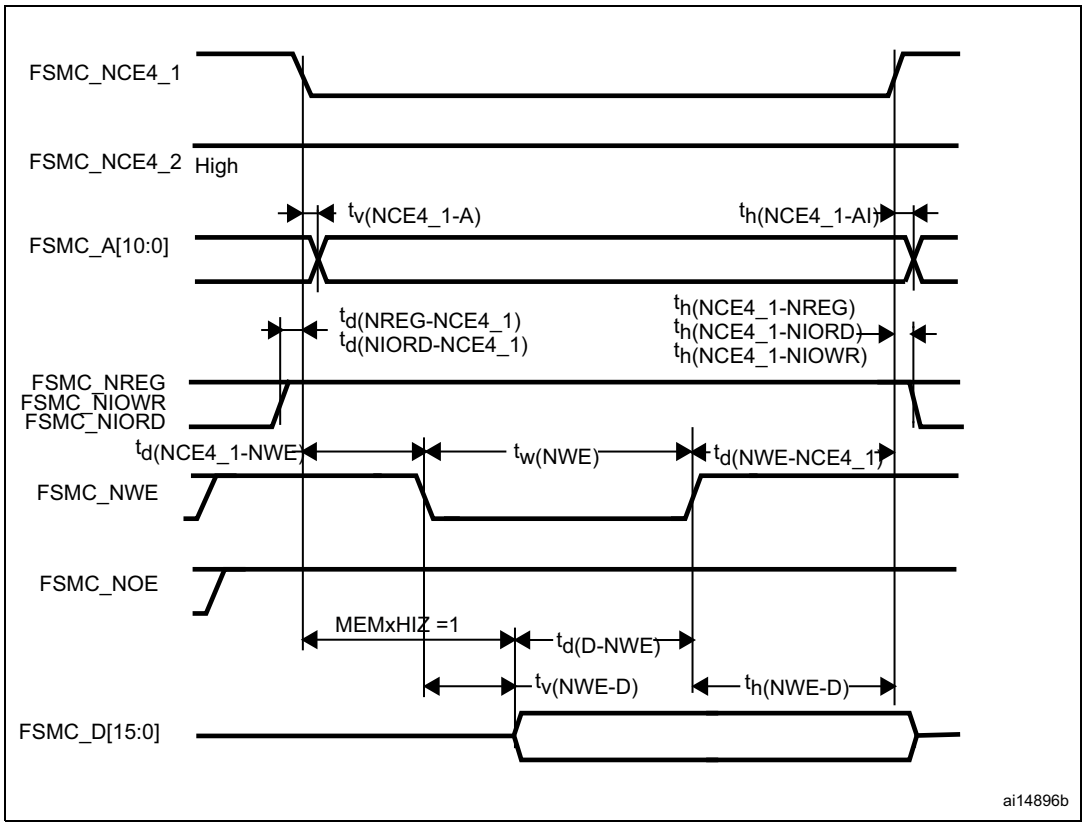


Table 43. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$3t_{HCLK}$	$3t_{HCLK}$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$2t_{HCLK} + 2$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3t_{HCLK} + 1.5$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK} + 8$	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$2t_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$2t_{HCLK}$	-	ns

1. C_L = 15 pF.

Table 58. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

USB characteristics

The USB interface is USB-IF certified (Full Speed).

Table 59. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

5.3.18 CAN (controller area network) interface

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (CAN_TX and CAN_RX).

5.3.19 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 62* are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 10*.

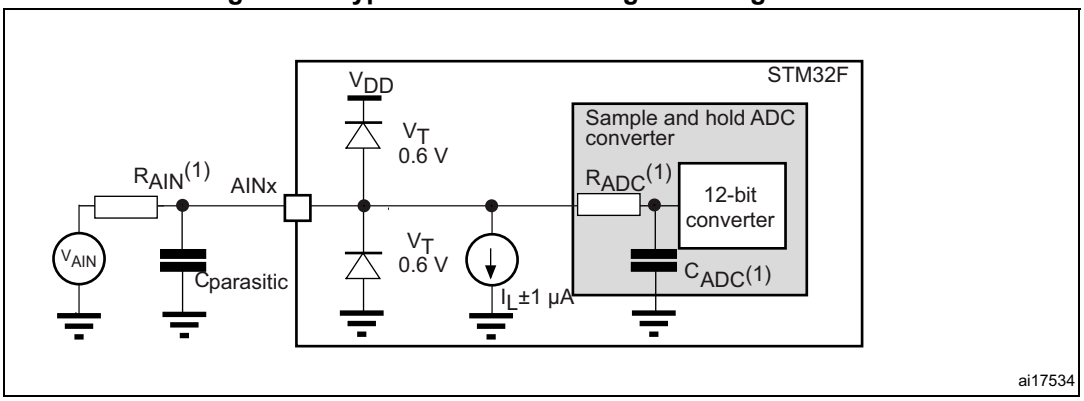
Note: It is recommended to perform a calibration after each power-up.

Table 62. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	-	2.4	-	3.6	V
V_{REF+}	Positive reference voltage	-	2.4	-	V_{DDA}	V
I_{VREF}	Current on the V_{REF} input pin	-	-	160	220(1)	µA
f_{ADC}	ADC clock frequency	-	0.6	-	14	MHz
f_S(2)	Sampling rate	-	0.05	-	1	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 14 MHz	-	-	823	kHz
		-	-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)	-	0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* and *Table 63* for details	-	-	50	kΩ
R_{ADC}(2)	Sampling switch resistance	-	-	-	1	kΩ
C_{ADC}(2)	Internal sample and hold capacitor	-	-	-	8	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 14 MHz	5.9			µs
		-	83			$1/f_{ADC}$
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.214	µs
		-	-	-	3(4)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 14 MHz	-	-	0.143	µs
		-	-	-	2(4)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 14 MHz	0.107	-	17.1	µs
		-	1.5	-	239.5	$1/f_{ADC}$
t_{STAB}(2)	Power-up time	-	0	0	1	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 14 MHz	1		18	µs
		-	14 to 252 (t_S for sampling +12.5 for successive approximation)			$1/f_{ADC}$

1. Guaranteed by characterization results, not tested in production.

Figure 56. Typical connection diagram using the ADC

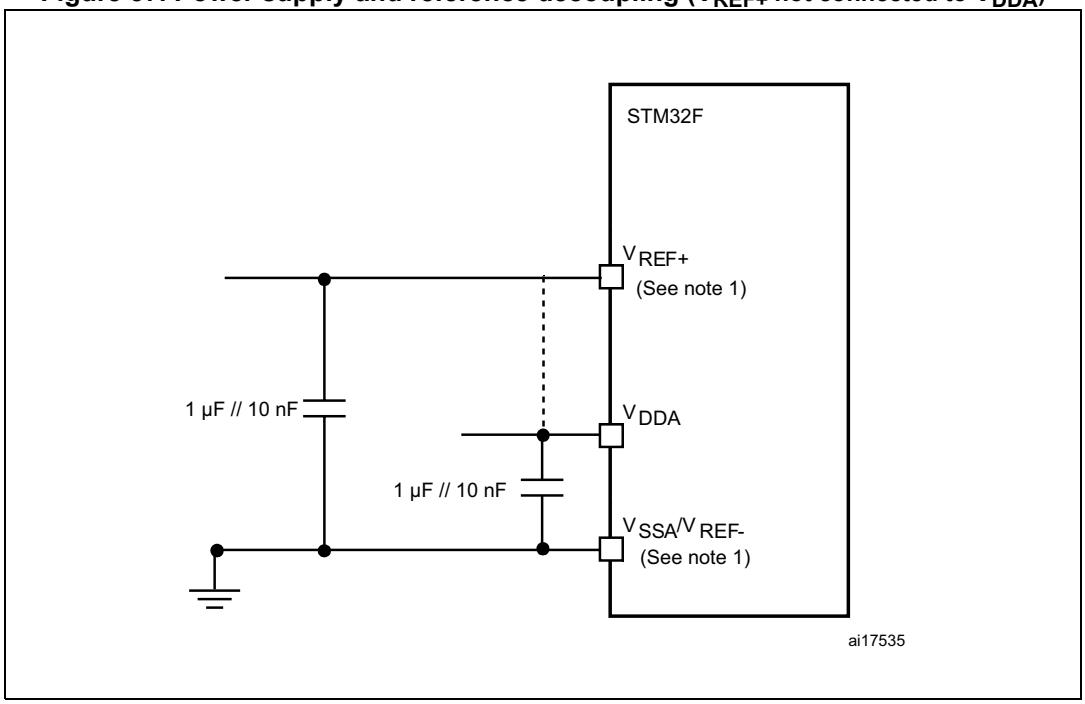


1. Refer to *Table 62* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 57* or *Figure 58*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 57. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

6.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 10: General operating conditions on page 44*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 72. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LFBGA144 - 10 × 10 mm / 0.8 mm pitch	40	°C/W
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	30	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	

6.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

Table 74. Document revision history

Date	Revision	Changes
18-Jan-2012	3	*Asynchronous waveforms and timings*: added notes about t_{HCLK} clock period and FSMC_BusTurnAroundDuration; updated conditions, modified *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings*, *Table 32: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings*, *Table 34: Asynchronous multiplexed PSRAM/NOR read timings*, and *Table 35: Asynchronous multiplexed PSRAM/NOR write timings*; added *Table 33: Asynchronous multiplexed read timings*. *Synchronous waveforms and timings*: updated *Figure 27: Synchronous multiplexed PSRAM write timings*; updated *Table 36: Synchronous multiplexed NOR/PSRAM read timings*, *Table 37: Synchronous multiplexed PSRAM write timings*, *Table 38: Synchronous non-multiplexed NOR/PSRAM read timings*, and *Table 39: Synchronous non-multiplexed PSRAM write timings*. *PC Card/CompactFlash controller waveforms and timings*: updated *Figure 35: PC Card/CompactFlash controller waveforms for I/O space write access*; split switching characteristics into *Table 40: Switching characteristics for PC Card/CF read and write cycles in attribute/common space* and *Table 41: Switching characteristics for PC Card/CF read and write cycles in I/O space*, modified values, and removed footnote concerning preliminary values. *NAND controller waveforms and timings*: updated conditions, split switching characteristics into *Table 42: Switching characteristics for NAND Flash read cycles* and *Table 43: Switching characteristics for NAND Flash write cycles*, and values modified. *Section 5.3.14: I/O port characteristics*: updated footnote*1* of *Table 49: I/O static characteristics*; updated *Output driving current*. *Table 50: Output voltage characteristics*: swapped “TTL and “CMOS” ports in the conditions column. *Table 54: I^2C characteristics*: updated footnote *2.* Updated *Table 58: SD / MMC characteristics*. *Table 62: ADC characteristics*: updated footnote *1.* *Table 64: ADC accuracy - limited test conditions*: updated footnote *3.* *Table 67: TS characteristics*: updated footnote *1.*