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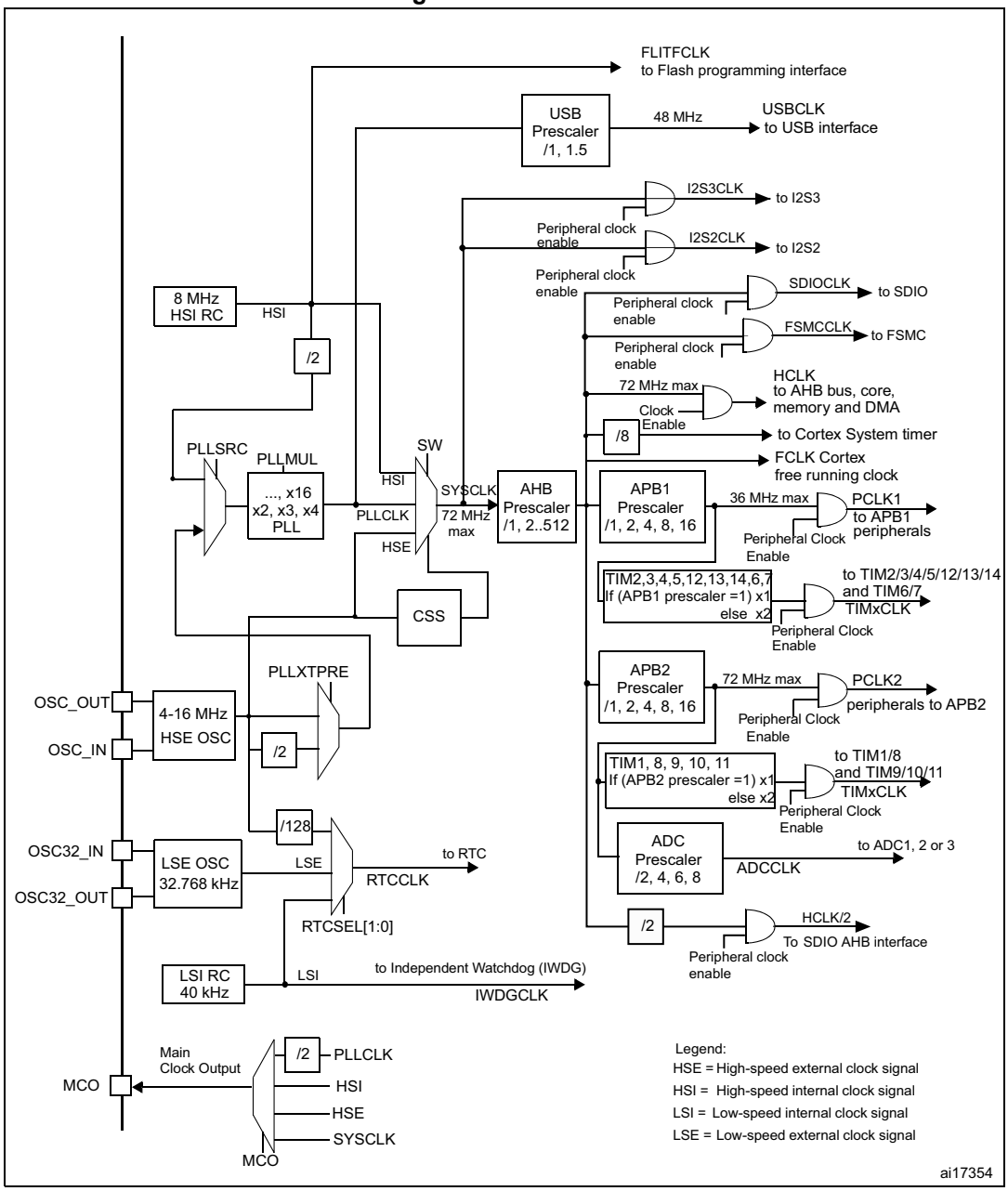
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	768KB (768K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vft7

Figure 2. Clock tree



1. When the HSI is used as a PLL clock input, the maximum system clock frequency that can be achieved is 64 MHz.
2. For the USB function to be available, both HSE and PLL must be enabled, with the USBCLK at 48 MHz.
3. To have an ADC conversion time of 1 µs, APB2 must be at 14 MHz, 28 MHz or 56 MHz.

2.3 Overview

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F103xF and STM32F103xG performance line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.3.3 Embedded Flash memory

768 Kbytes to 1 Mbyte of embedded Flash are available for storing programs and data. The Flash memory is organized as two banks. The first bank has a size of 512 Kbytes. The second bank is either 256 or 512 Kbytes depending on the device. This gives the device the capability of writing to one bank while executing code from the other bank (read-while-write capability).

2.3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

2.3.12 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to VDDA is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

2.3.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

Advanced-control timers (TIM1 and TIM8)

The two advanced-control timers (TIM1 and TIM8) can each be seen as a three-phase PWM multiplexed on 6 channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be seen as a complete general-purpose timer. The 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the advanced-control timer counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features are shared with those of the general-purpose TIM timers which have the same architecture. The advanced-control timer can therefore work together with the TIM timers via the Timer Link feature for synchronization or event chaining.

General-purpose timers (TIMx)

There are10 synchronizable general-purpose timers embedded in the STM32F103xF and STM32F103xG performance line devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  There are up to 4 synchronizable general-purpose timers (TIM2, TIM3, TIM4 and TIM5) embedded in the STM32F103xF and STM32F103xG access line devices.

  These timers are based on a 16-bit auto-reload up/down counter, a 16-bit prescaler and feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input captures / output compares / PWMs on the largest packages.

  Their counter can be frozen in debug mode. Any of the general-purpose timers can be used to generate PWM outputs. They all have independent DMA request generation.

  These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

- **TIM10, TIM11 and TIM9**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

- **TIM13, TIM14 and TIM12**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM13 and TIM14 feature one independent channel, whereas TIM12 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
H3	10	17	28	PC2	I/O		PC2	ADC123_IN12	-
H4	11	18	29	PC3	I/O		PC3	ADC123_IN13	-
J1	12	19	30	V_{SSA}	S		V_{SSA}	-	-
K1	-	20	31	V_{REF-}	S		V_{REF-}	-	-
L1	-	21	32	V_{REF+}	S		V_{REF+}	-	-
M1	13	22	33	V_{DDA}	S		V_{DDA}	-	-
J2	14	23	34	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS(8) / ADC123_IN0 / TIM2_CH1_ETR / TIM5_CH1 / TIM8_ETR	-
K2	15	24	35	PA1	I/O		PA1	USART2_RTS(7) / ADC123_IN1 / TIM5_CH2 / TIM2_CH2(7)	-
L2	16	25	36	PA2	I/O		PA2	USART2_TX(7) / TIM5_CH3 / ADC123_IN2 / TIM9_CH1 / TIM2_CH3 (7)	-
M2	17	26	37	PA3	I/O		PA3	USART2_RX(7) / TIM5_CH4 / ADC123_IN3 / TIM2_CH4(7)/ TIM9_CH2	-
G4	18	27	38	V_{SS_4}	S		V_{SS_4}	-	-
F4	19	28	39	V_{DD_4}	S		V_{DD_4}	-	-
J3	20	29	40	PA4	I/O		PA4	SPI1_NSS(7) / USART2_CK(7) / DAC_OUT1 / ADC12_IN4	-
K3	21	30	41	PA5	I/O		PA5	SPI1_SCK(7) / DAC_OUT2 / ADC12_IN5	-
L3	22	31	42	PA6	I/O		PA6	SPI1_MISO(7) / TIM8_BKIN / ADC12_IN6 / TIM3_CH1(7)/ TIM13_CH1	TIM1_BKIN
M3	23	32	43	PA7	I/O		PA7	SPI1_MOSI(7)/ TIM8_CH1N / ADC12_IN7 / TIM3_CH2(7) / TIM14_CH1	TIM1_CH1N
J4	24	33	44	PC4	I/O		PC4	ADC12_IN14	-
K4	25	34	45	PC5	I/O		PC5	ADC12_IN15	-
L4	26	35	46	PB0	I/O		PB0	ADC12_IN8 / TIM3_CH3 / TIM8_CH2N	TIM1_CH2N

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
M12	34	52	74	PB13	I/O	FT	PB13	SPI2_SCK / I2S2_CK / USART3_CTS(7) / TIM1_CH1N	-
L11	35	53	75	PB14	I/O	FT	PB14	SPI2_MISO / TIM1_CH2N / USART3_RTS(7)/ TIM12_CH1	-
L12	36	54	76	PB15	I/O	FT	PB15	SPI2_MOSI / I2S2_SD / TIM1_CH3N(7) / TIM12_CH2	-
L9	-	55	77	PD8	I/O	FT	PD8	FSMC_D13	USART3_TX
K9	-	56	78	PD9	I/O	FT	PD9	FSMC_D14	USART3_RX
J9	-	57	79	PD10	I/O	FT	PD10	FSMC_D15	USART3_CK
H9	-	58	80	PD11	I/O	FT	PD11	FSMC_A16	USART3_CTS
L10	-	59	81	PD12	I/O	FT	PD12	FSMC_A17	TIM4_CH1 / USART3_RTS
K10	-	60	82	PD13	I/O	FT	PD13	FSMC_A18	TIM4_CH2
G8	-	-	83	V_{SS_8}	S		V_{SS_8}	-	-
F8	-	-	84	V_{DD_8}	S		V_{DD_8}	-	-
K11	-	61	85	PD14	I/O	FT	PD14	FSMC_D0	TIM4_CH3
K12	-	62	86	PD15	I/O	FT	PD15	FSMC_D1	TIM4_CH4
J12	-	-	87	PG2	I/O	FT	PG2	FSMC_A12	-
J11	-	-	88	PG3	I/O	FT	PG3	FSMC_A13	-
J10	-	-	89	PG4	I/O	FT	PG4	FSMC_A14	-
H12	-	-	90	PG5	I/O	FT	PG5	FSMC_A15	-
H11	-	-	91	PG6	I/O	FT	PG6	FSMC_INT2	-
H10	-	-	92	PG7	I/O	FT	PG7	FSMC_INT3	-
G11	-	-	93	PG8	I/O	FT	PG8	-	-
G10	-	-	94	V_{SS_9}	S		V_{SS_9}	-	-
F10	-	-	95	V_{DD_9}	S		V_{DD_9}	-	-
G12	37	63	96	PC6	I/O	FT	PC6	I2S2_MCK / TIM8_CH1 / SDIO_D6	TIM3_CH1
F12	38	64	97	PC7	I/O	FT	PC7	I2S3_MCK / TIM8_CH2 / SDIO_D7	TIM3_CH2
F11	39	65	98	PC8	I/O	FT	PC8	TIM8_CH3 / SDIO_D0	TIM3_CH3

Table 6. FSMC pin definition

Pins	FSMC					LQFP100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	-	A23	A23	-	Yes
PE3	-	-	A19	A19	-	Yes
PE4	-	-	A20	A20	-	Yes
PE5	-	-	A21	A21	-	Yes
PE6	-	-	A22	A22	-	Yes
PF0	A0	A0	A0	-	-	-
PF1	A1	A1	A1	-	-	-
PF2	A2	A2	A2	-	-	-
PF3	A3	-	A3	-	-	-
PF4	A4	-	A4	-	-	-
PF5	A5	-	A5	-	-	-
PF6	NIORD	NIORD		-	-	-
PF7	NREG	NREG		-	-	-
PF8	NIOWR	NIOWR		-	-	-
PF9	CD	CD		-	-	-
PF10	INTR	INTR		-	-	-
PF11	NIOS16	NIOS16		-	-	-
PF12	A6	-	A6	-	-	-
PF13	A7	-	A7	-	-	-
PF14	A8	-	A8	-	-	-
PF15	A9	-	A9	-	-	-
PG0	A10	-	A10	-	-	-
PG1	-	-	A11	-	-	-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V £ V_{DD} £ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

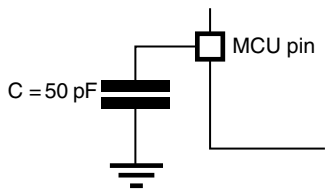


Figure 9. Pin input voltage

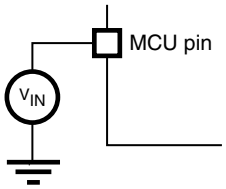


Table 19. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	72 MHz	32.5	7	mA
			48 MHz	23	5	
			36 MHz	17.7	4	
			24 MHz	12.2	3.1	
			16 MHz	8.4	2.3	
			8 MHz	4.6	1.5	
			4 MHz	3	1.3	
			2 MHz	2.15	1.25	
			1 MHz	1.7	1.2	
			500 kHz	1.5	1.15	
			125 kHz	1.35	1.15	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	28.7	5.7	
			48 MHz	22	4.4	
			36 MHz	17	3.35	
			24 MHz	11.6	2.3	
			16 MHz	7.7	1.6	
			8 MHz	3.9	0.8	
			4 MHz	2.3	0.7	
			2 MHz	1.5	0.6	
			1 MHz	1.1	0.5	
			500 kHz	0.9	0.5	
			125 kHz	0.7	0.5	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 20. Peripheral current consumption(1) (continued)

Peripheral		Current consumption
APB1 (up to 36 MHz)	APB1-Bridge	8,61
	TIM2	37,22
	TIM3	36,39
	TIM4	35,56
	TIM5	33,61
	TIM6	7,78
	TIM7	7,78
	TIM12	19,17
	TIM13	12,22
	TIM14	13,33
	SPI2/I2S2(3)	8,33
	SPI3/I2S3(3)	8,33
	USART2	12,22
	USART3	12,22
	UART4	12,22
	UART5	12,22
	I2C1	10,28
	I2C2	10,28
	USB	18,89
	CAN1	18,89
	DAC(4)	9,17
	WWDG	3,06
	PWR	2,50
	BKP	2,78
	IWDG	4,44

Table 20. Peripheral current consumption(1) (continued)

Peripheral		Current consumption
APB2 (up to 72 MHz)	APB2-Bridge	2,78
	GPIOA	7,64
	GPIOB	7,64
	GPIOC	7,64
	GPIOD	8,47
	GPIOE	8,47
	GPIOF	8,19
	GPIOG	8,19
	SPI1	5,14
	USART1	16,67
	TIM1	28,47
	TIM8	24,31
	TIM9	11,81
	TIM10	8,47
	TIM11	8,47
	ADC1(5)(6)	17,68
	ADC2(5)(6)	15,54
	ADC3(5)(6)	16,43

1. f_{HCLK} = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master peripheral is ON.
3. When the I2S is enabled, a current consumption equal to 0.02 mA must be added.
4. When DAC_OU1 or DAC_OUT2 is enabled, a current consumption equal to 0.36 mA must be added.
5. Specific conditions for ADC: f_{HCLK} = 56 MHz, $f_{APB1} = f_{HCLK/2}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$/ When ADON bit in the ADC_CR2 register is set to 1, a current consumption equal to 0.59 mA must be added.
6. When the ADC is enabled, a current consumption equal to 0.1 mA must be added.

5.3.6 External clock source characteristics

High-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 24*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 24. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor	-		-	5	-	MΩ
C(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 kΩ		-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}		-	-	1.4	µA
g_m	Oscillator transconductance	-		5	-	-	µA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Guaranteed by characterization results, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer, PCB layout and humidity.

Note: For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 21). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq$ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then C_{L1} = C_{L2} = 8 pF.

Figure 26. Synchronous multiplexed NOR/PSRAM read timings

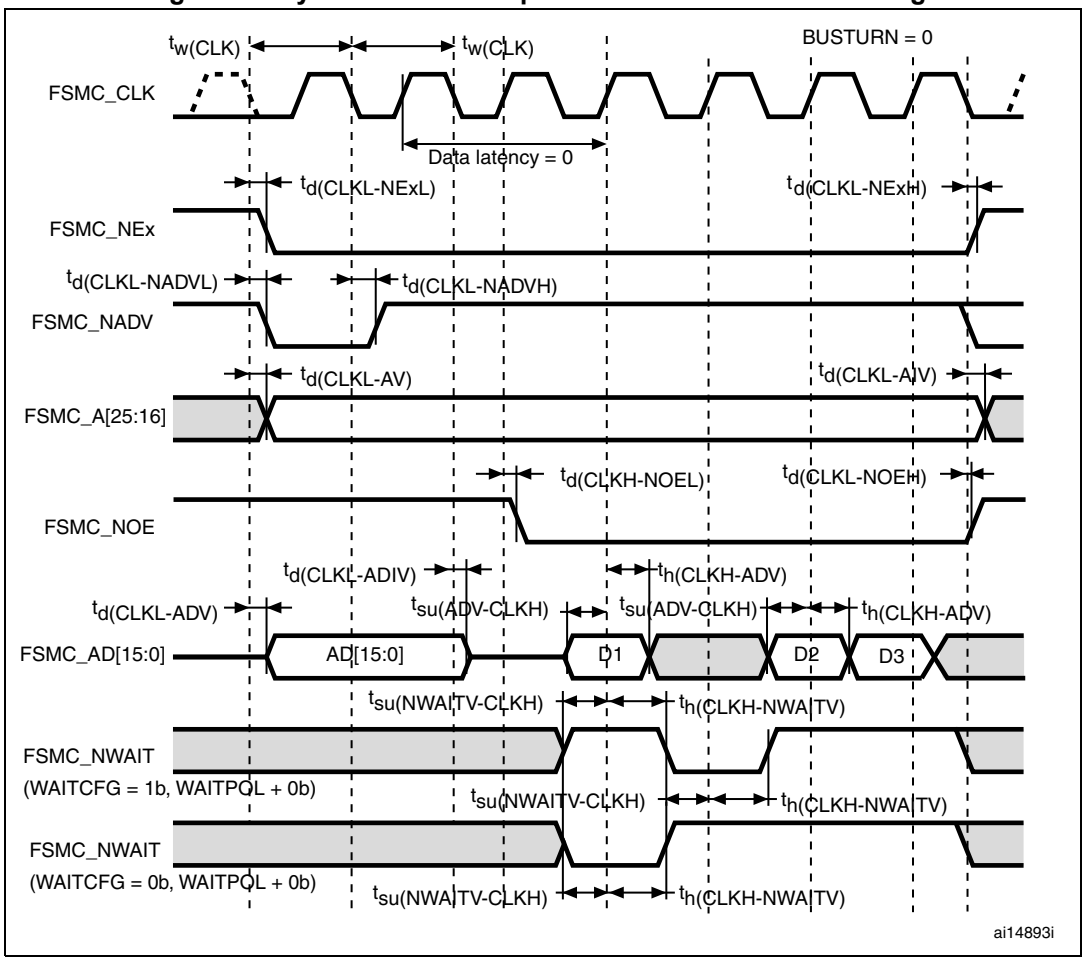


Figure 35. PC Card/CompactFlash controller waveforms for I/O space write access

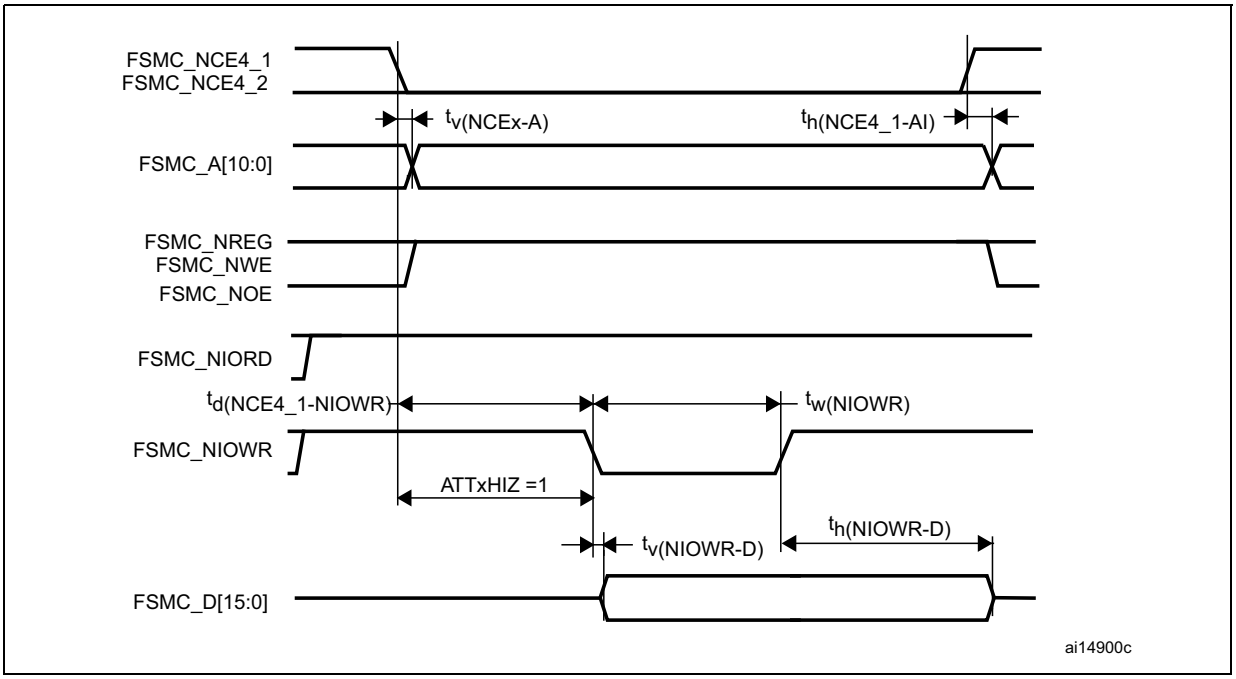


Table 40. Switching characteristics for PC Card/CF read and write cycles in attribute/common space

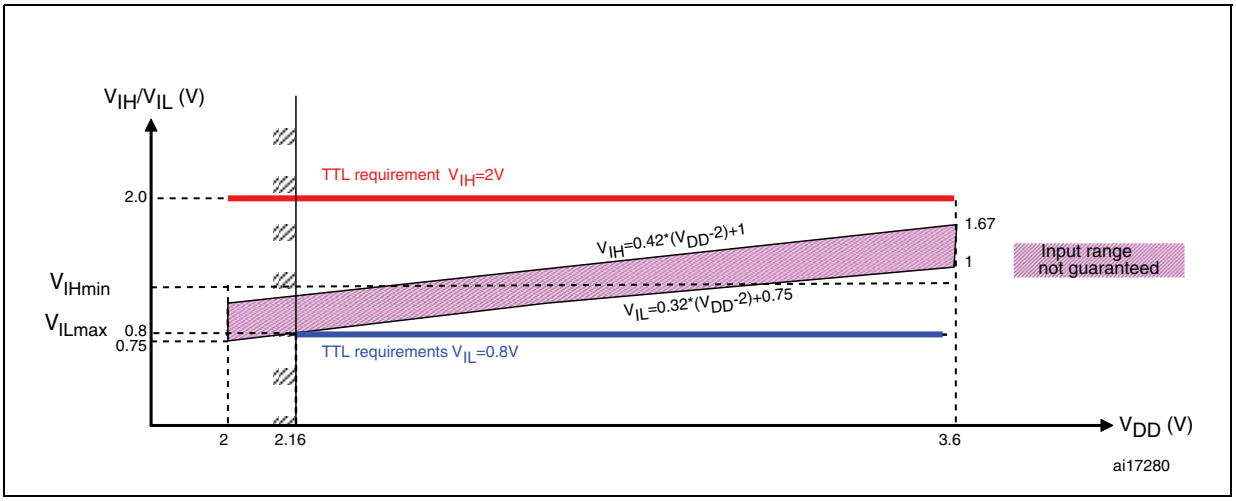
Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FSMC_NCEx low to FSMC_Ay valid	-	0	ns
$t_{h(NCEx-AI)}$	FSMC_NCEx high to FSMC_Ax invalid	0	-	
$t_{d(NREG-NCEx)}$	FSMC_NCEx low to FSMC_NREG valid	-	2	
$t_{h(NCEx-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid	t_{HCLK} + 4	-	
$t_{d(NCEx\_NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5t_{HCLK}$ + 1	
$t_{d(NCEx\_NOE)}$	FSMC_NCEx low to FSMC_NOE low	-	$5t_{HCLK}$ + 1	
$t_{w(NOE)}$	FSMC_NOE low width	$8t_{HCLK}$ - 0.5	$8t_{HCLK}$ + 1	
$t_{d(NOE-NCEx}$	FSMC_NOE high to FSMC_NCEx high	$5t_{HCLK}$ - 0.5	-	
$t_{su(D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	32	-	
$t_{h(NOE-D)}$	FSMC_NOE high to FSMC_D[15:0] invalid	t_{HCLK}	-	
$t_{w(NWE)}$	FSMC_NWE low width	$8t_{HCLK}$ – 1	$8t_{HCLK}$ + 4	
$t_{d(NWE\_NCEx)}$	FSMC_NWE high to FSMC_NCEx high	$5t_{HCLK}$ + 1.5	-	
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5t_{HCLK}$ + 1	
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$11t_{HCLK}$	-	
$t_{d(D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	$13t_{HCLK}$ + 2.5	-	

Table 43. Switching characteristics for NAND Flash write cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NWE)}$	FSMC_NWE low width	$3t_{HCLK}$	$3t_{HCLK}$	ns
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	ns
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$2t_{HCLK} + 2$	-	ns
$t_{d(ALE-NWE)}$	FSMC_ALE valid before FSMC_NWE low	-	$3t_{HCLK} + 1.5$	ns
$t_{h(NWE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$3t_{HCLK} + 8$	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$2t_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$2t_{HCLK}$	-	ns

1. C_L = 15 pF.

Figure 43. 5 V tolerant I/O input characteristics - TTL port



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ±8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ±3 mA. When using the GPIOs PC13 to PC15 in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in *Section 5.2*:

- The sum of the currents sourced by all the I/Os on $V_{DD,}$ plus the maximum Run consumption of the MCU sourced on $V_{DD,}$ cannot exceed the absolute maximum rating I_{VDD} (see *Table 8*).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating I_{VSS} (see *Table 8*).

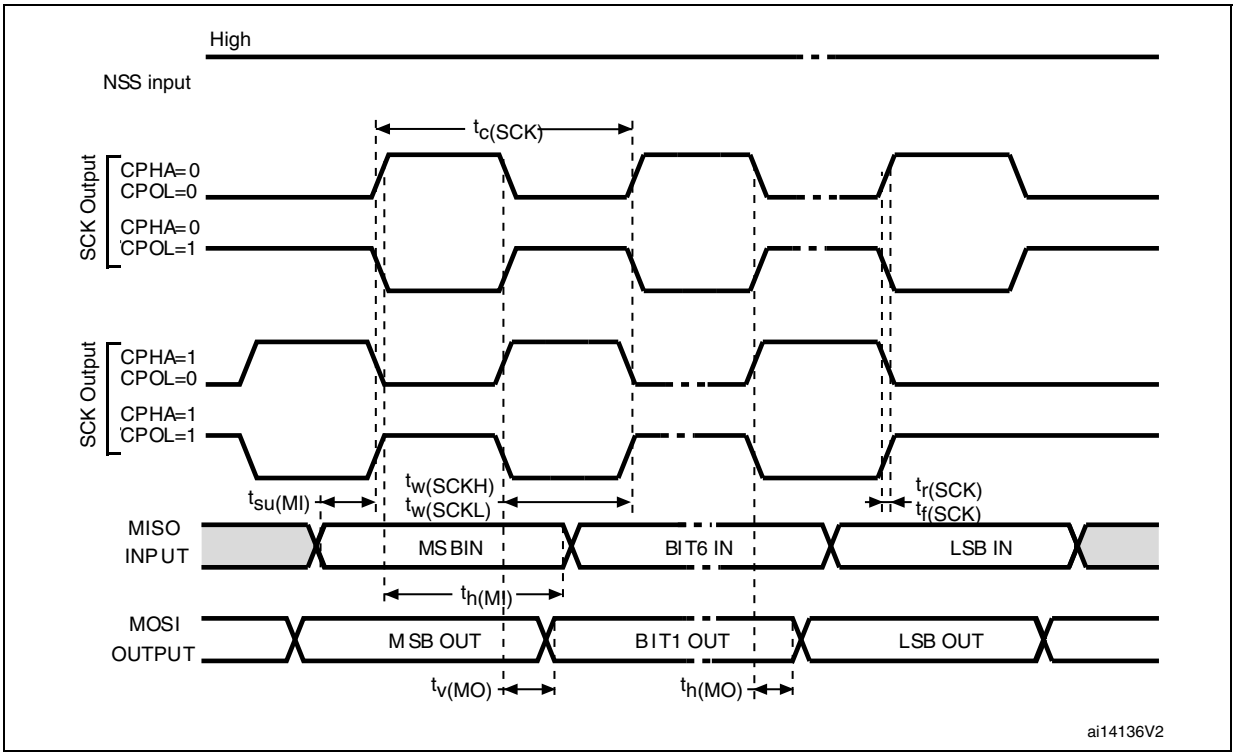
Output voltage levels

Unless otherwise specified, the parameters given in *Table 50* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 50. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	TTL port(3) I_{IO} = +8 mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin when 8 pins are sunk at same time	CMOS port(3) I_{IO} =+ 8mA 2.7 V < V_{DD} < 3.6 V	-	0.4	V
V_{OH} (2)	Output high level voltage for an I/O pin when 8 pins are sourced at same time		2.4	-	

Figure 49. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Table 57. I^2S characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
DuCy(SCK)	I2S slave input clock duty cycle	Slave mode		30	70	%
f_{CK} $1/t_{c(CK)}$	I^2S clock frequency	Master mode (data: 16 bits, Audio frequency = 48 kHz)		1.522	1.525	MHz
		Slave mode		0	6.5	
$t_{r(CK)}$ $t_{f(CK)}$	I^2S clock rise and fall time	Capacitive load C_L = 50 pF		-	8	ns
$t_{v(WS)}$ (1)	WS valid time	Master mode		3	-	
$t_{h(WS)}$ (1)	WS hold time	Master mode	I2S2	2	-	
			I2S3	0	-	
$t_{su(WS)}$ (1)	WS setup time	Slave mode		4	-	
$t_{h(WS)}$ (1)	WS hold time	Slave mode		0	-	
$t_{w(CKH)}$ (1)	CK high and low time	Master f_{PCLK}= 16 MHz, audio frequency = 48 kHz		312.5	-	
$t_{w(CKL)}$ (1)				345	-	
$t_{su(SD\_MR)}$ (1)	Data input setup time	Master receiver	I2S2	2	-	
			I2S3	6.5	-	
$t_{su(SD\_SR)}$ (1)	Data input setup time	Slave receiver		1.5	-	
$t_{h(SD\_MR)}$ (1)(2)	Data input hold time	Master receiver		0	-	
$t_{h(SD\_SR)}$ (1)(2)		Slave receiver		0.5	-	
$t_{v(SD\_ST)}$ (1)(2)	Data output valid time	Slave transmitter (after enable edge)		-	18	
$t_{h(SD\_ST)}$ (1)	Data output hold time	Slave transmitter (after enable edge)		11	-	
$t_{v(SD\_MT)}$ (1)(2)	Data output valid time	Master transmitter (after enable edge)		-	3	
$t_{h(SD\_MT)}$ (1)	Data output hold time	Master transmitter (after enable edge)		0	-	

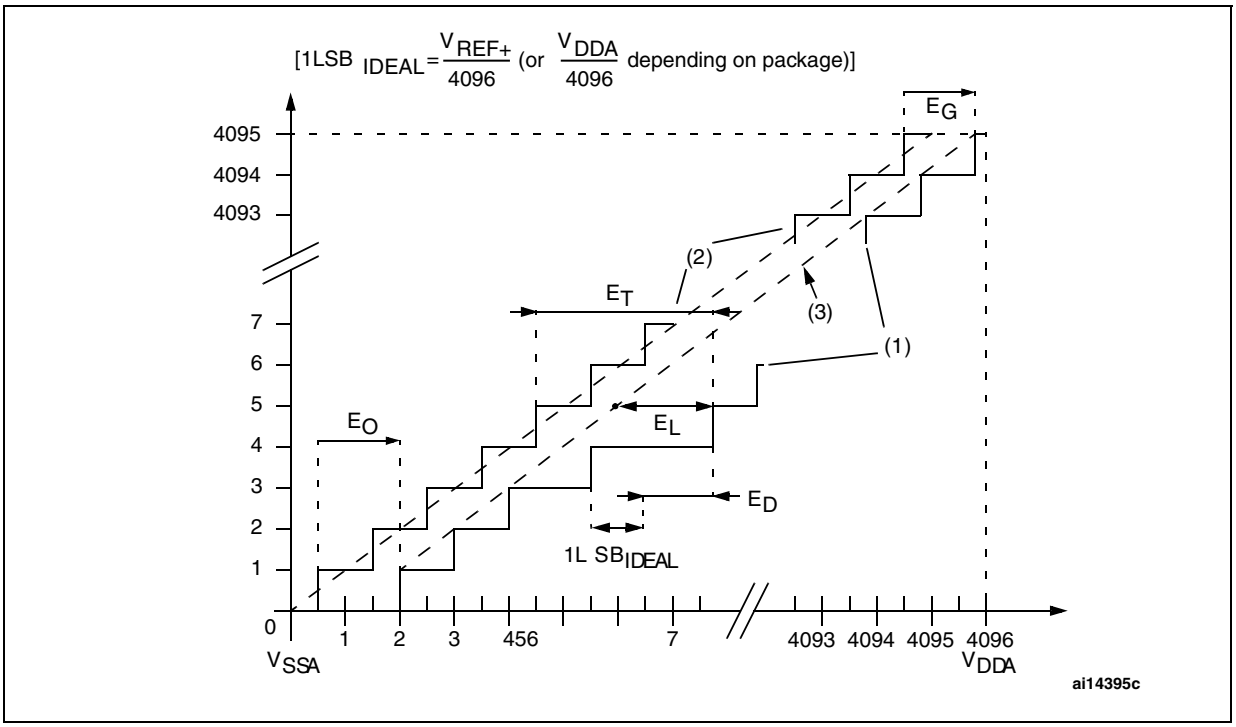
1. Guaranteed by design and/or characterization results, not tested in production.
2. Depends on f_{PCLK}. For example, if f_{PCLK}=8 MHz, then T_{PCLK} = $1/f_{PLCLK}$ =125 ns.

Table 65. ADC accuracy(1) (2)(3)

Symbol	Parameter	Test conditions	Typ	Max(4)	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 V to 3.6 V Measurements made after ADC calibration	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted V_{DD}, frequency, V_{REF} and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
   Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.14* does not affect the ADC accuracy.
4. Preliminary values.

Figure 55. ADC accuracy characteristics



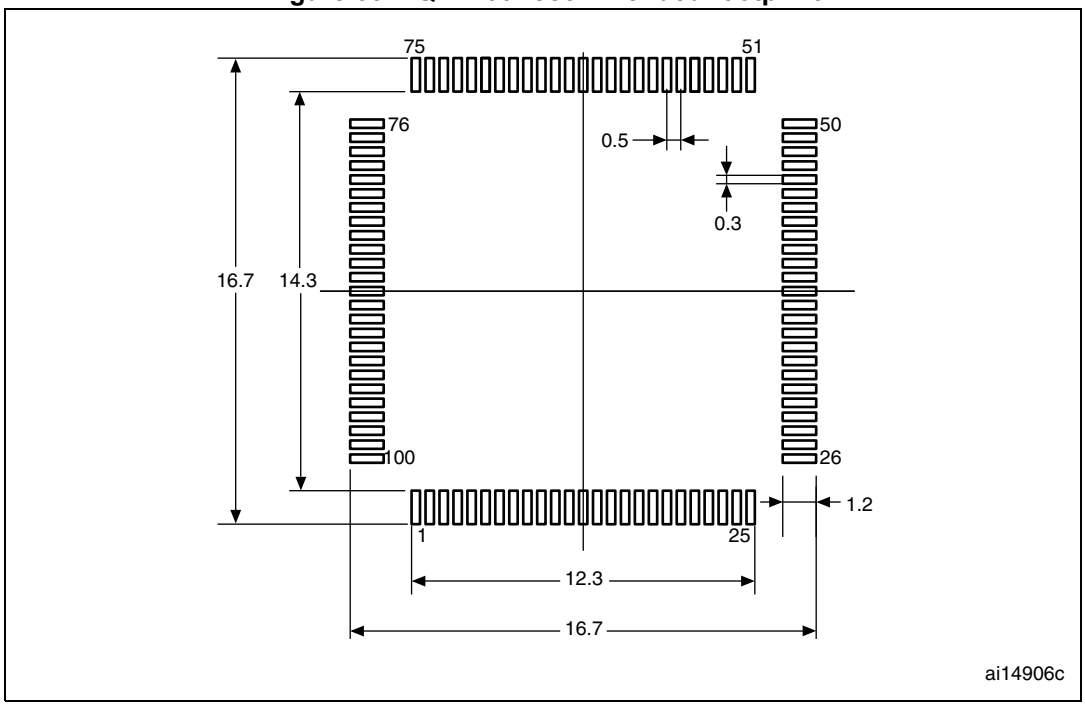
1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

Table 70. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 66. LQFP100 recommended footprint



1. Dimensions are in millimeters.