STMicroelectronics - STM32F103VGT6J Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vgt6j

2.3.21 Serial peripheral interface (SPI)

Up to three SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full-duplex and simplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes.

All SPIs can be served by the DMA controller.

2.3.22 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available, that can be operated in master or slave mode. These interfaces can be configured to operate with 16/32 bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 48 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

2.3.23 SDIO

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.
The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is also fully compliant with the CE-ATA digital protocol Rev1.1.

2.3.24 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

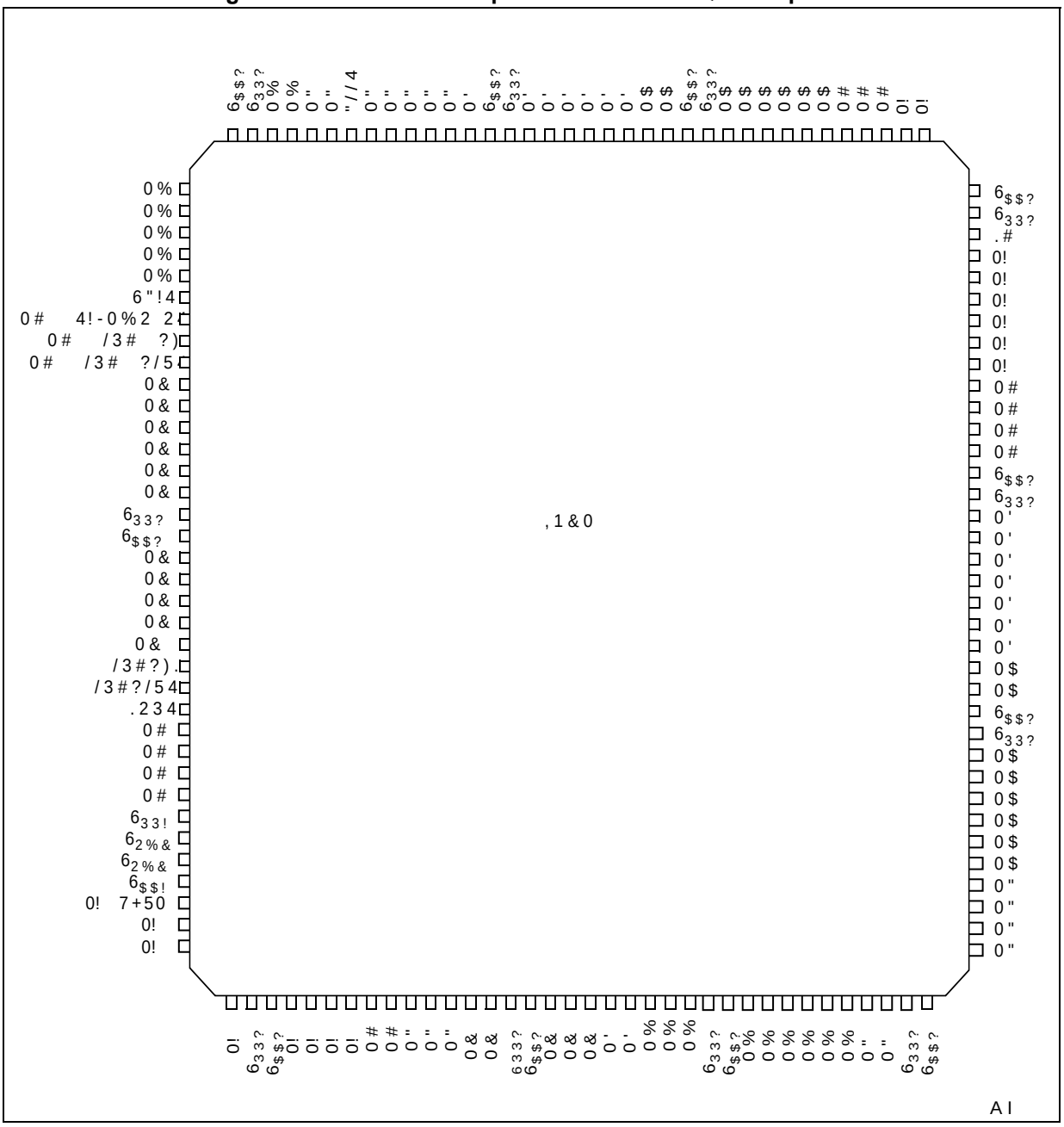
2.3.25 Universal serial bus (USB)

The STM32F103xF and STM32F103xG performance line embed a USB device peripheral compatible with the USB full-speed 12 Mbs. The USB interface implements a full-speed (12 Mbit/s) function interface. It has software-configurable endpoint setting and suspend/resume support. The dedicated 48 MHz clock is generated from the internal main PLL (the clock source must use a HSE crystal oscillator).

2.3.26 GPIOs (general-purpose inputs/outputs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high current-capable.

Figure 4. STM32F103xF/G performance line LQFP144 pinout



1. The above figure shows the package top view.

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
H3	10	17	28	PC2	I/O		PC2	ADC123_IN12	-
H4	11	18	29	PC3	I/O		PC3	ADC123_IN13	-
J1	12	19	30	V_{SSA}	S		V_{SSA}	-	-
K1	-	20	31	V_{REF-}	S		V_{REF-}	-	-
L1	-	21	32	V_{REF+}	S		V_{REF+}	-	-
M1	13	22	33	V_{DDA}	S		V_{DDA}	-	-
J2	14	23	34	PA0-WKUP	I/O		PA0	WKUP/USART2_CTS(8) / ADC123_IN0 / TIM2_CH1_ETR / TIM5_CH1 / TIM8_ETR	-
K2	15	24	35	PA1	I/O		PA1	USART2_RTS(7) / ADC123_IN1 / TIM5_CH2 / TIM2_CH2(7)	-
L2	16	25	36	PA2	I/O		PA2	USART2_TX(7) / TIM5_CH3 / ADC123_IN2 / TIM9_CH1 / TIM2_CH3 (7)	-
M2	17	26	37	PA3	I/O		PA3	USART2_RX(7) / TIM5_CH4 / ADC123_IN3 / TIM2_CH4(7)/ TIM9_CH2	-
G4	18	27	38	V_{SS_4}	S		V_{SS_4}	-	-
F4	19	28	39	V_{DD_4}	S		V_{DD_4}	-	-
J3	20	29	40	PA4	I/O		PA4	SPI1_NSS(7) / USART2_CK(7) / DAC_OUT1 / ADC12_IN4	-
K3	21	30	41	PA5	I/O		PA5	SPI1_SCK(7) / DAC_OUT2 / ADC12_IN5	-
L3	22	31	42	PA6	I/O		PA6	SPI1_MISO(7) / TIM8_BKIN / ADC12_IN6 / TIM3_CH1(7)/ TIM13_CH1	TIM1_BKIN
M3	23	32	43	PA7	I/O		PA7	SPI1_MOSI(7)/ TIM8_CH1N / ADC12_IN7 / TIM3_CH2(7) / TIM14_CH1	TIM1_CH1N
J4	24	33	44	PC4	I/O		PC4	ADC12_IN14	-
K4	25	34	45	PC5	I/O		PC5	ADC12_IN15	-
L4	26	35	46	PB0	I/O		PB0	ADC12_IN8 / TIM3_CH3 / TIM8_CH2N	TIM1_CH2N

Table 6. FSMC pin definition

Pins	FSMC					LQFP100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PE2	-	-	A23	A23	-	Yes
PE3	-	-	A19	A19	-	Yes
PE4	-	-	A20	A20	-	Yes
PE5	-	-	A21	A21	-	Yes
PE6	-	-	A22	A22	-	Yes
PF0	A0	A0	A0	-	-	-
PF1	A1	A1	A1	-	-	-
PF2	A2	A2	A2	-	-	-
PF3	A3	-	A3	-	-	-
PF4	A4	-	A4	-	-	-
PF5	A5	-	A5	-	-	-
PF6	NIORD	NIORD		-	-	-
PF7	NREG	NREG		-	-	-
PF8	NIOWR	NIOWR		-	-	-
PF9	CD	CD		-	-	-
PF10	INTR	INTR		-	-	-
PF11	NIOS16	NIOS16		-	-	-
PF12	A6	-	A6	-	-	-
PF13	A7	-	A7	-	-	-
PF14	A8	-	A8	-	-	-
PF15	A9	-	A9	-	-	-
PG0	A10	-	A10	-	-	-
PG1	-	-	A11	-	-	-
PE7	D4	D4	D4	DA4	D4	Yes
PE8	D5	D5	D5	DA5	D5	Yes
PE9	D6	D6	D6	DA6	D6	Yes
PE10	D7	D7	D7	DA7	D7	Yes
PE11	D8	D8	D8	DA8	D8	Yes
PE12	D9	D9	D9	DA9	D9	Yes
PE13	D10	D10	D10	DA10	D10	Yes
PE14	D11	D11	D11	DA11	D11	Yes
PE15	D12	D12	D12	DA12	D12	Yes
PD8	D13	D13	D13	DA13	D13	Yes

Table 6. FSMC pin definition (continued)

Pins	FSMC					LQFP100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11	-	-	A16	A16	CLE	Yes
PD12	-	-	A17	A17	ALE	Yes
PD13	-	-	A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2	-	-	A12	-	-	-
PG3	-	-	A13	-	-	-
PG4	-	-	A14	-	-	-
PG5	-	-	A15	-	-	-
PG6	-	-	-	-	INT2	-
PG7	-	-	-	-	INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3	-	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	-	NE1	NE1	NCE2	Yes
PG9	-	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	NCE4_2	-	-	-	-
PG12	-	-	NE4	NE4	-	-
PG13	-	-	A24	A24	-	-
PG14	-	-	A25	A25	-	-
PB7	-	-	NADV	NADV	-	Yes
PE0	-	-	NBL0	NBL0	-	Yes
PE1	-	-	NBL1	NBL1	-	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

4 Memory mapping

The memory map is shown in *Figure 7*.

Table 9. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	150	°C

5.3 Operating conditions

5.3.1 General operating conditions

Table 10. General operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	72	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	0	36	
f_{PCLK2}	Internal APB2 clock frequency	-	0	72	
V_{DD}	Standard operating voltage	-	2	3.6	V
V_{DDA}(1)	Analog operating voltage (ADC not used)	Must be the same potential as V_{DD}(2)	2	3.6	V
	Analog operating voltage (ADC used)		2.4	3.6	
V_{BAT}	Backup operating voltage	-	1.8	3.6	V
P_D	Power dissipation at T_A = 85 °C for suffix 6 or T_A = 105 °C for suffix 7(3)	LQFP144	-	666	mW
		LQFP100	-	434	
		LQFP64	-	444	
		LFBGA144	-	500	
T_A	Ambient temperature for 6 suffix version	Maximum power dissipation	–40	85	°C
		Low-power dissipation(4)	–40	105	
	Ambient temperature for 7 suffix version	Maximum power dissipation	–40	105	°C
		Low-power dissipation(4)	–40	125	
T_J	Junction temperature range	6 suffix version	–40	105	°C
		7 suffix version	–40	125	

1. When the ADC is used, refer to *Table 62: ADC characteristics*.
2. It is recommended to power V_{DD} and V_{DDA} from the same source. A maximum difference of 300 mV between V_{DD} and V_{DDA} can be tolerated during power-up and operation.
3. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 129*).
4. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed $T_J$max (see *Table 6.5: Thermal characteristics on page 129*).

Table 16. Maximum current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	External clock(2), all peripherals enabled	72 MHz	47.5	48.5	mA
			48 MHz	34	35	
			36 MHz	27.5	27.5	
			24 MHz	20	20.5	
			16 MHz	15	16	
			8 MHz	9	11	
		External clock(2), all peripherals disabled	72 MHz	9.5	11.2	
			48 MHz	7.7	9.5	
			36 MHz	6.9	8.5	
			24 MHz	5.9	7.8	
			16 MHz	5.4	7.2	
			8 MHz	4.7	6.4	

1. Guaranteed by characterization results, not tested in production at V_{DD} max, f_{HCLK} max with peripherals enabled.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 16. Typical current consumption in Stop mode with regulator in low-power mode versus temperature at different V_{DD} values

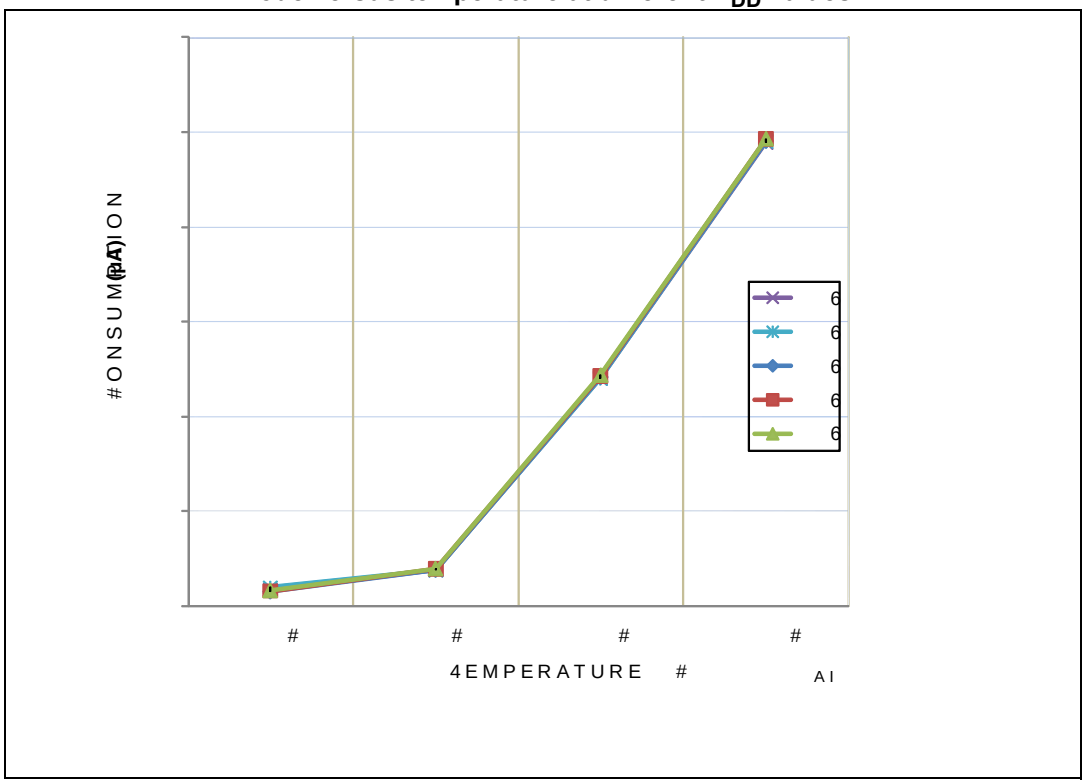


Figure 17. Typical current consumption in Standby mode versus temperature at different V_{DD} values

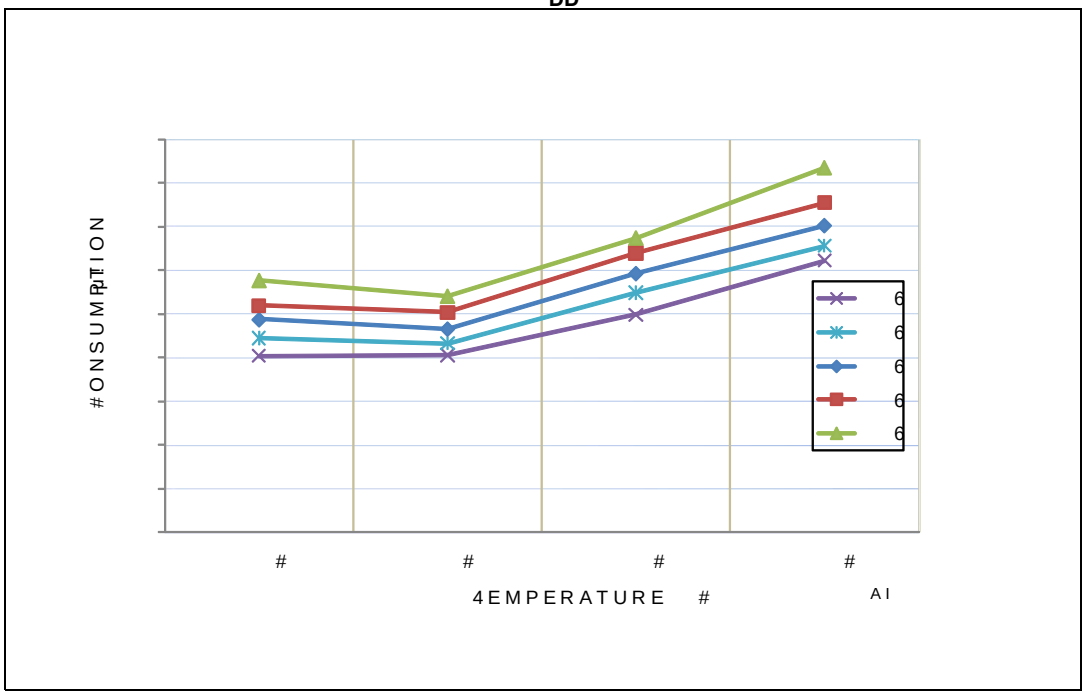
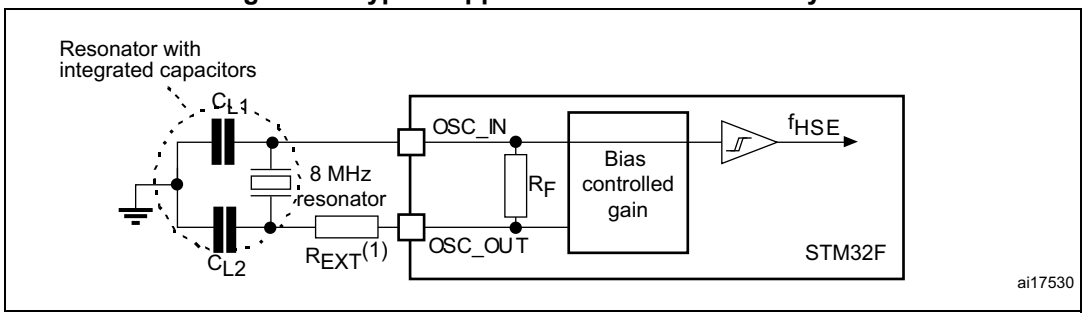


Figure 20. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed internal (LSI) RC oscillator

Table 26. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 27* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

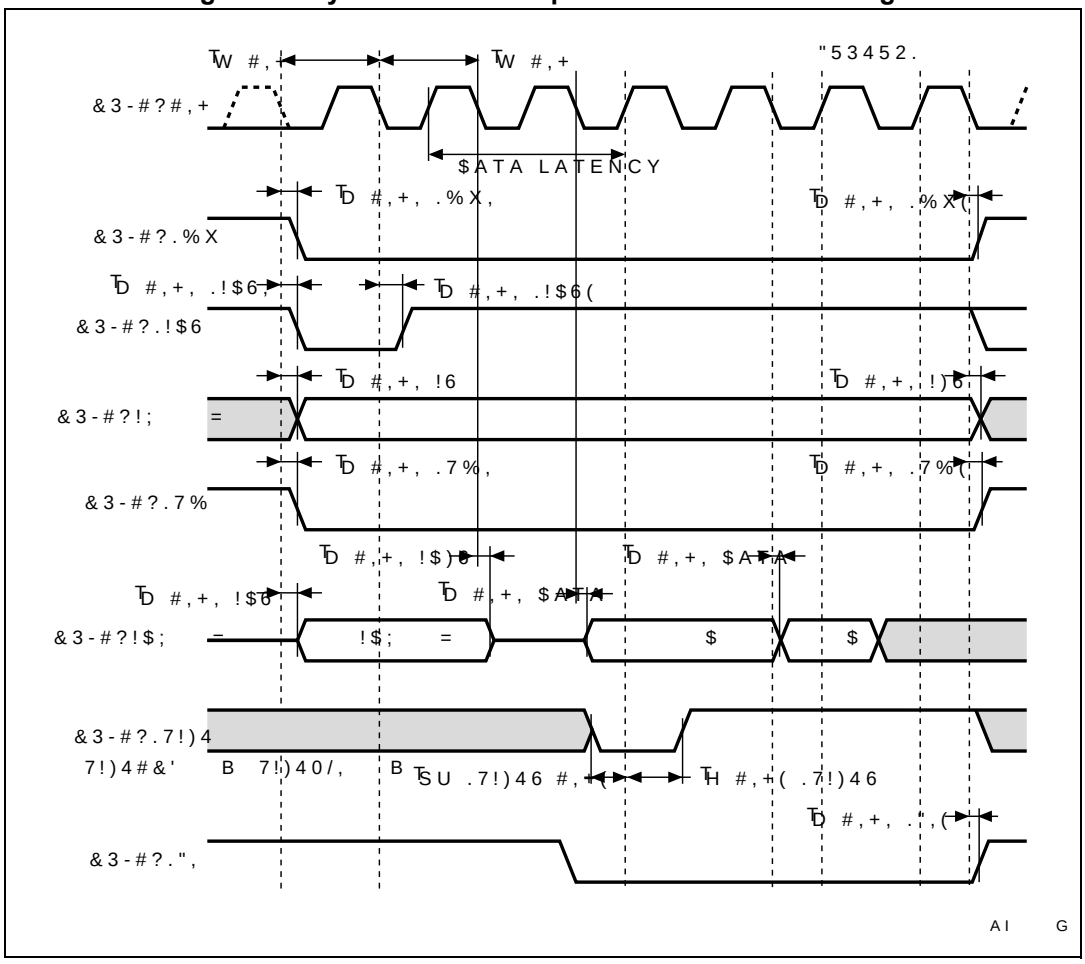
All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

Figure 27. Synchronous multiplexed PSRAM write timings



1. C_L = 15 pF.

Figure 29. Synchronous non-multiplexed PSRAM write timings

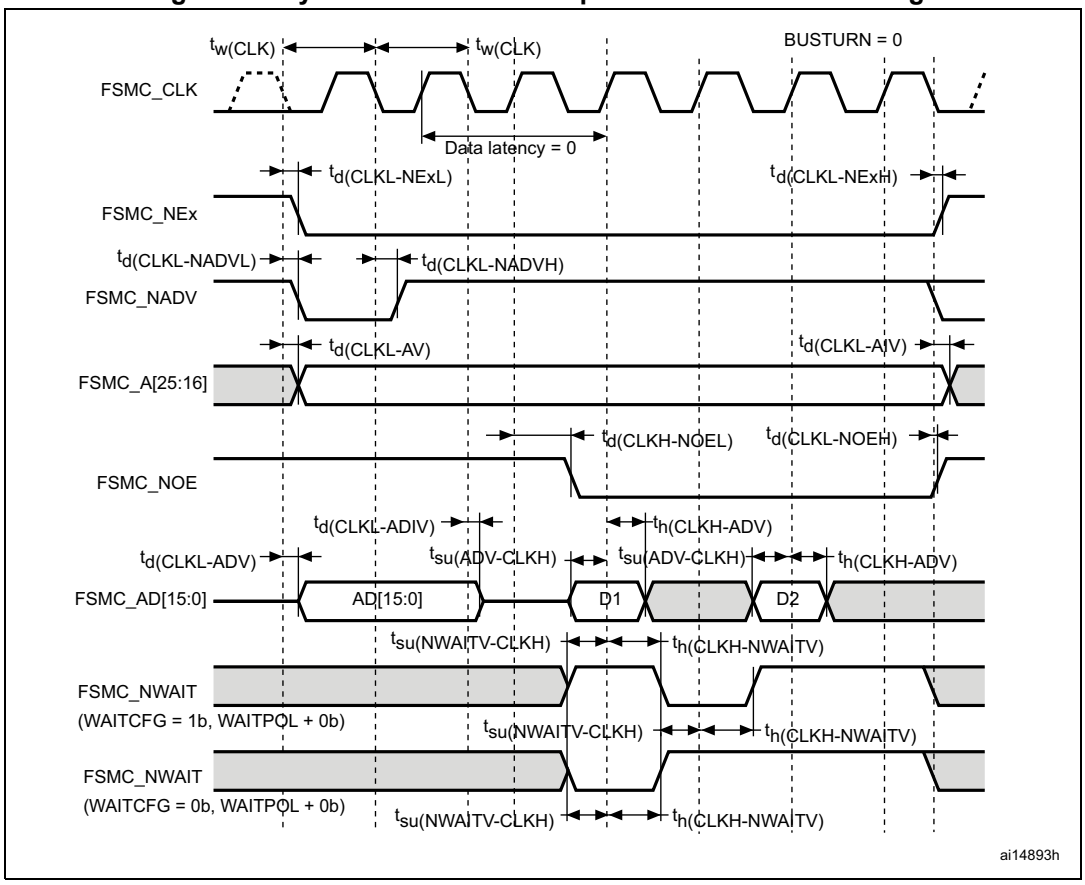


Table 39. Synchronous non-multiplexed PSRAM write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.6	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	0.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	1.5	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	1	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	0.5	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 16...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 16...25)	1.5	-	ns
$t_{d(CLKL-NWEL)}$	FSMC_CLK low to FSMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	FSMC_CLK low to FSMC_NWE high	1.5	-	ns
$t_{d(CLKL-Data)}$	FSMC_D[15:0] valid data after FSMC_CLK low	-	2.5	ns
$t_{d(CLKL-NBLH)}$	FSMC_CLK low to FSMC_NBL high	0.5	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

Table 41. Switching characteristics for PC Card/CF read and write cycles in I/O space

Symbol	Parameter	Min	Max	Unit
$tw_{(NIOWR)}$	FSMC_NIOWR low width	8 THCLK	-	ns
$tv_{(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	5 THCLK - 4	ns
$th_{(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	11THCLK - 7	-	ns
$td_{(NCE4_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	5THCLK + 1	ns
$th_{(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	5THCLK - 2.5	-	ns
$td_{(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	5THCLK - 0.5	ns
$th_{(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	5 THCLK - 0.5	-	ns
$tw_{(NIORD)}$	FSMC_NIORD low width	8THCLK	-	ns
$tsu_{(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	28	-	ns
$td_{(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	3	-	ns

NAND controller waveforms and timings

Figure 36 through *Figure 39* represent synchronous waveforms and *Table 43* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x00;
- COM.FSMC_WaitSetupTime = 0x02;
- COM.FSMC_HoldSetupTime = 0x01;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x00;
- ATT.FSMC_WaitSetupTime = 0x02;
- ATT.FSMC_HoldSetupTime = 0x01;
- ATT.FSMC_HiZSetupTime = 0x00;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 47. SPI timing diagram - slave mode and CPHA = 0

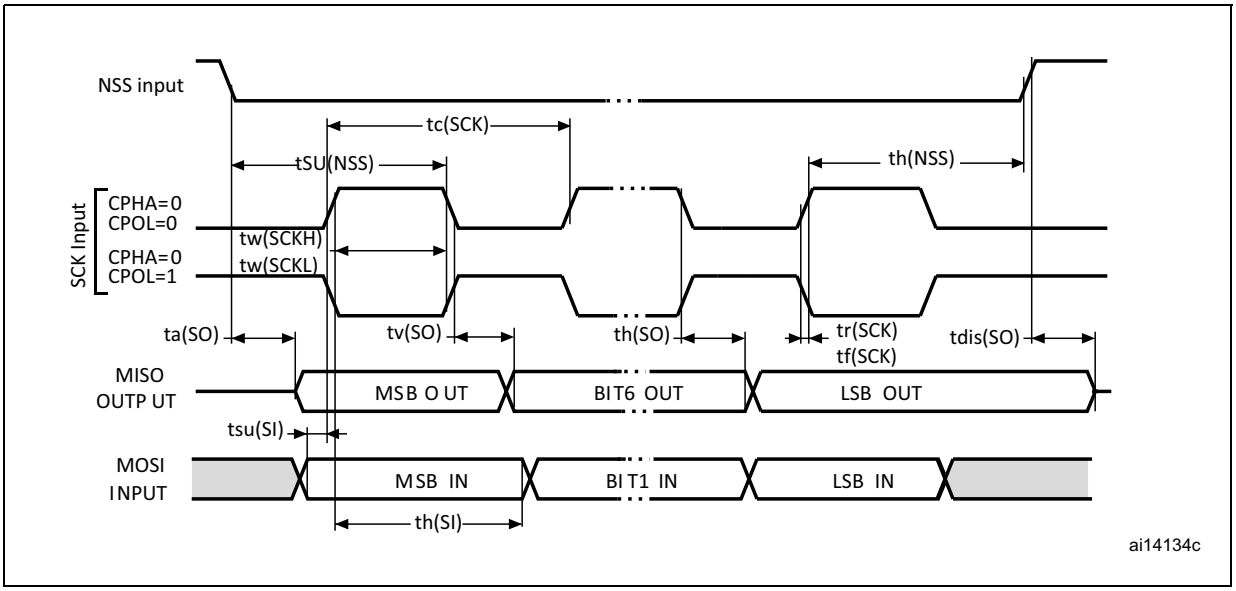
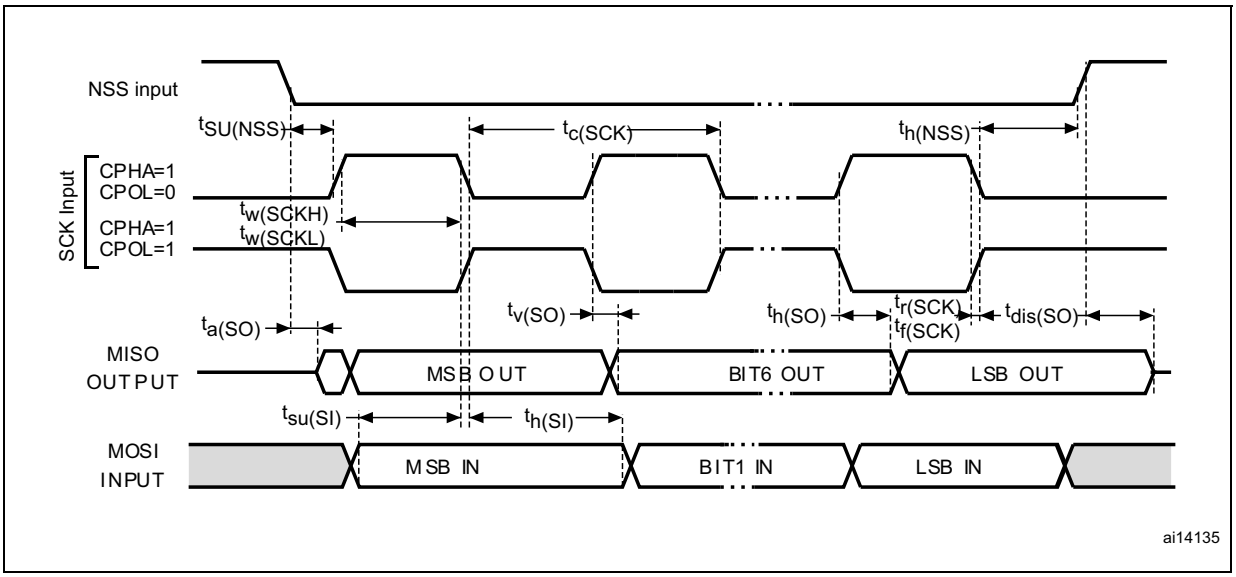


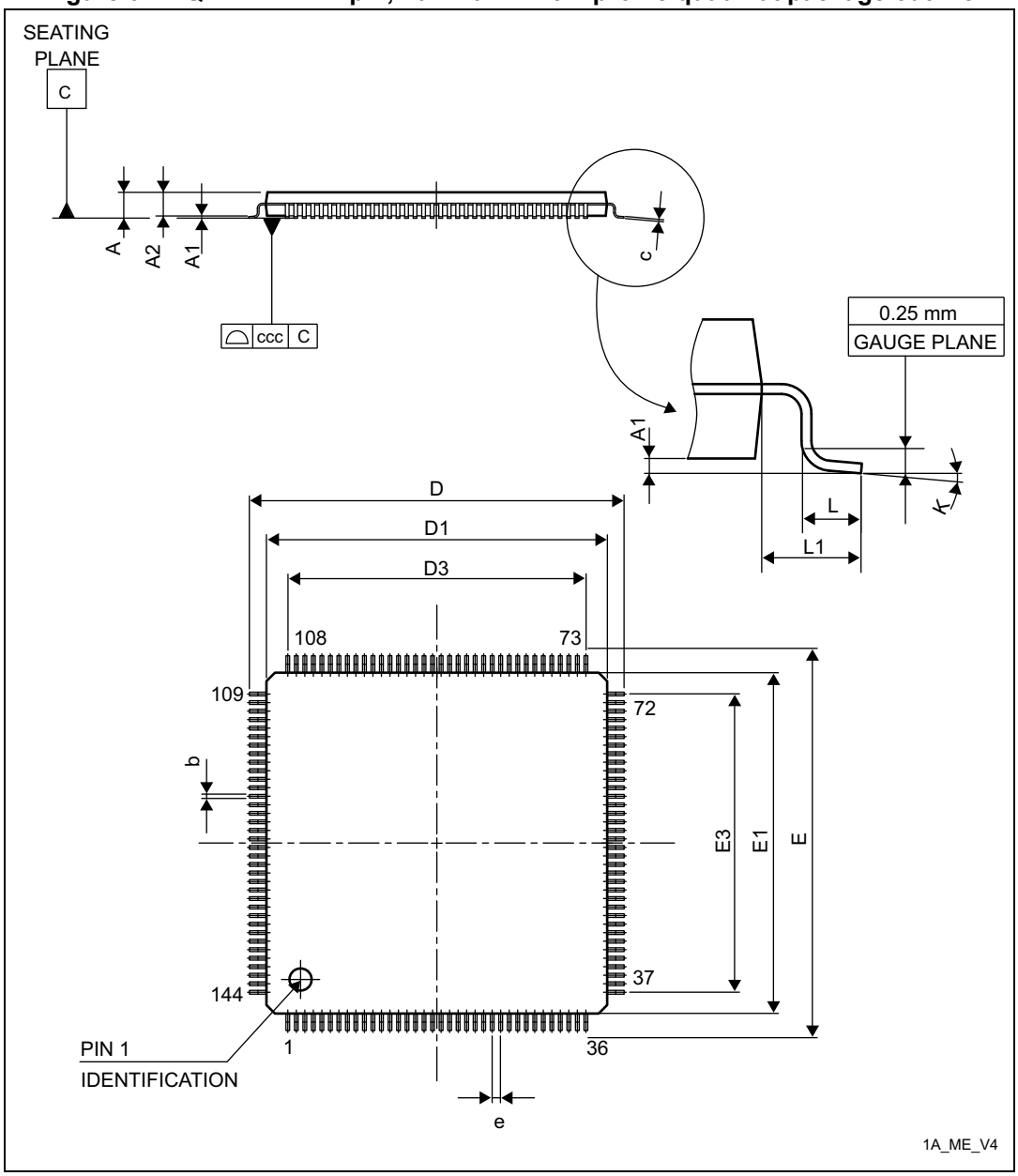
Figure 48. SPI timing diagram - slave mode and CPHA = 1(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

6.2 LQFP144 package information

Figure 62. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package outline



1. Drawing is not to scale.

6.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 73: STM32F103xF and STM32F103xG ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xF and STM32F103xG at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 72* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 73: STM32F103xF and STM32F103xG ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 72* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 115 °C + (46 °C/W × 134 mW) = 115 °C + 6.2 °C = 121.2 °C

This is within the range of the suffix 7 version parts (–40 < T_J < 125 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 7: Part numbering*).

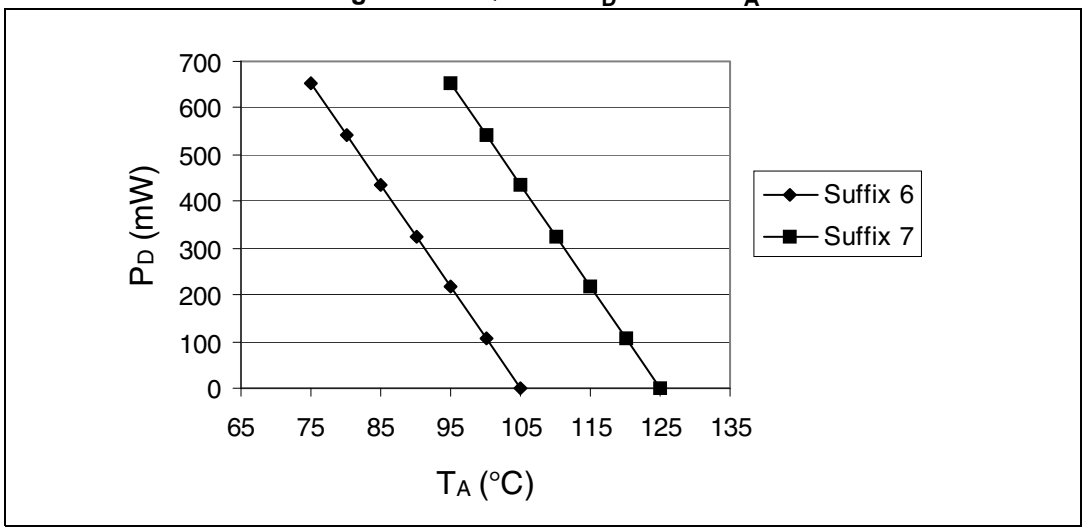



Figure 71. LQFP100 P_D max vs. T_A