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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	80
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103vgt7

2 Description

The STM32F103xF and STM32F103xG performance line family incorporates the high-performance ARM® Cortex®-M3 32-bit RISC core operating at a 72 MHz frequency, high-speed embedded memories (Flash memory up to 1 Mbyte and SRAM up to 96 Kbytes), and an extensive range of enhanced I/Os and peripherals connected to two APB buses. All devices offer three 12-bit ADCs, ten general-purpose 16-bit timers plus two PWM timers, as well as standard and advanced communication interfaces: up to two I^2Cs, three SPIs, two I^2Ss, one SDIO, five USARTs, an USB and a CAN.

The STM32F103xF/G XL-density performance line family operates in the –40 to +105 °C temperature range, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F103xF/G high-density performance line microcontroller family suitable for a wide range of applications such as motor drives, application control, medical and handheld equipment, PC and gaming peripherals, GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems and video intercom.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.19 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.20 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F103xF and STM32F103xG performance line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
M4	27	36	47	PB1	I/O		PB1	ADC12_IN9 / TIM3_CH4(7) / TIM8_CH3N	TIM1_CH3N
J5	28	37	48	PB2	I/O	FT	PB2/BOOT1	-	-
M5	-	-	49	PF11	I/O	FT	PF11	FSMC_NIOS16	-
L5	-	-	50	PF12	I/O	FT	PF12	FSMC_A6	-
H5	-	-	51	V_{SS_6}	S		V_{SS_6}	-	-
G5	-	-	52	V_{DD_6}	S		V_{DD_6}	-	-
K5	-	-	53	PF13	I/O	FT	PF13	FSMC_A7	-
M6	-	-	54	PF14	I/O	FT	PF14	FSMC_A8	-
L6	-	-	55	PF15	I/O	FT	PF15	FSMC_A9	-
K6	-	-	56	PG0	I/O	FT	PG0	FSMC_A10	-
J6	-	-	57	PG1	I/O	FT	PG1	FSMC_A11	-
M7	-	38	58	PE7	I/O	FT	PE7	FSMC_D4	TIM1_ETR
L7	-	39	59	PE8	I/O	FT	PE8	FSMC_D5	TIM1_CH1N
K7	-	40	60	PE9	I/O	FT	PE9	FSMC_D6	TIM1_CH1
H6	-	-	61	V_{SS_7}	S		V_{SS_7}	-	-
G6	-	-	62	V_{DD_7}	S		V_{DD_7}	-	-
J7	-	41	63	PE10	I/O	FT	PE10	FSMC_D7	TIM1_CH2N
H8	-	42	64	PE11	I/O	FT	PE11	FSMC_D8	TIM1_CH2
J8	-	43	65	PE12	I/O	FT	PE12	FSMC_D9	TIM1_CH3N
K8	-	44	66	PE13	I/O	FT	PE13	FSMC_D10	TIM1_CH3
L8	-	45	67	PE14	I/O	FT	PE14	FSMC_D11	TIM1_CH4
M8	-	46	68	PE15	I/O	FT	PE15	FSMC_D12	TIM1_BKIN
M9	29	47	69	PB10	I/O	FT	PB10	I2C2_SCL / USART3_TX(7)	TIM2_CH3
M10	30	48	70	PB11	I/O	FT	PB11	I2C2_SDA / USART3_RX(7)	TIM2_CH4
H7	31	49	71	V_{SS_1}	S		V_{SS_1}	-	-
G7	32	50	72	V_{DD_1}	S		V_{DD_1}	-	-
M11	33	51	73	PB12	I/O	FT	PB12	SPI2_NSS / I2S2_WS / I2C2_SMBA / USART3_CK(7) / TIM1_BKIN(7)	-

Figure 16. Typical current consumption in Stop mode with regulator in low-power mode versus temperature at different V_{DD} values

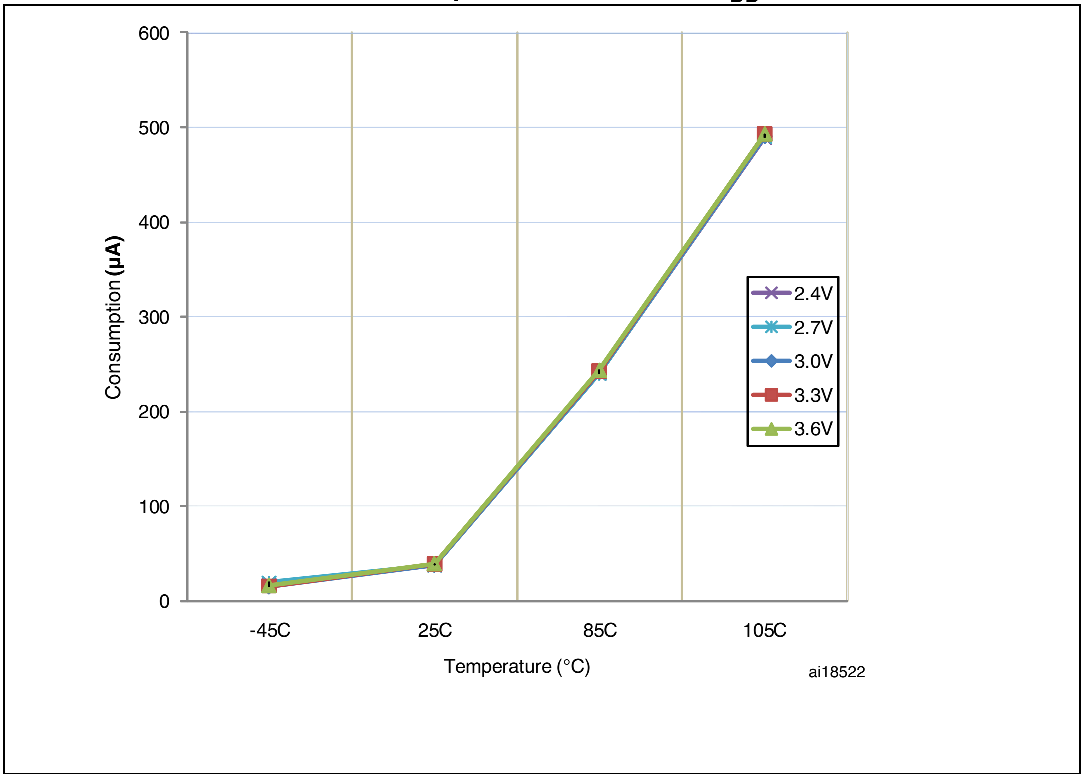
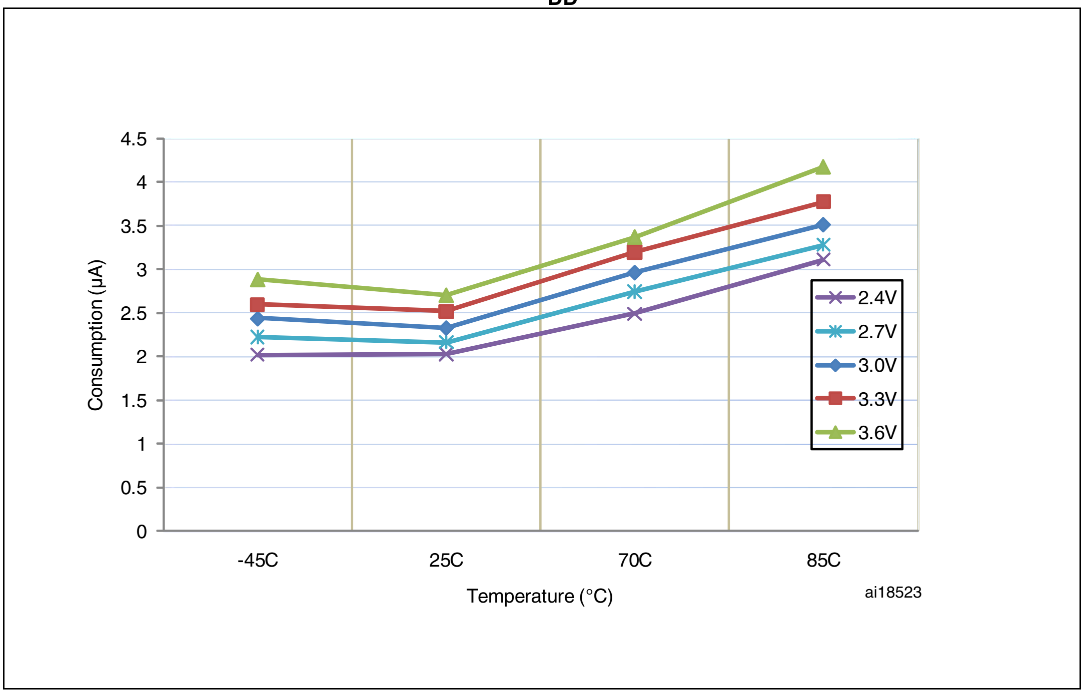


Figure 17. Typical current consumption in Standby mode versus temperature at different V_{DD} values



Low-speed external clock generated from a crystal/ceramic resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 24*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 24. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)(2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R_F	Feedback resistor	-		-	5	-	MΩ
C(2)	Recommended load capacitance versus equivalent serial resistance of the crystal (R_S)	R_S = 30 kΩ		-	-	15	pF
I_2	LSE driving current	V_{DD} = 3.3 V, V_{IN} = V_{SS}		-	-	1.4	µA
g_m	Oscillator transconductance	-		5	-	-	µA/V
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	T_A = 50 °C	-	1.5	-	s
			T_A = 25 °C	-	2.5	-	
			T_A = 10 °C	-	4	-	
			T_A = 0 °C	-	6	-	
			T_A = -10 °C	-	10	-	
			T_A = -20 °C	-	17	-	
			T_A = -30 °C	-	32	-	
			T_A = -40 °C	-	60	-	

1. Guaranteed by characterization results, not tested in production.
2. Refer to the note and caution paragraphs below the table, and to the application note AN2867 “Oscillator design guide for ST microcontrollers”.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) until a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer, PCB layout and humidity.

Note: *For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 15 pF range selected to match the requirements of the crystal or resonator (see Figure 21). C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.*
Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$ where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Caution: To avoid exceeding the maximum value of C_{L1} and C_{L2} (15 pF) it is strongly recommended to use a resonator with a load capacitance $C_L \leq$ 7 pF. Never use a resonator with a load capacitance of 12.5 pF.
Example: if you choose a resonator with a load capacitance of C_L = 6 pF, and C_{stray} = 2 pF, then C_{L1} = C_{L2} = 8 pF.

Table 30. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min[1]	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Years
		1 kcycle[2] at T_A = 105 °C	10	
		10 kcycles[2] at T_A = 55 °C	20	

1. Guaranteed by characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

Table 32. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$3t_{HCLK}$ + 0.5	$3t_{HCLK}$ + 1.5	ns
$t_{v(NWE\_NE)}$	FSMC_NEx low to FSMC_NWE low	t_{HCLK} + 0.5	t_{HCLK} + 1.5	ns
$t_{w(NWE)}$	FSMC_NWE low time	t_{HCLK} – 0.5	t_{HCLK} + 1	ns
$t_{h(NE\_NWE)}$	FSMC_NWE high to FSMC_NE high hold time	t_{HCLK} – 0.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	t_{HCLK}	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	1.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	t_{HCLK} – 1.5	-	ns
$t_{v(Data\_NE)}$	FSMC_NEx low to Data valid	-	t_{HCLK}	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	t_{HCLK}	-	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	-	0	ns
$t_{w(NADV)}$	FSMC_NADV low time	-	t_{HCLK} + 1.5	ns

1. C_L = 15 pF.

Table 33. Asynchronous multiplexed read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7t_{HCLK}$ + 0.5	$7t_{HCLK}$ + 2	
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK}$ + 0.5	$3t_{HCLK}$ + 1.5	
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK}$ – 1	$4t_{HCLK}$ + 1	
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0.5	-	
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	0	1	
$t_{w(NADV)}$	FSMC_NADV low time	t_{HCLK} + 0.5	t_{HCLK} + 2	
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC NADV high	t_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	t_{HCLK} – 2	-	
$t_{h(BL\_NOE)}$	FSMC_BL time after FSMC_NOE high	0.5	-	
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$4t_{HCLK}$ – 0.5	-	
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$4t_{HCLK}$ – 1	-	
$t_{h(Data\_NE)}$	Data hold time after FSMC_NEx high	0	-	
$t_{h(Data\_NOE)}$	Data hold time after FSMC_NOE high	0	-	

Table 35. Asynchronous multiplexed PSRAM/NOR write timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{h(A\_NWE)}$	Address hold time after FSMC_NWE high	$4t_{HCLK} - 2$	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0.5	ns
$t_{h(BL\_NWE)}$	FSMC_BL hold time after FSMC_NWE high	$t_{HCLK} - 1.5$	-	ns
$t_{v(Data\_NADV)}$	FSMC_NADV high to Data valid	-	$t_{HCLK} + 6$	ns
$t_{h(Data\_NWE)}$	Data hold time after FSMC_NWE high	$t_{HCLK} - 0.5$	-	ns

1. C_L = 15 pF.

Synchronous waveforms and timings

Figure 26 through *Figure 29* represent synchronous waveforms and *Table 37* through *Table 39* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- BurstAccessMode = FSMC_BurstAccessMode_Enable;
- MemoryType = FSMC_MemoryType_CRAM;
- WriteBurst = FSMC_WriteBurst_Enable;
- CLKDivision = 1; (0 is not supported, see the STM32F10xxx reference manual)
- DataLatency = 1 for NOR Flash; DataLatency = 0 for PSRAM

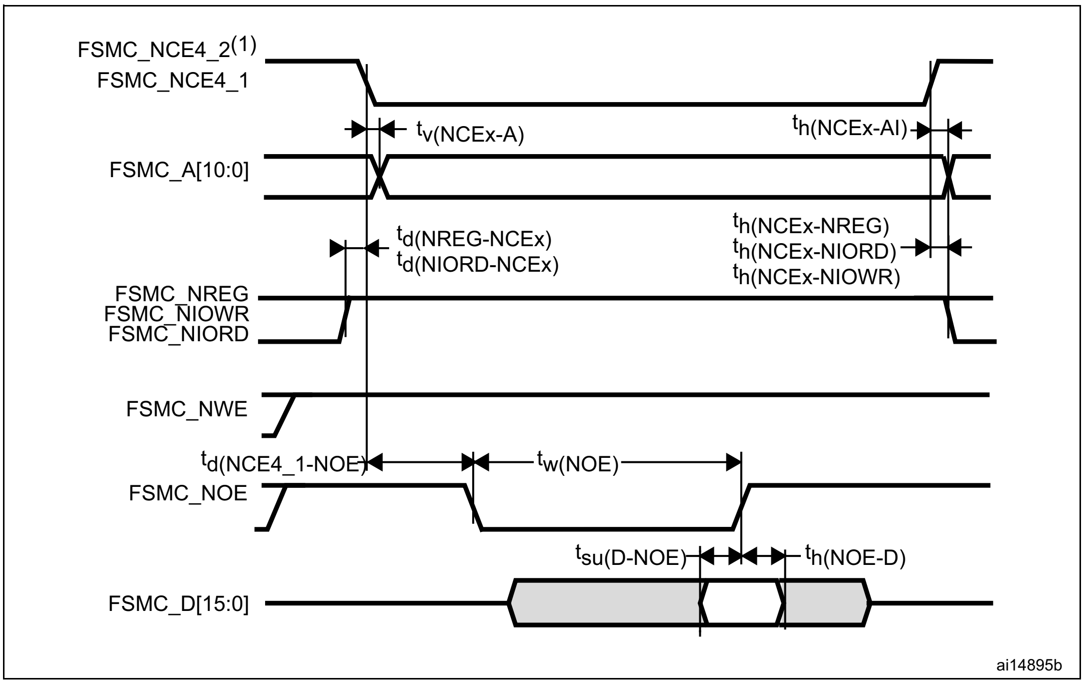
1. C_L = 15 pF.

PC Card/CompactFlash controller waveforms and timings

Figure 30 through *Figure 35* represent synchronous waveforms and *Table 42* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x04;
- COM.FSMC_WaitSetupTime = 0x07;
- COM.FSMC_HoldSetupTime = 0x04;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x04;
- ATT.FSMC_WaitSetupTime = 0x07;
- ATT.FSMC_HoldSetupTime = 0x04;
- ATT.FSMC_HiZSetupTime = 0x00;
- IO.FSMC_SetupTime = 0x04;
- IO.FSMC_WaitSetupTime = 0x07;
- IO.FSMC_HoldSetupTime = 0x04;
- IO.FSMC_HiZSetupTime = 0x00;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 30. PC Card/CompactFlash controller waveforms for common memory read access



1. FSMC_NCE4_2 remains high (inactive during 8-bit access.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 45. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}]		Unit
				8/48 MHz	8/72 MHz	
S_{EMI}	Peak level	$V_{DD} = 3.3$ V, $T_A = 25$ °C, LQFP144 package compliant with IEC 61967-2	0.1 to 30 MHz	8	12	dBμV
			30 to 130 MHz	31	21	
			130 MHz to 1GHz	28	33	
			SAE EMI Level	4	4	-

5.3.12 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 46. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value(1)	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	$T_A = +25$ °C, conforming to JESD22-A114	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	$T_A = +25$ °C, conforming to JESD22-C101	III	500	

1. Guaranteed by characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Figure 40. Standard I/O input characteristics - CMOS port

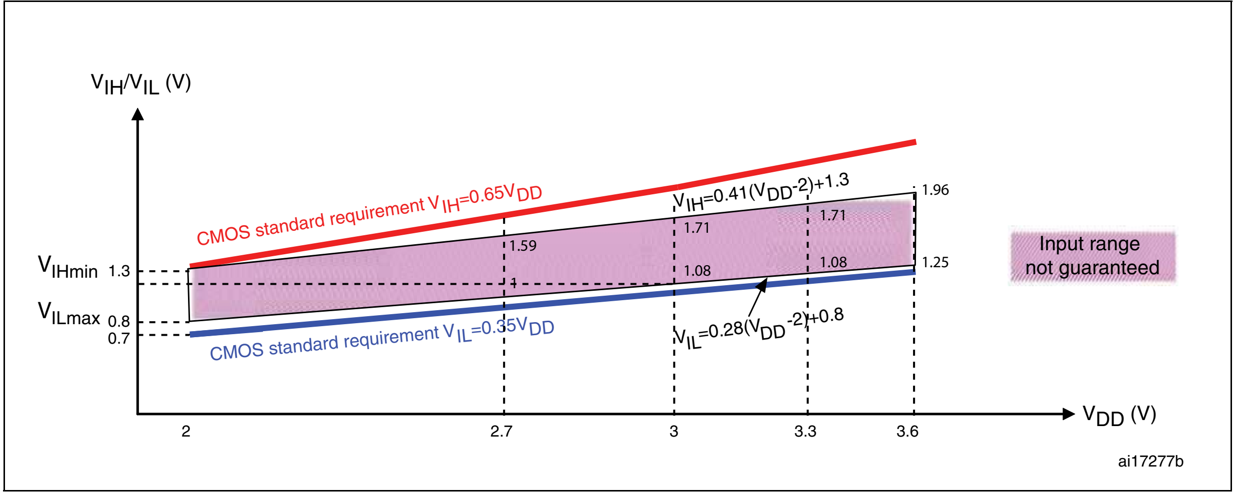


Figure 41. Standard I/O input characteristics - TTL port

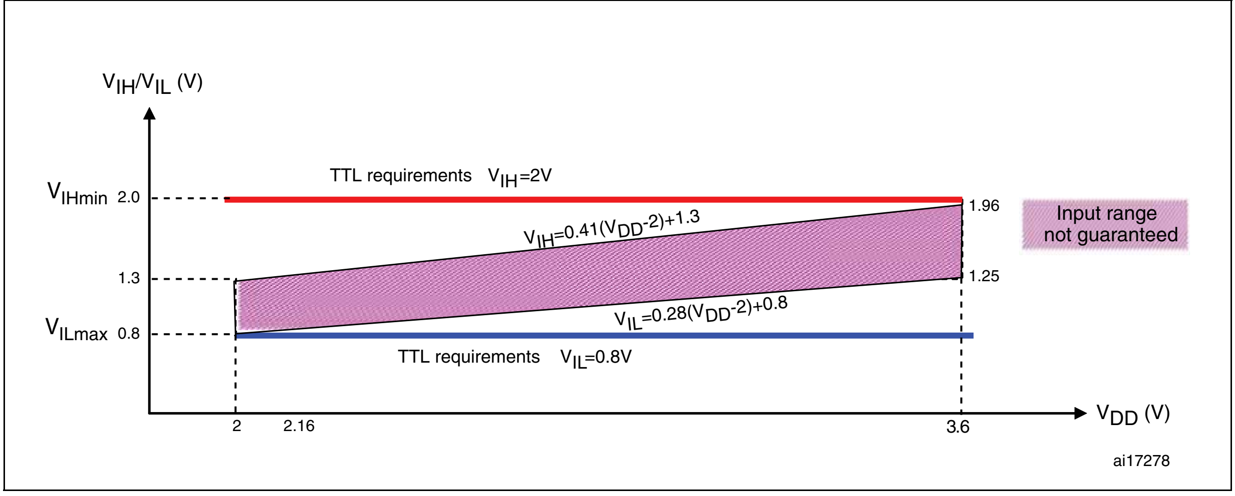
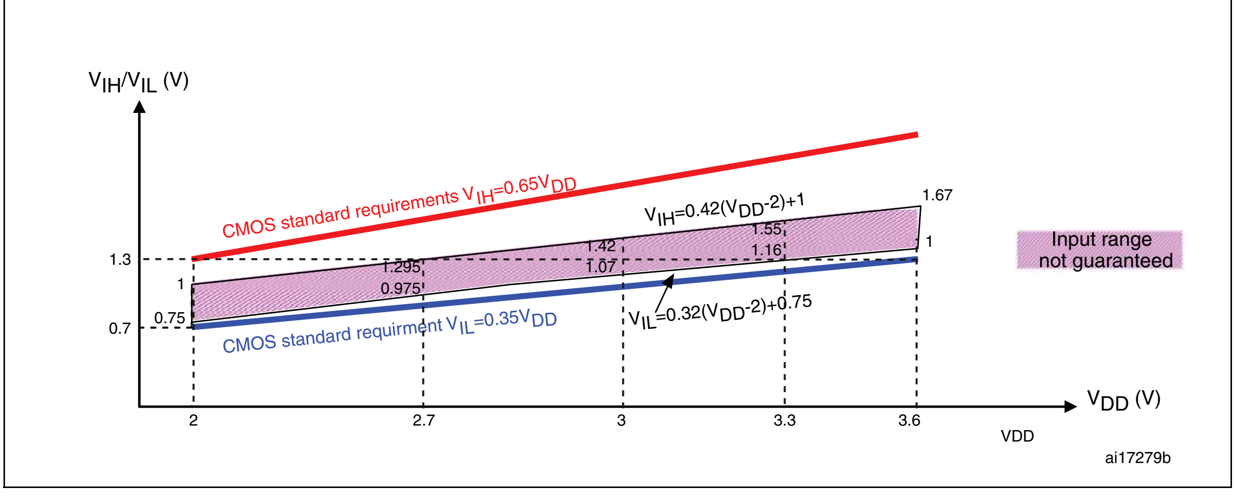


Figure 42. 5 V tolerant I/O input characteristics - CMOS port



Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 44* and *Table 51*, respectively.

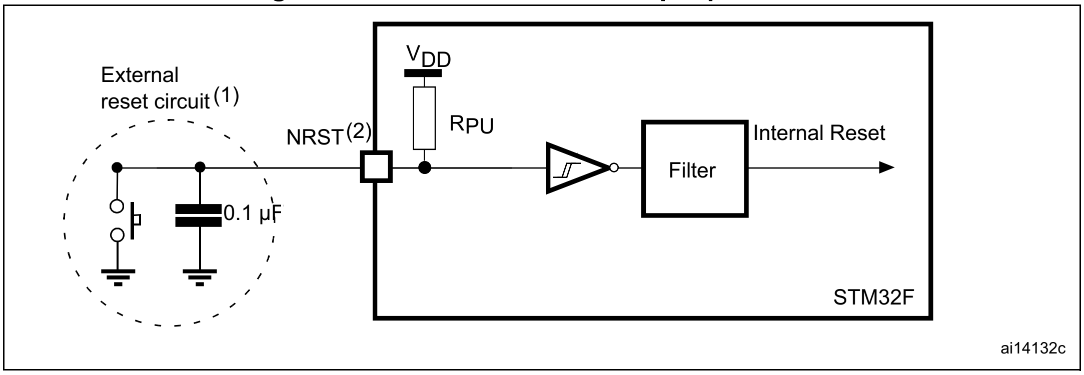
Unless otherwise specified, the parameters given in *Table 51* are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 51. I/O AC characteristics(1)

<table>
<tr><th>MODEx[1:0] bit value(1)</th><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Min</th><th>Max</th><th>Unit</th></tr>
<tr><td rowspan="3">10</td><td>$f_{max(IO)out}$</td><td>Maximum frequency(2)</td><td>C_L = 50 pF, V_{DD} = 2 V to 3.6 V</td><td>-</td><td>2</td><td>MHz</td></tr>
<tr><td>$t_{f(IO)out}$</td><td>Output high to low level fall time</td><td rowspan="2">C_L = 50 pF, V_{DD} = 2 V to 3.6 V</td><td>-</td><td>125(3)</td><td rowspan="2">ns</td></tr>
<tr><td>$t_{r(IO)out}$</td><td>Output low to high level rise time</td><td>-</td><td>125(3)</td></tr>
<tr><td rowspan="3">01</td><td>$f_{max(IO)out}$</td><td>Maximum frequency(2)</td><td>C_L = 50 pF, V_{DD} = 2 V to 3.6 V</td><td>-</td><td>10</td><td>MHz</td></tr>
<tr><td>$t_{f(IO)out}$</td><td>Output high to low level fall time</td><td rowspan="2">C_L = 50 pF, V_{DD} = 2 V to 3.6 V</td><td>-</td><td>25(3)</td><td rowspan="2">ns</td></tr>
<tr><td>$t_{r(IO)out}$</td><td>Output low to high level rise time</td><td>-</td><td>25(3)</td></tr>
<tr><td rowspan="9">11</td><td rowspan="3">$F_{max(IO)out}$</td><td rowspan="3">Maximum frequency(2)</td><td>C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V</td><td>-</td><td>50</td><td>MHz</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V</td><td>-</td><td>30</td><td>MHz</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2 V to 2.7 V</td><td>-</td><td>20</td><td>MHz</td></tr>
<tr><td rowspan="3">$t_{f(IO)out}$</td><td rowspan="3">Output high to low level fall time</td><td>C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V</td><td>-</td><td>5(3)</td><td rowspan="6">ns</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V</td><td>-</td><td>8(3)</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2 V to 2.7 V</td><td>-</td><td>12(3)</td></tr>
<tr><td rowspan="3">$t_{r(IO)out}$</td><td rowspan="3">Output low to high level rise time</td><td>C_L = 30 pF, V_{DD} = 2.7 V to 3.6 V</td><td>-</td><td>5(3)</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2.7 V to 3.6 V</td><td>-</td><td>8(3)</td></tr>
<tr><td>C_L = 50 pF, V_{DD} = 2 V to 2.7 V</td><td>-</td><td>12(3)</td></tr>
<tr><td>-</td><td>t_{EXTIpw}</td><td>Pulse width of external signals detected by the EXTI controller</td><td>-</td><td>10</td><td>-</td><td>ns</td></tr>
</table>

1. The I/O speed is configured using the MODEx[1:0] bits. Refer to the STM32F10xxx reference manual for a description of GPIO Port configuration register.
2. The maximum frequency is defined in *Figure 44*.
3. Guaranteed by design, not tested in production.

Figure 45. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 52*. Otherwise the reset will not be taken into account by the device.

5.3.16 TIM timer characteristics

The parameters given in *Table 53* are guaranteed by design.

Refer to *Section 5.3.14: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 53. TIMx(1) characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	-	1	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	13.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TIMxCLK}/2$	MHz
		$f_{TIMxCLK}$ = 72 MHz	0	36	MHz
Res_{TIM}	Timer resolution	-	-	16	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	-	1	65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	0.0139	910	µs
t_{MAX_COUNT}	Maximum possible count	-	-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 72 MHz	-	59.6	s

1. TIMx is used as a general term to refer to the TIM1, TIM2, TIM3 and TIM4 timers.

I^2S - SPI characteristics

Unless otherwise specified, the parameters given in *Table 56* for SPI or in *Table 57* for I^2S are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

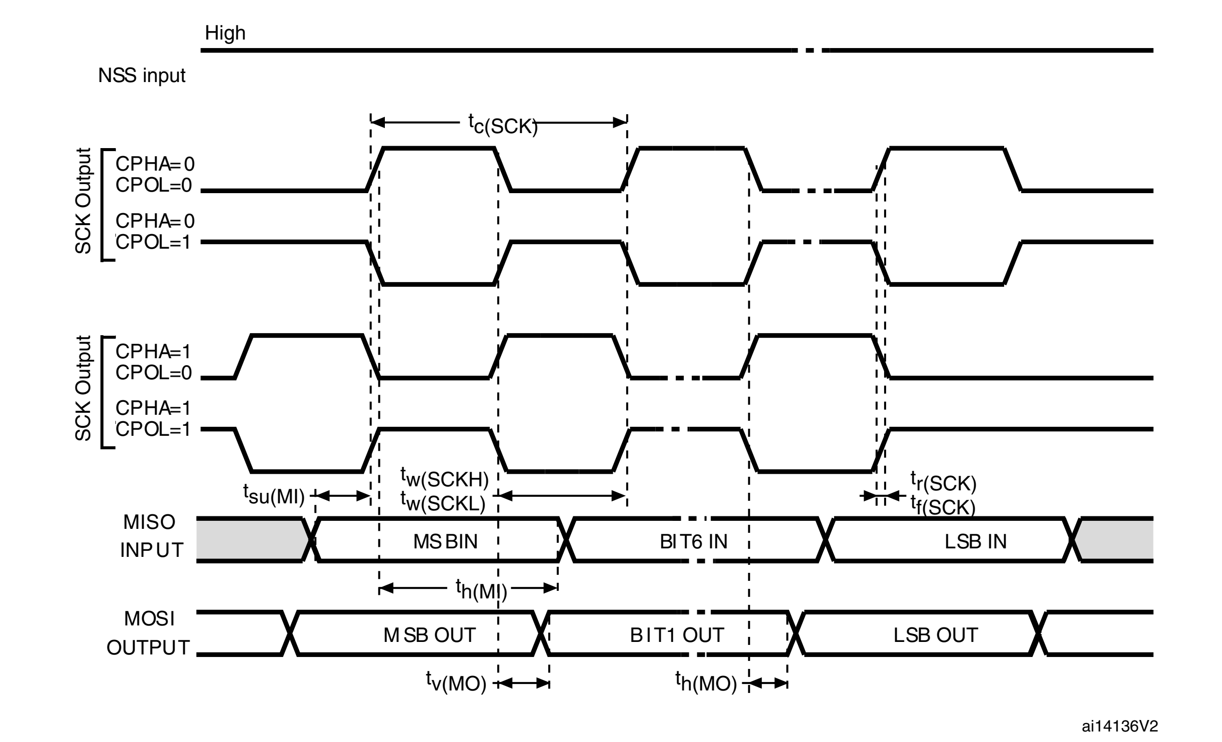
Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I^2S).

Table 56. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode	-	18	MHz
		Slave mode	-	18	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI clock rise and fall time	Capacitive load: C = 30 pF	-	8	ns
DuCy(SCK)	SPI slave input clock duty cycle	Slave mode	30	70	%
$t_{su(NSS)}$(1)	NSS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(NSS)}$(1)	NSS hold time	Slave mode	$2t_{PCLK}$	-	
$t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1)	SCK high and low time	Master mode, f_{PCLK} = 36 MHz, presc = 4	50	60	
$t_{su(MI)}$(1) $t_{su(SI)}$(1)	Data input setup time	Master mode	5	-	
		Slave mode	5	-	
$t_{h(MI)}$(1)	Data input hold time	Master mode	5	-	
$t_{h(SI)}$(1)		Slave mode	4	-	
$t_{a(SO)}$(1)(2)	Data output access time	Slave mode, f_{PCLK} = 20 MHz	0	$3t_{PCLK}$	
$t_{dis(SO)}$(1)(3)	Data output disable time	Slave mode	2	10	
$t_{v(SO)}$(1)	Data output valid time	Slave mode (after enable edge)	-	25	
$t_{v(MO)}$(1)	Data output valid time	Master mode (after enable edge)	-	5	
$t_{h(SO)}$(1)	Data output hold time	Slave mode (after enable edge)	15	-	
$t_{h(MO)}$(1)		Master mode (after enable edge)	2	-	

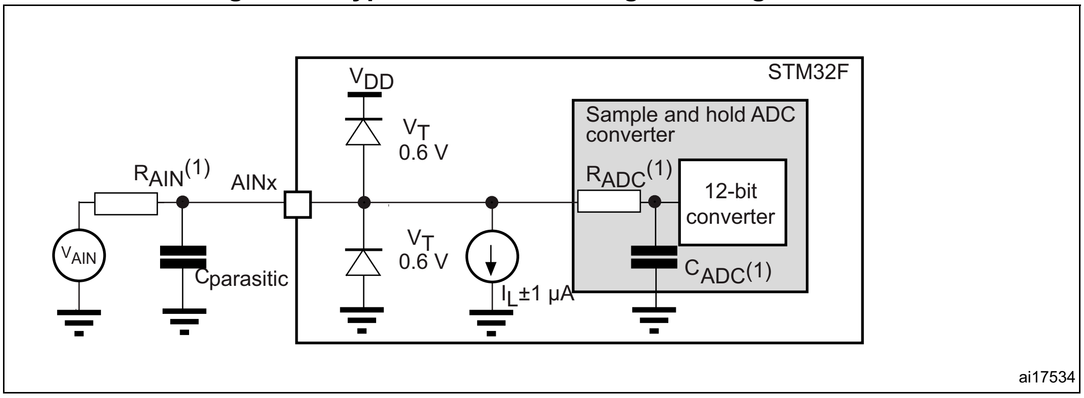
1. Guaranteed by characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 49. SPI timing diagram - master mode(1)



1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

Figure 56. Typical connection diagram using the ADC

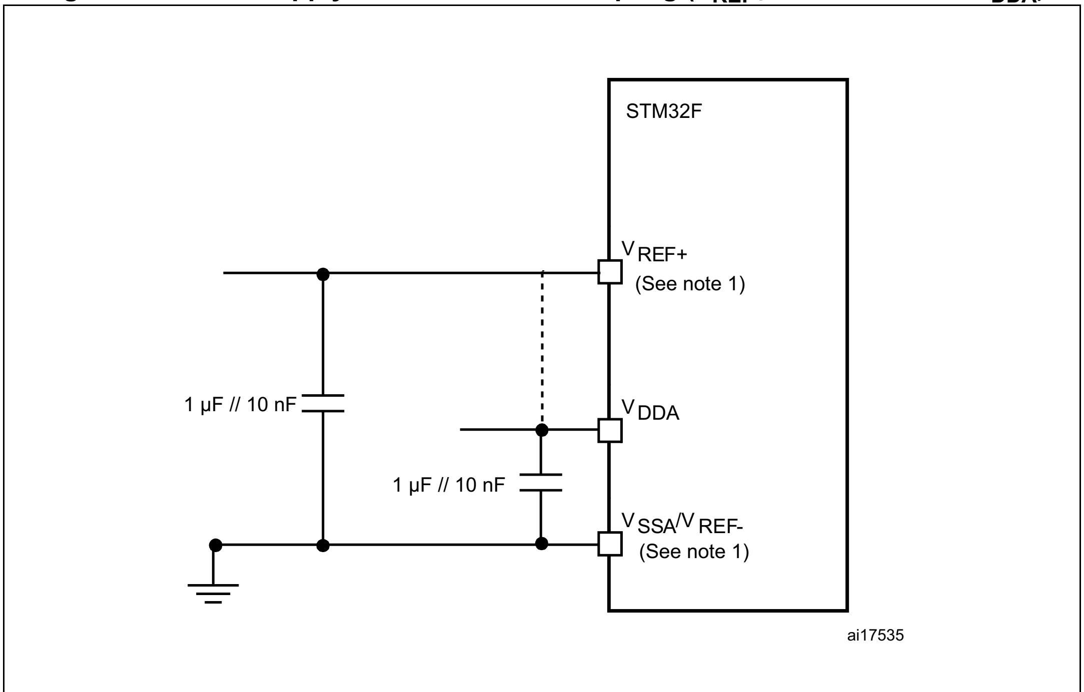


1. Refer to *Table 62* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 57* or *Figure 58*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 57. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



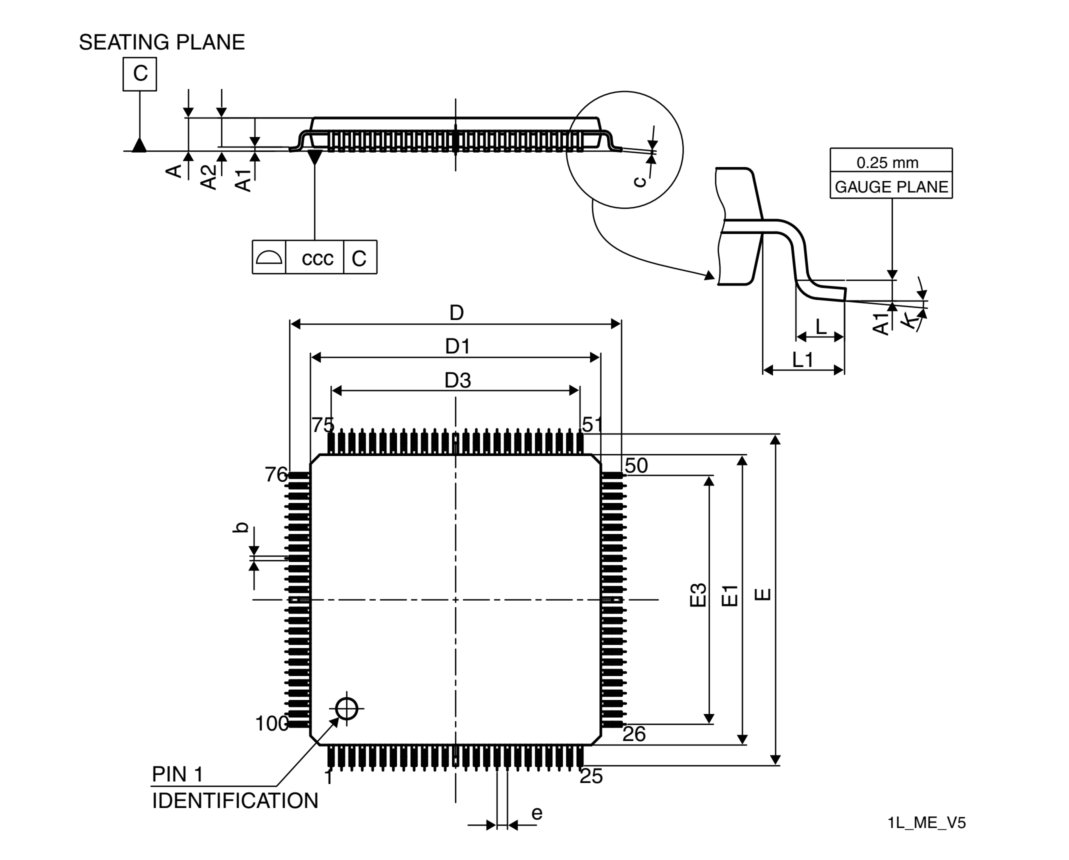
1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

6.3 LQFP100 package information

Figure 65. LFP100 – 14 x 14 mm 100 pin low-profile quad flat package outline



1. Drawing is not to scale.

Table 70. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-

6.5 Thermal characteristics

The maximum chip junction temperature ($T_J$max) must never exceed the values given in *Table 10: General operating conditions on page 44*.

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

T_J max = T_A max + (P_D max x Θ_{JA})

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$max),
- P_{INT} max is the product of I_{DD} and V_{DD}, expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$P_{I/O}$ max = $\Sigma (V_{OL} \times I_{OL}) + \Sigma((V_{DD} - V_{OH}) \times I_{OH})$,

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 72. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	**Thermal resistance junction-ambient** LFBGA144 - 10 × 10 mm / 0.8 mm pitch	40	°C/W
	Thermal resistance junction-ambient LQFP144 - 20 × 20 mm / 0.5 mm pitch	30	
	Thermal resistance junction-ambient LQFP100 - 14 × 14 mm / 0.5 mm pitch	46	
	Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch	45	

6.5.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

8 Revision history

Table 74. Document revision history

Date	Revision	Changes
27-Oct-2009	1	Initial release.
15-Nov-2010	2	LQFP64 package mechanical data updated: see *Figure 66: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline* and *Table 71: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data*. Internal code removed from *Table 73: STM32F103xF and STM32F103xG ordering information scheme*. Updated note 2 below *Table 54: I²C characteristics* Updated *Figure 46: I²C bus AC waveforms and measurement circuit* Updated *Figure 45: Recommended NRST pin protection* Updated note 1 below *Table 49: I/O static characteristics* Updated *Table 20: Peripheral current consumption* Updated *Table 14: Maximum current consumption in Run mode, code with data processing running from Flash* Updated *Table 15: Maximum current consumption in Run mode, code with data processing running from RAM* Updated *Table 16: Maximum current consumption in Sleep mode, code running from Flash or RAM* Updated *Table 17: Typical and maximum current consumptions in Stop and Standby modes* Updated *Table 18: Typical current consumption in Run mode, code with data processing running from Flash* Updated *Table 19: Typical current consumption in Sleep mode, code running from Flash or RAM* Updated *Table 24: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)* Updated *Figure 22: Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms on page 63* Added *Section 5.3.13: I/O current injection characteristics on page 84*
18-Jan-2012	3	*Section 2.3.26: GPIOs (general-purpose inputs/outputs)*: modified text of last sentence. *Table 5: STM32F103xF and STM32F103xG pin definitions*: updated pins PD0, PD1, OSC_IN, OSC_OUT, PB8, PB9, and PF8. *Table 7: Voltage characteristics*: Removed the previous footnotes 2 and 3 and added current footnote *2*. *Table 8: Current characteristics*: updated footnotes *3*, *4*, and *5*. *Table 21: High-speed external user clock characteristics*: replaced the $t_{w(HSE)}$ min value by 5 (instead of 16). *Table 24: LSE oscillator characteristics (f_{LSE} = 32.768 kHz)*: updated symbols and footnotes.