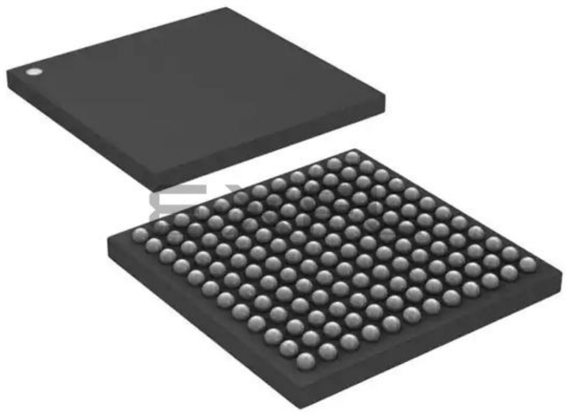

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 72MHz |
| Connectivity | CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB |
| Peripherals | DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT |
| Number of I/O | 112 |
| Program Memory Size | 1MB (1M x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 96K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 3.6V |
| Data Converters | A/D 21x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 144-LFBGA |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zgh6 |

# List of figures

### 2.3.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

### 2.3.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

### 2.3.12 Power supply schemes

- $V_{DD}$ = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through $V_{DD}$ pins.
- $V_{SSA}$, $V_{DDA}$ = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to VDDA is 2.4 V when the ADC or DAC is used). $V_{DDA}$ and $V_{SSA}$ must be connected to $V_{DD}$ and $V_{SS}$, respectively.
- $V_{BAT}$ = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when $V_{DD}$ is not present.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

### 2.3.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when $V_{DD}$ is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the $V_{DD}/V_{DDA}$ power supply and compares it to the $V_{PVD}$ threshold. An interrupt can be generated when $V_{DD}/V_{DDA}$ drops below the $V_{PVD}$ threshold and/or when $V_{DD}/V_{DDA}$ is higher than the $V_{PVD}$ threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and $V_{PVD}$.

The DMA can be used with the main peripherals: SPI, $I^2C$, USART, general-purpose, basic and advanced-control timers TIMx, DAC, $I^2S$, SDIO and ADC.

### 2.3.17 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on $V_{DD}$ supply when present or through the $V_{BAT}$ pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when $V_{DD}$ power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

### 2.3.18 Timers and watchdogs

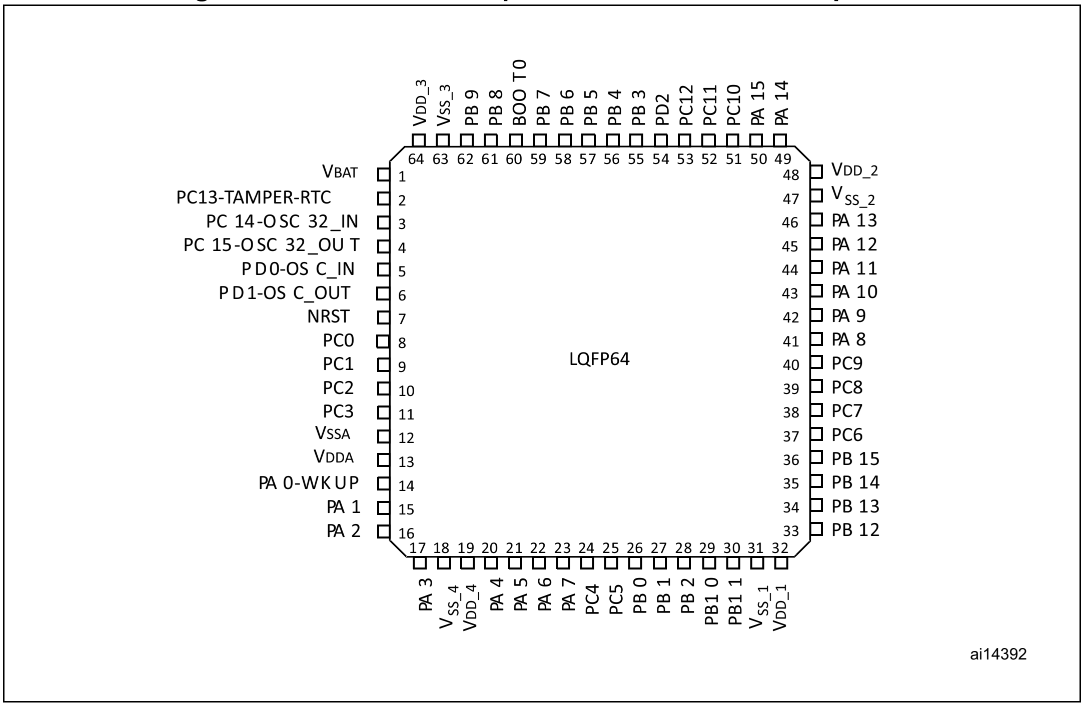
The XL-density STM32F103xF/G performance line devices include up to two advanced-control timers, up to ten general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

*Table 4* compares the features of the advanced-control, general-purpose and basic timers.

**Table 4. STM32F103xF and STM32F103xG timer feature comparison**

| Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|---|---|---|---|---|---|---|
| TIM1, TIM8 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | Yes |
| TIM2, TIM3, TIM4, TIM5 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| TIM9, TIM12 | 16-bit | Up | Any integer between 1 and 65536 | No | 2 | No |
| TIM10, TIM11 TIM13, TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No |
| TIM6, TIM7 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 0 | No |

**Figure 6. STM32F103xF/G performance line LQFP64 pinout**




1. The above figure shows the package top view.

**Table 5. STM32F103xF and STM32F103xG pin definitions (continued)**

| Pins | | | | Pin name | Type[1] | I / O level[2] | Main function[3] (after reset) | Alternate functions[4] | |
|---|---|---|---|---|---|---|---|---|---|
| LFBGA144 | LQFP64 | LQFP100 | LQFP144 | | | | | Default | Remap |
| M12 | 34 | 52 | 74 | PB13 | I/O | FT | PB13 | SPI2_SCK / I2S2_CK / USART3_CTS[7] / TIM1_CH1N | - |
| L11 | 35 | 53 | 75 | PB14 | I/O | FT | PB14 | SPI2_MISO / TIM1_CH2N / USART3_RTS[7]/ TIM12_CH1 | - |
| L12 | 36 | 54 | 76 | PB15 | I/O | FT | PB15 | SPI2_MOSI / I2S2_SD / TIM1_CH3N[7] / TIM12_CH2 | - |
| L9 | - | 55 | 77 | PD8 | I/O | FT | PD8 | FSMC_D13 | USART3_TX |
| K9 | - | 56 | 78 | PD9 | I/O | FT | PD9 | FSMC_D14 | USART3_RX |
| J9 | - | 57 | 79 | PD10 | I/O | FT | PD10 | FSMC_D15 | USART3_CK |
| H9 | - | 58 | 80 | PD11 | I/O | FT | PD11 | FSMC_A16 | USART3_CTS |
| L10 | - | 59 | 81 | PD12 | I/O | FT | PD12 | FSMC_A17 | TIM4_CH1 / USART3_RTS |
| K10 | - | 60 | 82 | PD13 | I/O | FT | PD13 | FSMC_A18 | TIM4_CH2 |
| G8 | - | - | 83 | $V_{SS\_8}$ | S | | $V_{SS\_8}$ | - | - |
| F8 | - | - | 84 | $V_{DD\_8}$ | S | | $V_{DD\_8}$ | - | - |
| K11 | - | 61 | 85 | PD14 | I/O | FT | PD14 | FSMC_D0 | TIM4_CH3 |
| K12 | - | 62 | 86 | PD15 | I/O | FT | PD15 | FSMC_D1 | TIM4_CH4 |
| J12 | - | - | 87 | PG2 | I/O | FT | PG2 | FSMC_A12 | - |
| J11 | - | - | 88 | PG3 | I/O | FT | PG3 | FSMC_A13 | - |
| J10 | - | - | 89 | PG4 | I/O | FT | PG4 | FSMC_A14 | - |
| H12 | - | - | 90 | PG5 | I/O | FT | PG5 | FSMC_A15 | - |
| H11 | - | - | 91 | PG6 | I/O | FT | PG6 | FSMC_INT2 | - |
| H10 | - | - | 92 | PG7 | I/O | FT | PG7 | FSMC_INT3 | - |
| G11 | - | - | 93 | PG8 | I/O | FT | PG8 | - | - |
| G10 | - | - | 94 | $V_{SS\_9}$ | S | | $V_{SS\_9}$ | - | - |
| F10 | - | - | 95 | $V_{DD\_9}$ | S | | $V_{DD\_9}$ | - | - |
| G12 | 37 | 63 | 96 | PC6 | I/O | FT | PC6 | I2S2_MCK / TIM8_CH1 / SDIO_D6 | TIM3_CH1 |
| F12 | 38 | 64 | 97 | PC7 | I/O | FT | PC7 | I2S3_MCK / TIM8_CH2 / SDIO_D7 | TIM3_CH2 |
| F11 | 39 | 65 | 98 | PC8 | I/O | FT | PC8 | TIM8_CH3 / SDIO_D0 | TIM3_CH3 |

Table 20. Peripheral current consumption(1) (continued)

| Peripheral | | Current consumption |
|---|---|---|
| APB2 (up to 72 MHz) | APB2-Bridge | 2,78 |
| | GPIOA | 7,64 |
| | GPIOB | 7,64 |
| | GPIOC | 7,64 |
| | GPIOD | 8,47 |
| | GPIOE | 8,47 |
| | GPIOF | 8,19 |
| | GPIOG | 8,19 |
| | SPI1 | 5,14 |
| | USART1 | 16,67 |
| | TIM1 | 28,47 |
| | TIM8 | 24,31 |
| | TIM9 | 11,81 |
| | TIM10 | 8,47 |
| | TIM11 | 8,47 |
| | ADC1(5)(6) | 17,68 |
| | ADC2(5)(6) | 15,54 |
| | ADC3(5)(6) | 16,43 |

1. $f_{HCLK}$ = 72 MHz, $f_{APB1} = f_{HCLK}/2$, $f_{APB2} = f_{HCLK}$, default prescaler value for each peripheral.
2. The BusMatrix is automatically active when at least one master peripheral is ON.
3. When the I2S is enabled, a current consumption equal to 0.02 mA must be added.
4. When DAC_OU1 or DAC_OUT2 is enabled, a current consumption equal to 0.36 mA must be added.
5. Specific conditions for ADC: $f_{HCLK}$ = 56 MHz, $f_{APB1} = f_{HCLK/2}$, $f_{APB2} = f_{HCLK}$, $f_{ADCCLK} = f_{APB2}/4$/ When ADON bit in the ADC_CR2 register is set to 1, a current consumption equal to 0.59 mA must be added.
6. When the ADC is enabled, a current consumption equal to 0.1 mA must be added.

## 5.3.6 External clock source characteristics

### High-speed external user clock generated from an external source

The characteristics given in *Table 21* result from tests performed using an high-speed external clock source, and under ambient temperature and supply voltage conditions summarized in *Table 10*.

**Figure 27. Synchronous multiplexed PSRAM write timings**

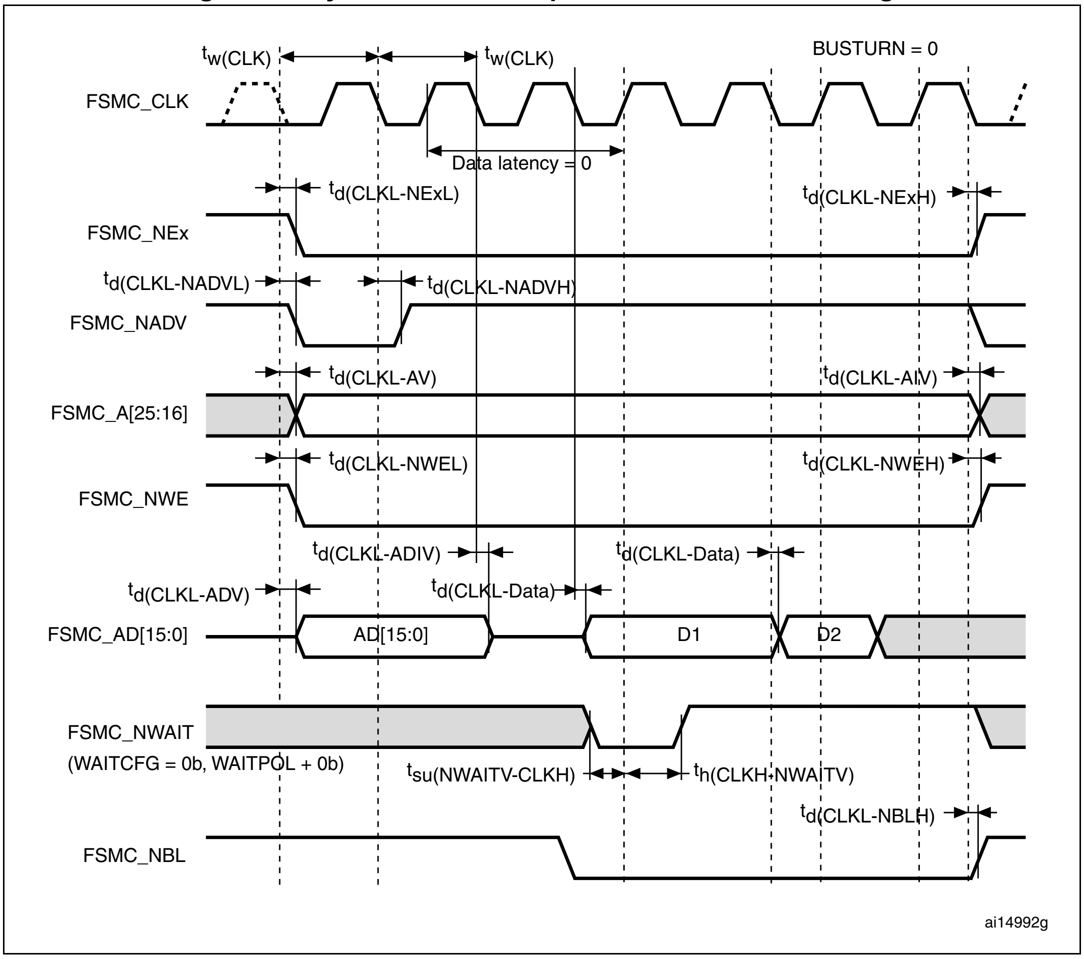
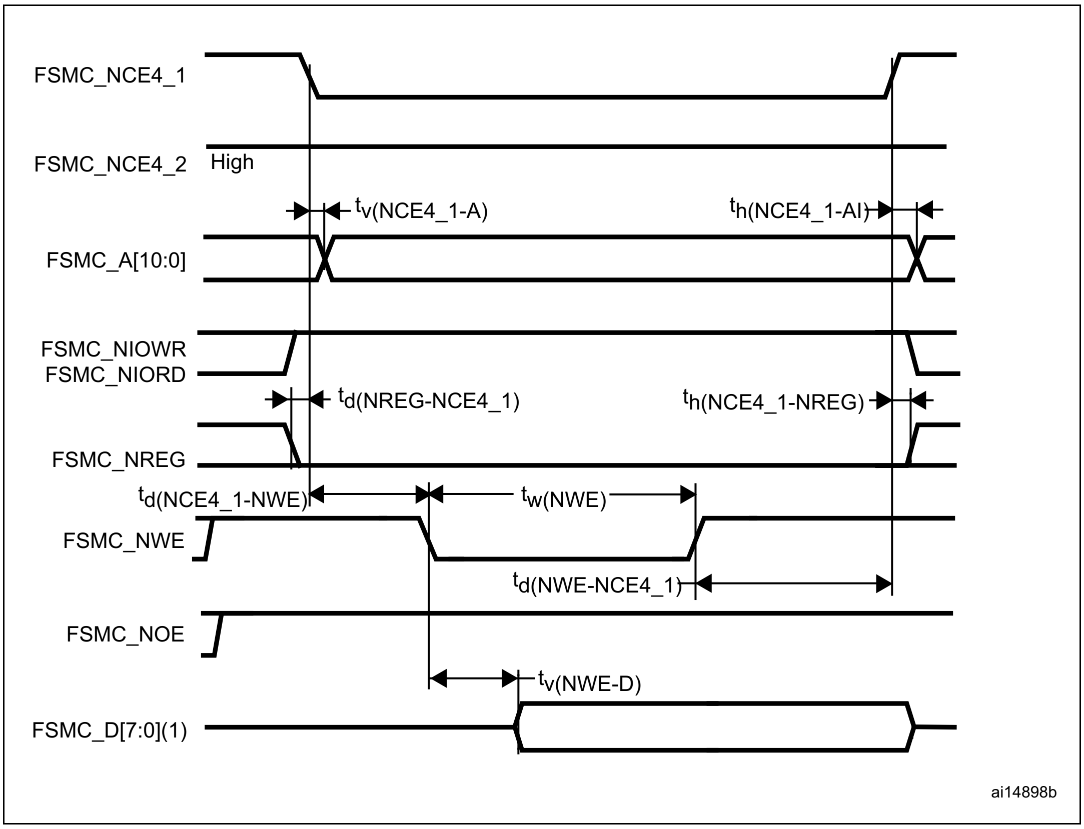


**Figure 33. PC Card/CompactFlash controller waveforms for attribute memory write access**




1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

**Figure 34. PC Card/CompactFlash controller waveforms for I/O space read access**

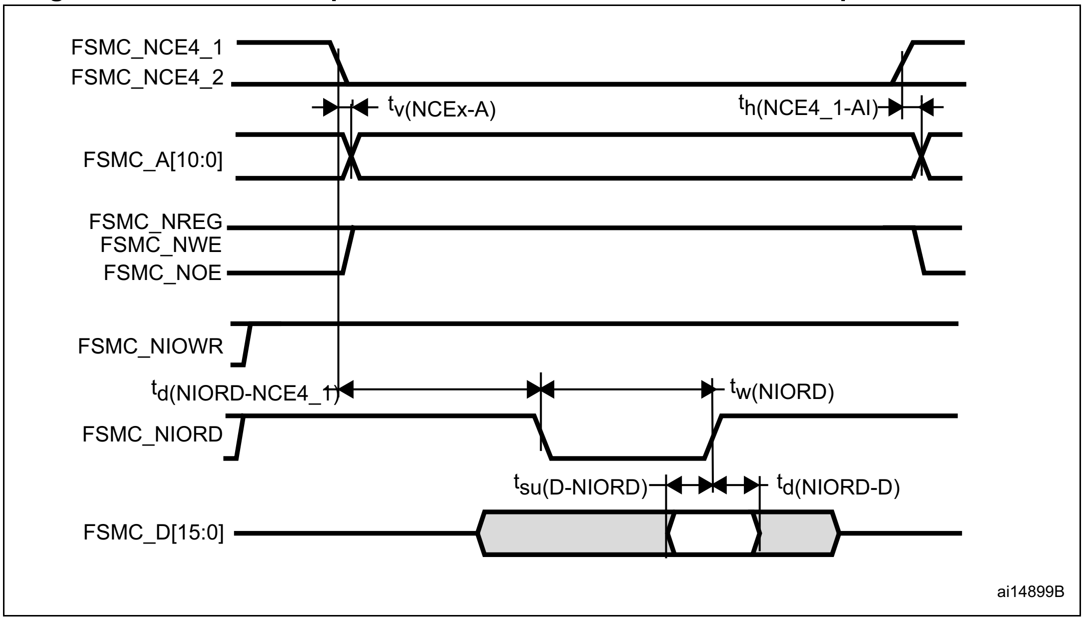


**Figure 38. NAND controller waveforms for common memory read access**

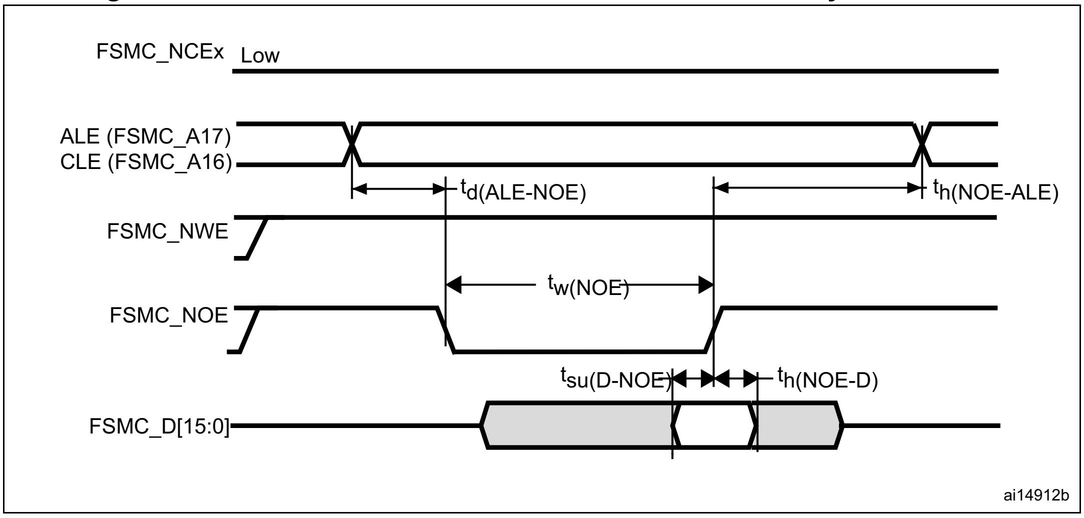



**Figure 39. NAND controller waveforms for common memory write access**

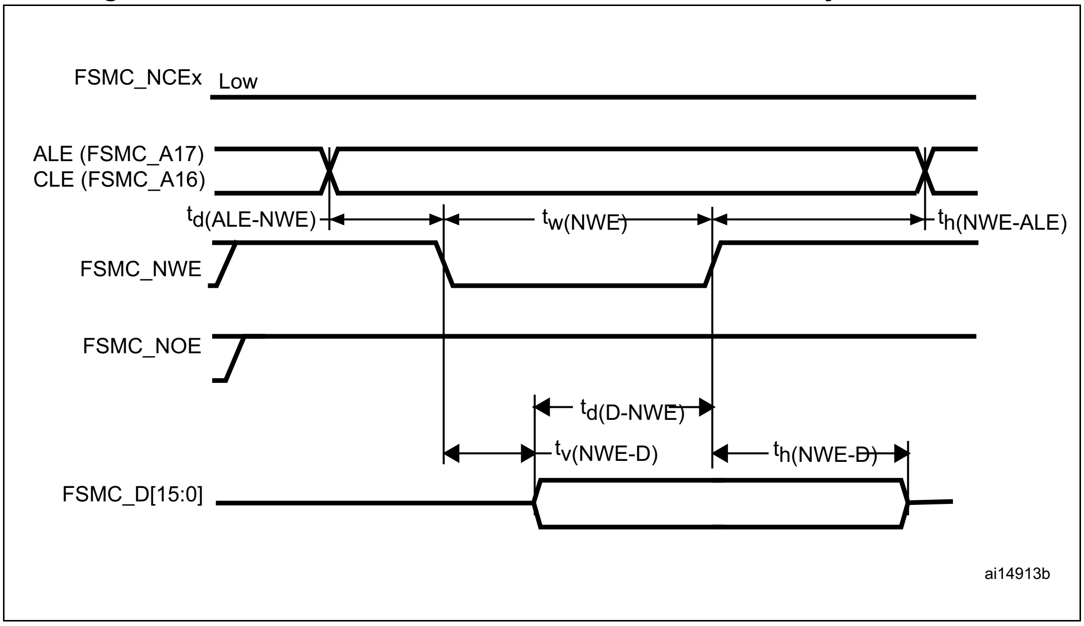



**Table 42. Switching characteristics for NAND Flash read cycles(1)**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{w(NOE)}$ | FSMC_NOE low width | $3t_{HCLK} – 1$ | $3t_{HCLK} + 1$ | ns |
| $t_{su(D-NOE)}$ | FSMC_D[15:0] valid data before FSMC_NOE high | 13 | - | ns |
| $t_{h(NOE-D)}$ | FSMC_D[15:0] valid data after FSMC_NOE high | 0 | - | ns |
| $t_{d(ALE-NOE)}$ | FSMC_ALE valid before FSMC_NOE low | - | $2t_{HCLK}$ | ns |
| $t_{h(NOE-ALE)}$ | FSMC_NWE high to FSMC_ALE invalid | $2t_{HCLK}$ | - | ns |

1. $C_L$ = 15 pF.

Table 47. Electrical sensitivities

| Symbol | Parameter | Conditions | Class |
|---|---|---|---|
| LU | Static latch-up class | $T_A$ = +105 °C conforming to JESD78A | II level A |

### 5.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below $V_{SS}$ or above $V_{DD}$ (for standard, 3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

#### Functional susceptibilty to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (>5 LSB TUE), out of spec current injection on adjacent pins or other functional failure (for example reset, oscillator frequency deviation).

The test results are given in *Table 48*

Table 48. I/O current injection susceptibility

| Symbol | Description | Functional susceptibility | | Unit |
|---|---|---|---|---|
| | | Negative injection | Positive injection | |
| $I_{INJ}$ | Injected current on OSC_IN32, OSC_OUT32, PA4, PA5, PC13 | -0 | +0 | mA |
| | Injected current on all FT pins | -5 | +0 | |
| | Injected current on any other pin | -5 | +5 | |

**Figure 40. Standard I/O input characteristics - CMOS port**

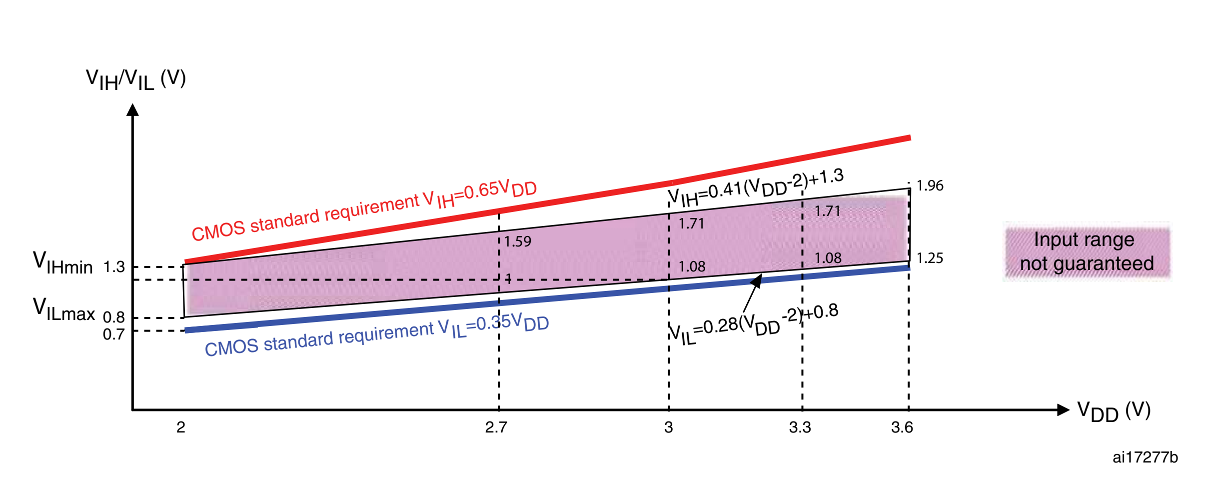



**Figure 41. Standard I/O input characteristics - TTL port**

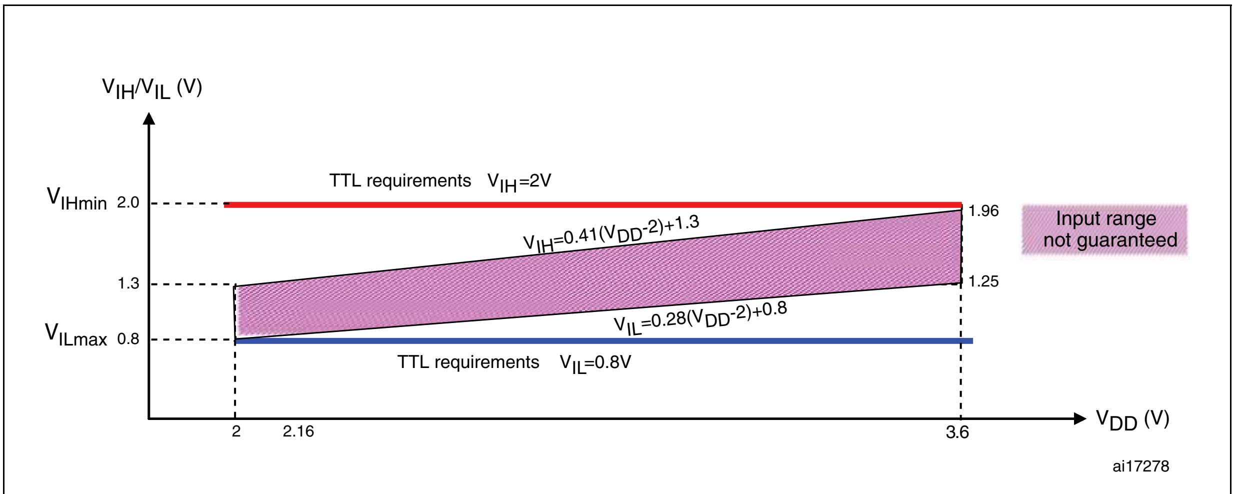
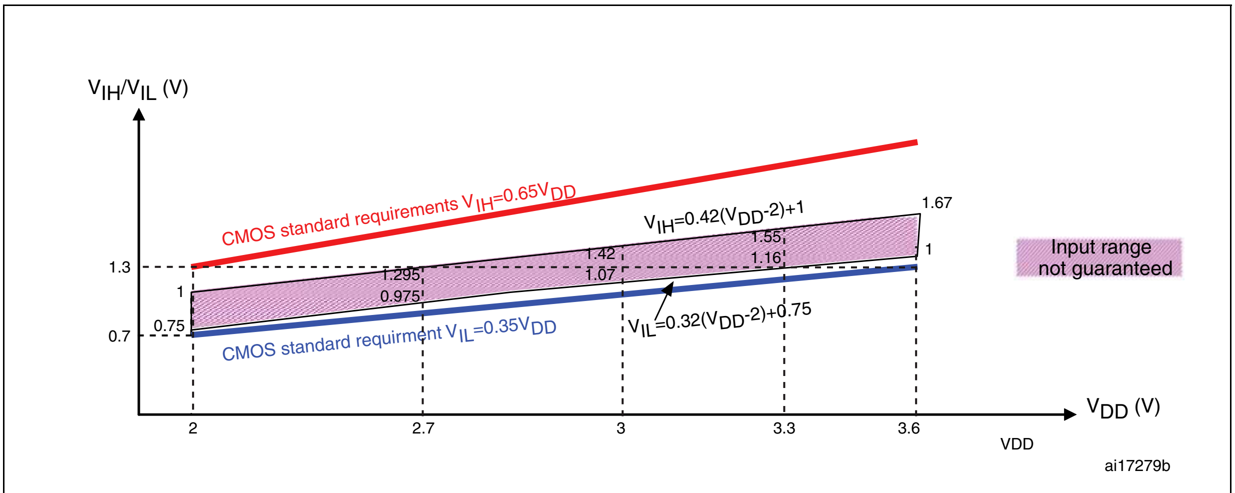



**Figure 42. 5 V tolerant I/O input characteristics - CMOS port**



### $I^2S$ - SPI characteristics

Unless otherwise specified, the parameters given in *Table 56* for SPI or in *Table 57* for $I^2S$ are derived from tests performed under ambient temperature, $f_{PCLKx}$ frequency and $V_{DD}$ supply voltage conditions summarized in *Table 10*.

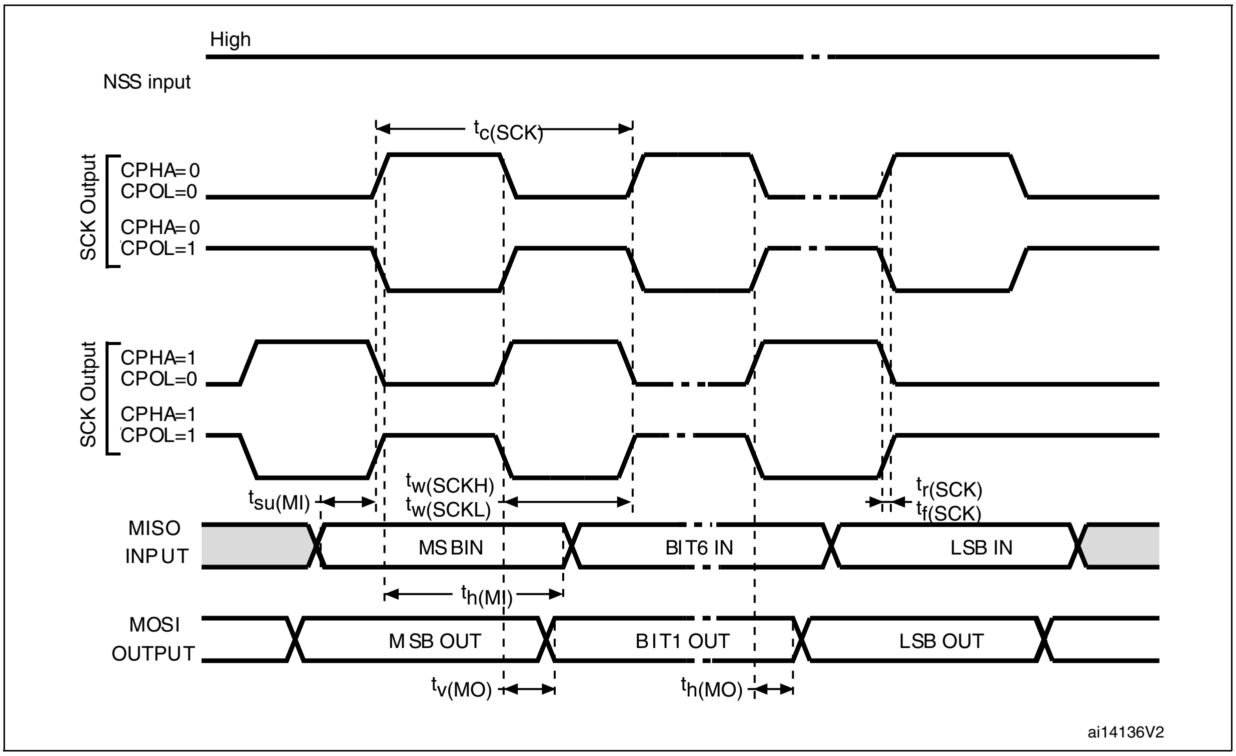
Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for $I^2S$).

**Table 56. SPI characteristics**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $f_{SCK}$ $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 18 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 30 pF | - | 8 | ns |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 30 | 70 | % |
| $t_{su(NSS)}$(1) | NSS setup time | Slave mode | $4t_{PCLK}$ | - | ns |
| $t_{h(NSS)}$(1) | NSS hold time | Slave mode | $2t_{PCLK}$ | - | |
| $t_{w(SCKH)}$(1) $t_{w(SCKL)}$(1) | SCK high and low time | Master mode, $f_{PCLK}$ = 36 MHz, presc = 4 | 50 | 60 | |
| $t_{su(MI)}$(1) $t_{su(SI)}$(1) | Data input setup time | Master mode | 5 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}$(1) | Data input hold time | Master mode | 5 | - | |
| $t_{h(SI)}$(1) | | Slave mode | 4 | - | |
| $t_{a(SO)}$(1)(2) | Data output access time | Slave mode, $f_{PCLK}$ = 20 MHz | 0 | $3t_{PCLK}$ | |
| $t_{dis(SO)}$(1)(3) | Data output disable time | Slave mode | 2 | 10 | |
| $t_{v(SO)}$(1) | Data output valid time | Slave mode (after enable edge) | - | 25 | |
| $t_{v(MO)}$(1) | Data output valid time | Master mode (after enable edge) | - | 5 | |
| $t_{h(SO)}$(1) | Data output hold time | Slave mode (after enable edge) | 15 | - | |
| $t_{h(MO)}$(1) | | Master mode (after enable edge) | 2 | - | |

1. Guaranteed by characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

**Figure 49. SPI timing diagram - master mode[1]**




1. Measurement points are done at CMOS levels: $0.3V_{DD}$ and $0.7V_{DD}$.

2. Guaranteed by design, not tested in production.
3. $V_{REF+}$ can be internally connected to $V_{DDA}$ and $V_{REF-}$ can be internally connected to $V_{SSA}$, depending on the package. Refer to *Section 3: Pinouts and pin descriptions* for further details.
4. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 62*.

### Equation 1: $R_{AIN}$ max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

**Table 63. $R_{AIN}$ max for $f_{ADC}$ = 14 MHz(1)**

| $T_s$ (cycles) | $t_S$ (µs) | $R_{AIN}$ max (kΩ) |
|---|---|---|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | NA |
| 239.5 | 17.1 | NA |

1. Guaranteed by design, not tested in production.

**Table 64. ADC accuracy - limited test conditions(1)(2)**

| Symbol | Parameter | Test conditions | Typ | Max(3) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 56 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 3 V to 3.6 V $T_A$ = 25 °C Measurements made after ADC calibration $V_{REF+} = V_{DDA}$ | ±1.3 | ±2 | LSB |
| EO | Offset error | | ±1 | ±1.5 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±0.7 | ±1 | |
| EL | Integral linearity error | | ±0.8 | ±1.5 | |

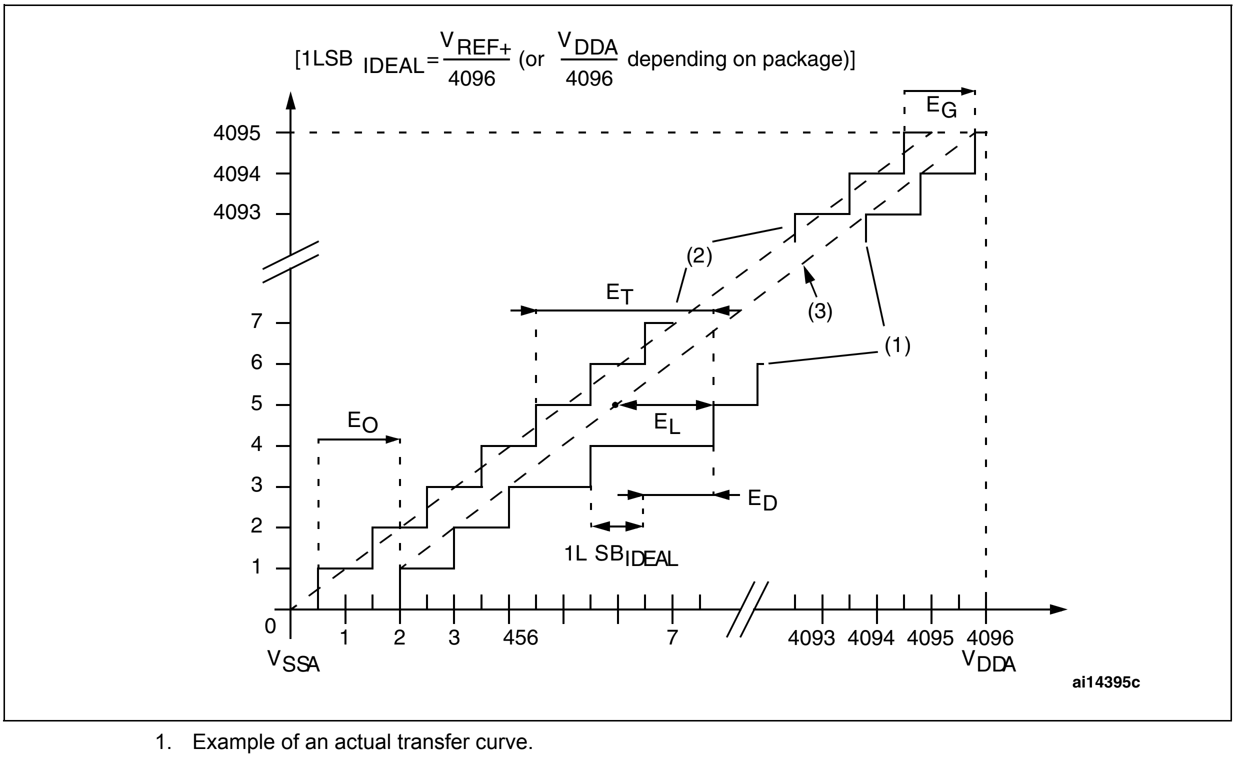
1. ADC DC accuracy values are measured after internal calibration.
2. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.14* does not affect the ADC accuracy.
3. Guaranteed by characterization results, not tested in production.

**Table 65. ADC accuracy(1) (2)(3)**

| Symbol | Parameter | Test conditions | Typ | Max(4) | Unit |
|---|---|---|---|---|---|
| ET | Total unadjusted error | $f_{PCLK2}$ = 56 MHz, $f_{ADC}$ = 14 MHz, $R_{AIN}$ < 10 kΩ, $V_{DDA}$ = 2.4 V to 3.6 V Measurements made after ADC calibration | ±2 | ±5 | LSB |
| EO | Offset error | | ±1.5 | ±2.5 | |
| EG | Gain error | | ±1.5 | ±3 | |
| ED | Differential linearity error | | ±1 | ±2 | |
| EL | Integral linearity error | | ±1.5 | ±3 | |

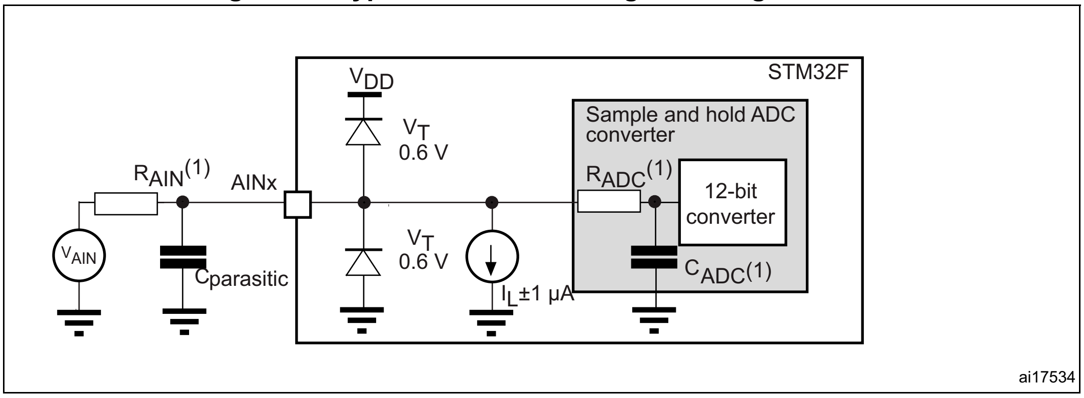
1. ADC DC accuracy values are measured after internal calibration.
2. Better performance could be achieved in restricted $V_{DD}$, frequency, $V_{REF}$ and temperature ranges.
3. ADC Accuracy vs. Negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
Any positive injection current within the limits specified for $I_{INJ(PIN)}$ and $\Sigma I_{INJ(PIN)}$ in *Section 5.3.14* does not affect the ADC accuracy.
4. Preliminary values.

**Figure 55. ADC accuracy characteristics**




1. Example of an actual transfer curve.
2. Ideal transfer curve.
3. End point correlation line.
4. ET = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
EO = Offset Error: deviation between the first actual transition and the first ideal one.
EG = Gain Error: deviation between the last ideal transition and the last actual one.
ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

**Figure 56. Typical connection diagram using the ADC**

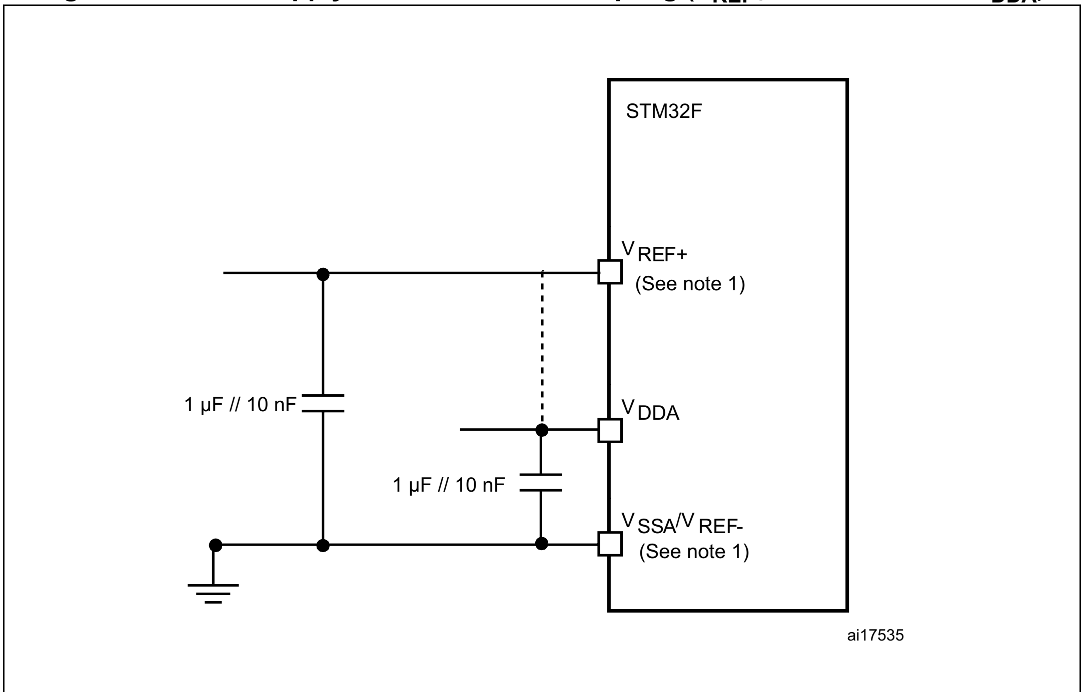



1. Refer to *Table 62* for the values of $R_{AIN}$, $R_{ADC}$ and $C_{ADC}$.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, $f_{ADC}$ should be reduced.

## General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 57* or *Figure 58*, depending on whether $V_{REF+}$ is connected to $V_{DDA}$ or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

**Figure 57. Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$)**



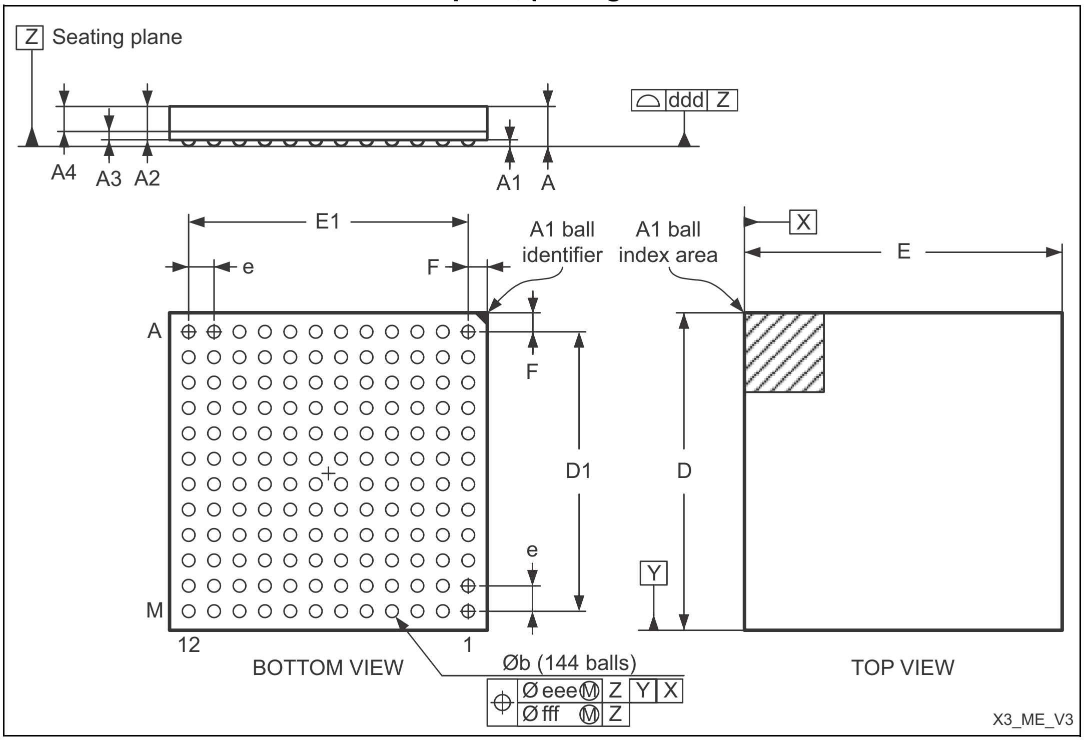

1. $V_{REF+}$ and $V_{REF-}$ inputs are available only on 100-pin packages.

# 6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

## 6.1 LFBGA144 package information

**Figure 60. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package outline**

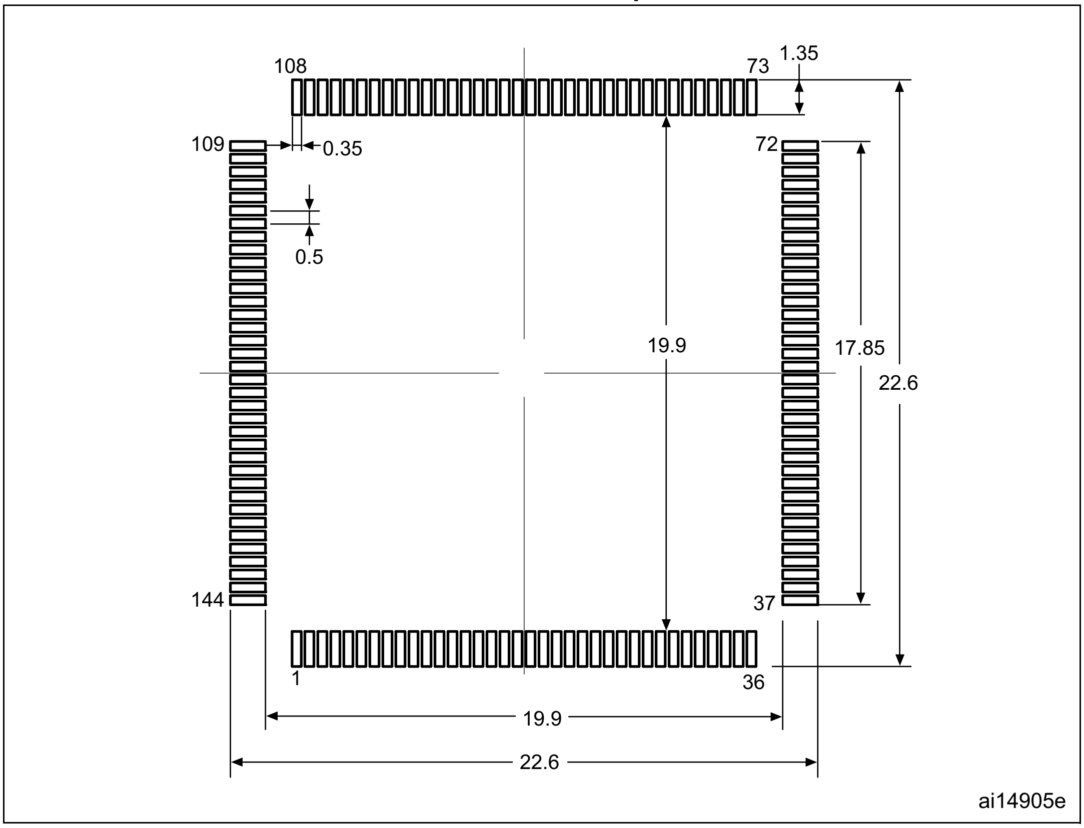



1. Drawing is not to scale.

**Table 68. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data**

| Symbol | millimeters | | | inches(1) | | |
|---|---|---|---|---|---|---|
| | Min | Typ | Max | Typ | Min | Max |
| A(2) | - | - | 1.700 | | | 0.0669 |
| A1 | 0.210 | - | - | 0.0083 | | |
| A2 | - | 1.060 | - | | 0.0417 | |
| A3 | | 0.026 | | | 0.0010 | |
| A4 | - | 0.800 | - | - | 0.0315 | - |
| b | 0.350 | 0.400 | 0.450 | 0.0138 | 0.0157 | 0.0177 |
| D | 9.850 | 10.000 | 10.150 | 0.3878 | 0.3937 | 0.3996 |
| D1 | - | 8.800 | - | - | 0.3465 | - |
| E | 9.850 | 10.000 | 10.150 | 0.3878 | 0.3937 | 0.3996 |
| E1 | - | 8.800 | - | - | 0.3465 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| F | - | 0.600 | - | - | 0.0236 | - |
| ddd | - | - | 0.100 | - | - | 0.0039 |

**Figure 63. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint**




1. Dimensions are expressed in millimeters.

Table 74. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 15-May-2015 | 4 | Added document status on first page.<br>Replace DAC1_OUT/DAC2_OUT by DAC_OUT1/DAC_OUT2, and updated TIM5 in *Figure 1: STM32F103xF and STM32F103xG performance line block diagram on page 12*.<br>Replaced USBDP/USBDM by USB_DP/USB_DM in the whole document.<br>Updated notes related to electrical values guaranteed by characterization results.<br>Updated *Table 20: Peripheral current consumption*.<br>Updated *Table 36: Synchronous multiplexed NOR/PSRAM read timings* to *Table 39: Synchronous non-multiplexed PSRAM write timings*(added FSMC_NWAIT timings). Updated *Figure 26: Synchronous multiplexed NOR/PSRAM read timings on page 73* and *Figure 28: Synchronous non-multiplexed NOR/PSRAM read timings on page 77* and *Figure 35: PC Card/CompactFlash controller waveforms for I/O space write access on page 83*.<br>Updated CDM class in *Table 46: ESD absolute maximum ratings*.<br>Updated *Figure 44: I/O AC characteristics definition on page 96* and *Figure 45: Recommended NRST pin protection on page 97*.<br>Updated *Figure 49: SPI timing diagram - master mode(1) on page 96*.<br>Modified note 3 in *Table 56: SPI characteristics*.<br>*Section : I2C interface characteristics*: Updated introduction, updated *Table 54: $I^2C$ characteristics* and *Figure 46: $I^2C$ bus AC waveforms and measurement circuit on page 99*.<br>Modified note 2 in *Table 64: ADC accuracy - limited test conditions*, *Figure 55: ADC accuracy characteristics on page 110* and *Figure 56: Typical connection diagram using the ADC on page 111*. Updated *Figure 57: Power supply and reference decoupling ($V_{REF+}$ not connected to $V_{DDA}$) on page 111* and *Figure 58: Power supply and reference decoupling ($V_{REF+}$ connected to $V_{DDA}$) on page 112*.<br>Updated $I_{DDA}$ description and Offset comment in *Table 66: DAC characteristics*.<br>Updated *Section 6.1: LFBGA144 package information* and added *Section : Device marking for LFBGA144 package*.<br>Updated *Section 6.2: LQFP144 package information* and added *Section : Device marking for LQFP144 package*.<br>Updated *Section 6.3: LQFP100 package information* and added *Section : Device marking for LQFP100 package*.<br>Updated *Section 6.4: LQFP64 package information* and added *Section : Device marking for LQFP64 package*. |