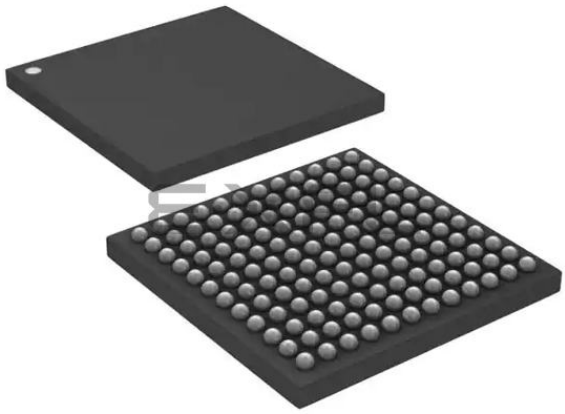

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zgh6j

List of tables

2.3.5 Embedded SRAM

96 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

2.3.6 FSMC (flexible static memory controller)

The FSMC is embedded in the STM32F103xF and STM32F103xG performance line family. It has four Chip Select outputs supporting the following modes: PC Card/Compact Flash, SRAM, PSRAM, NOR and NAND.

Functionality overview:

- The three FSMC interrupt lines are ORed in order to be connected to the NVIC
- Write FIFO
- Code execution from external memory except for NAND Flash and PC Card
- The targeted frequency, f_{CLK}, is HCLK/2, so external access is at 36 MHz when HCLK is at 72 MHz and external access is at 24 MHz when HCLK is at 48 MHz

2.3.7 LCD parallel interface

The FSMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high-performance solutions using external controllers with dedicated acceleration.

2.3.8 Nested vectored interrupt controller (NVIC)

The STM32F103xF and STM32F103xG performance line embeds a nested vectored interrupt controller able to handle up to 60 maskable interrupt channels (not including the 16 interrupt lines of Cortex®-M3) and 16 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of *late arriving* higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.9 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 19 edge detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 112 GPIOs can be connected to the 16 external interrupt lines.

Table 6. FSMC pin definition (continued)

Pins	FSMC					LQFP100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11	-	-	A16	A16	CLE	Yes
PD12	-	-	A17	A17	ALE	Yes
PD13	-	-	A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2	-	-	A12	-	-	-
PG3	-	-	A13	-	-	-
PG4	-	-	A14	-	-	-
PG5	-	-	A15	-	-	-
PG6	-	-	-	-	INT2	-
PG7	-	-	-	-	INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3	-	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	-	NE1	NE1	NCE2	Yes
PG9	-	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	NCE4_2	-	-	-	-
PG12	-	-	NE4	NE4	-	-
PG13	-	-	A24	A24	-	-
PG14	-	-	A25	A25	-	-
PB7	-	-	NADV	NADV	-	Yes
PE0	-	-	NBL0	NBL0	-	Yes
PE1	-	-	NBL1	NBL1	-	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V £ V_{DD} £ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

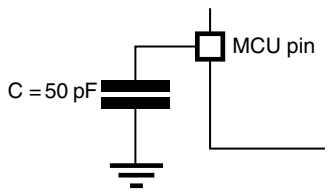


Figure 9. Pin input voltage

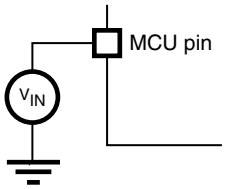
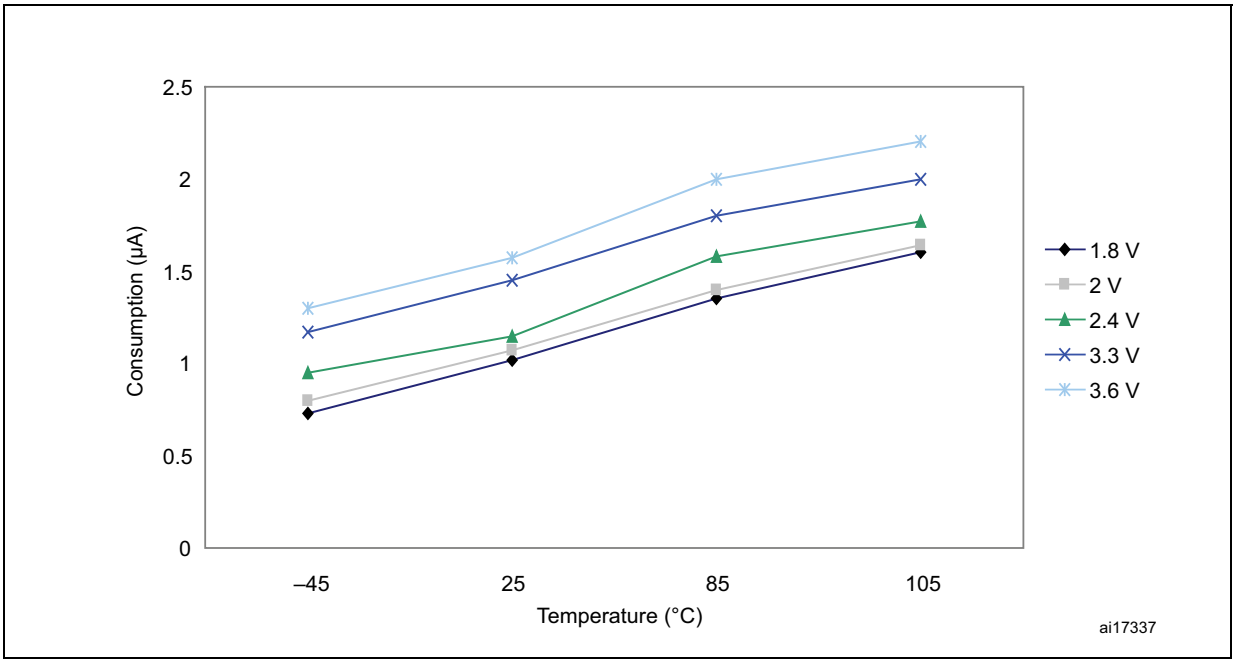


Table 17. Typical and maximum current consumptions in Stop and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max		Unit
			V_{DD}/V_{BAT} = 2.0 V	V_{DD}/V_{BAT} = 2.4 V	V_{DD}/V_{BAT} = 3.3 V	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Stop mode	Regulator in run mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog), f_{CK}=8 MHz	44.8	45.3	46.4	810	1680	µA
		Regulator in low-power mode, low-speed and high-speed internal RC oscillators and high-speed oscillator OFF (no independent watchdog)	37.4	37.8	38.7	790	1660	
	Supply current in Standby mode	Low-speed internal RC oscillator and independent watchdog OFF, low-speed oscillator and RTC OFF	1.8	2.0	2.5	5(2)	8(2)	
I_{DD_VBAT}	Backup domain supply current	Low-speed oscillator and RTC ON	1.05	1.1	1.4	2(2)	2.3(2)	

1. Typical values are measured at T_A = 25 °C.
2. Guaranteed by characterization results, not tested in production..

Figure 14. Typical current consumption on V_{BAT} with RTC on vs. temperature at different V_{BAT} values



Typical current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash access time is adjusted to f_{HCLK} frequency (0 wait state from 0 to 24 MHz, 1 wait state from 24 to 48 MHZ and 2 wait states above).
- Ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.
- Prefetch is ON (Reminder: this bit must be set before clock setting and bus prescaling)

When the peripherals are enabled $f_{PCLK1} = f_{HCLK}/4$, $f_{PCLK}2 = f_{HCLK}/2$, $f_{ADCCLK} = f_{PCLK2}/4$

Table 18. Typical current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Run mode	External clock(3)	72 MHz	52.5	33.5	mA
			48 MHz	36.6	23.8	
			36 MHz	28.5	18.7	
			24 MHz	24.1	12.8	
			16 MHz	14	9.2	
			8 MHz	7.7	5.4	
			4 MHz	4.6	3.4	
			2 MHz	3	2.3	
			1 MHz	2.2	1.8	
			500 kHz	1.7	1.5	
			125 kHz	1.4	1.3	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	45.5	28.6	mA
			48 MHz	35.1	22.4	
			36 MHz	27.5	17.5	
			24 MHz	18.9	11.6	
			16 MHz	12.2	8.2	
			8 MHz	7.2	4.8	
			4 MHz	4	2.7	
			2 MHz	2.3	1.7	
			1 MHz	1.5	1.2	
			500 kHz	1.1	0.9	
			125 kHz	0.75	0.7	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 19. Typical current consumption in Sleep mode, code running from Flash or RAM

Symbol	Parameter	Conditions	f_{HCLK}	Typ(1)		Unit
				All peripherals enabled(2)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	External clock(3)	72 MHz	32.5	7	mA
			48 MHz	23	5	
			36 MHz	17.7	4	
			24 MHz	12.2	3.1	
			16 MHz	8.4	2.3	
			8 MHz	4.6	1.5	
			4 MHz	3	1.3	
			2 MHz	2.15	1.25	
			1 MHz	1.7	1.2	
			500 kHz	1.5	1.15	
			125 kHz	1.35	1.15	
		Running on high speed internal RC (HSI), AHB prescaler used to reduce the frequency	64 MHz	28.7	5.7	
			48 MHz	22	4.4	
			36 MHz	17	3.35	
			24 MHz	11.6	2.3	
			16 MHz	7.7	1.6	
			8 MHz	3.9	0.8	
			4 MHz	2.3	0.7	
			2 MHz	1.5	0.6	
			1 MHz	1.1	0.5	
			500 kHz	0.9	0.5	
			125 kHz	0.7	0.5	

1. Typical values are measures at T_A = 25 °C, V_{DD} = 3.3 V.
2. Add an additional power consumption of 0.8 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is on (ADON bit is set in the ADC_CR2 register).
3. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

5.3.10 FSMC characteristics

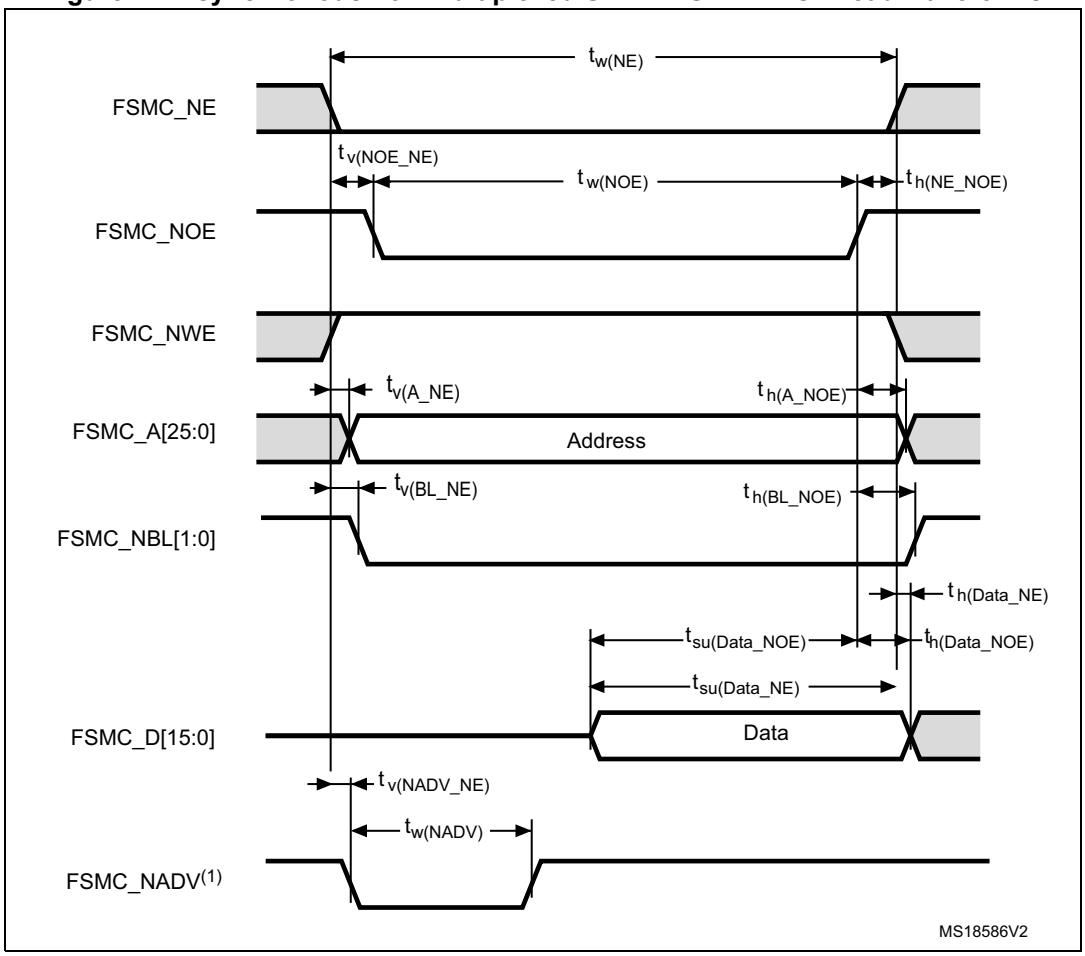
Asynchronous waveforms and timings

Figure 22 through *Figure 25* represent asynchronous waveforms and *Table 31* through *Table 35* provide the corresponding timings. The results shown in these tables are obtained with the following FSMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Note: On all tables, the t_{HCLK} is the HCLK clock period.

Figure 22. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms



1. Mode 2/B, C and D only. In Mode 1, FSMC_NADV is not used.

Note: FSMC_BusTurnAroundDuration = 0.

Figure 27. Synchronous multiplexed PSRAM write timings

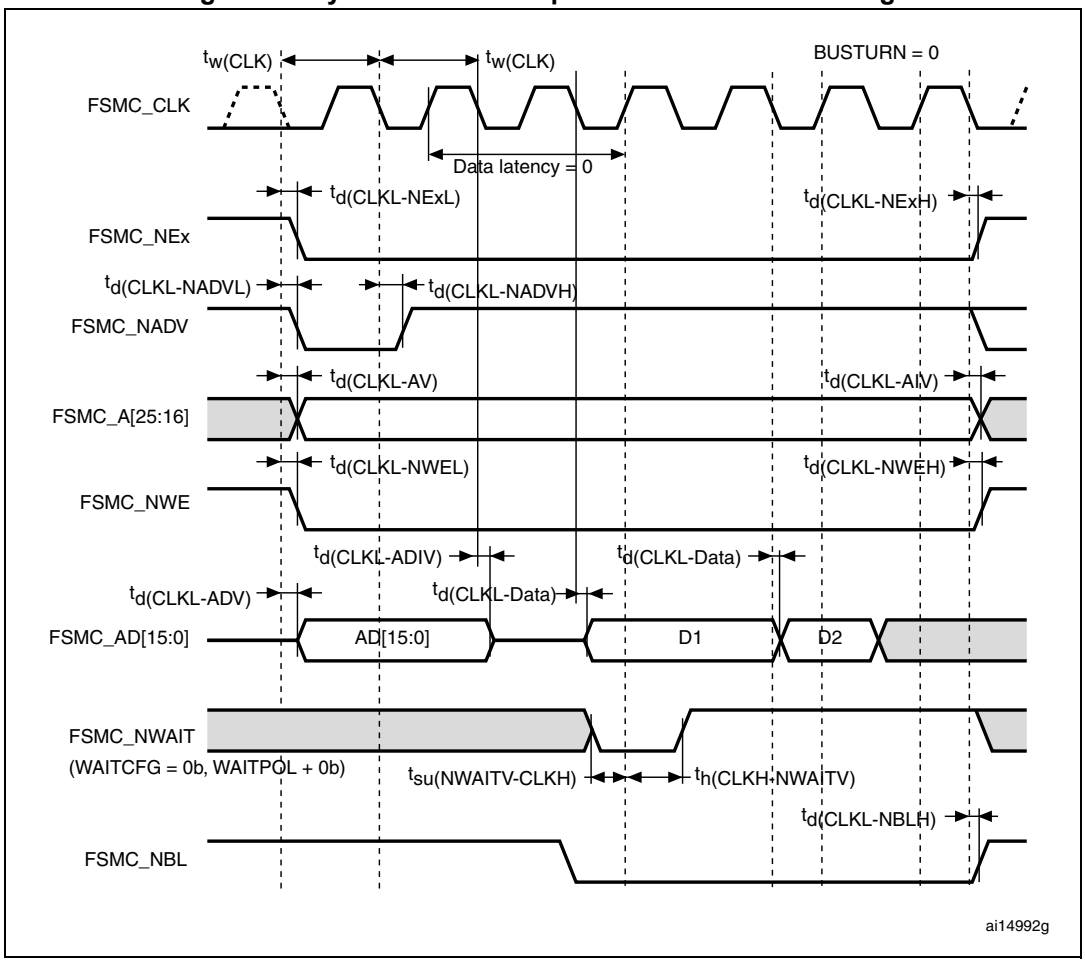


Figure 28. Synchronous non-multiplexed NOR/PSRAM read timings

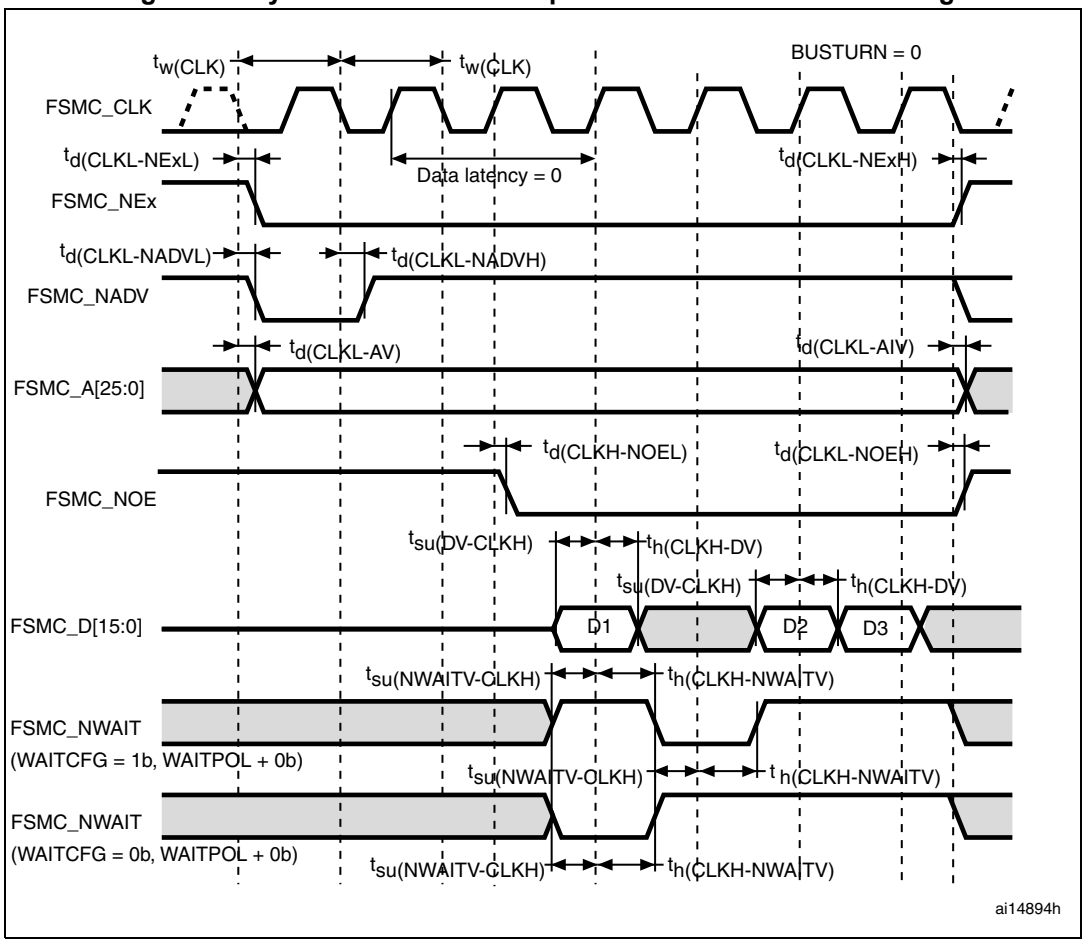


Table 38. Synchronous non-multiplexed NOR/PSRAM read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	FSMC_CLK period	27.6	-	ns
$t_{d(CLKL-NExL)}$	FSMC_CLK low to FSMC_NEx low (x = 0...2)	-	1.5	ns
$t_{d(CLKL-NExH)}$	FSMC_CLK low to FSMC_NEx high (x = 0...2)	2	-	ns
$t_{d(CLKL-NADVL)}$	FSMC_CLK low to FSMC_NADV low	-	0.5	ns
$t_{d(CLKL-NADVH)}$	FSMC_CLK low to FSMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	FSMC_CLK low to FSMC_Ax valid (x = 0...25)	-	0	ns
$t_{d(CLKL-AIV)}$	FSMC_CLK low to FSMC_Ax invalid (x = 0...25)	2	-	ns
$t_{d(CLKL-NOEL)}$	FSMC_CLK low to FSMC_NOE low	-	t_{HCLK} + 1	ns
$t_{d(CLKL-NOEH)}$	FSMC_CLK low to FSMC_NOE high	1.5	-	ns
$t_{su(DV-CLKH)}$	FSMC_D[15:0] valid data before FSMC_CLK high	3.5	-	ns
$t_{h(CLKH-DV)}$	FSMC_D[15:0] valid data after FSMC_CLK high	0	-	ns
$t_{su(NWAITV-CLKH)}$	FSMC_NWAIT valid before FSMC_SMCLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	FSMC_NWAIT valid after FSMC_CLK high	2	-	ns

Table 41. Switching characteristics for PC Card/CF read and write cycles in I/O space

Symbol	Parameter	Min	Max	Unit
$tw_{(NIOWR)}$	FSMC_NIOWR low width	8 THCLK	-	ns
$tv_{(NIOWR-D)}$	FSMC_NIOWR low to FSMC_D[15:0] valid	-	5 THCLK - 4	ns
$th_{(NIOWR-D)}$	FSMC_NIOWR high to FSMC_D[15:0] invalid	11THCLK - 7	-	ns
$td_{(NCE4\_1-NIOWR)}$	FSMC_NCE4_1 low to FSMC_NIOWR valid	-	5THCLK + 1	ns
$th_{(NCEx-NIOWR)}$	FSMC_NCEx high to FSMC_NIOWR invalid	5THCLK - 2.5	-	ns
$td_{(NIORD-NCEx)}$	FSMC_NCEx low to FSMC_NIORD valid	-	5THCLK - 0.5	ns
$th_{(NCEx-NIORD)}$	FSMC_NCEx high to FSMC_NIORD) valid	5 THCLK - 0.5	-	ns
$tw_{(NIORD)}$	FSMC_NIORD low width	8THCLK	-	ns
$tsu_{(D-NIORD)}$	FSMC_D[15:0] valid before FSMC_NIORD high	28	-	ns
$td_{(NIORD-D)}$	FSMC_D[15:0] valid after FSMC_NIORD high	3	-	ns

NAND controller waveforms and timings

Figure 36 through *Figure 39* represent synchronous waveforms and *Table 43* provides the corresponding timings. The results shown in this table are obtained with the following FSMC configuration:

- COM.FSMC_SetupTime = 0x00;
- COM.FSMC_WaitSetupTime = 0x02;
- COM.FSMC_HoldSetupTime = 0x01;
- COM.FSMC_HiZSetupTime = 0x00;
- ATT.FSMC_SetupTime = 0x00;
- ATT.FSMC_WaitSetupTime = 0x02;
- ATT.FSMC_HoldSetupTime = 0x01;
- ATT.FSMC_HiZSetupTime = 0x00;
- Bank = FSMC_Bank_NAND;
- MemoryDataWidth = FSMC_MemoryDataWidth_16b;
- ECC = FSMC_ECC_Enable;
- ECCPageSize = FSMC_ECCPageSize_512Bytes;
- TCLRSetupTime = 0;
- TARSetupTime = 0;

Figure 36. NAND controller waveforms for read access

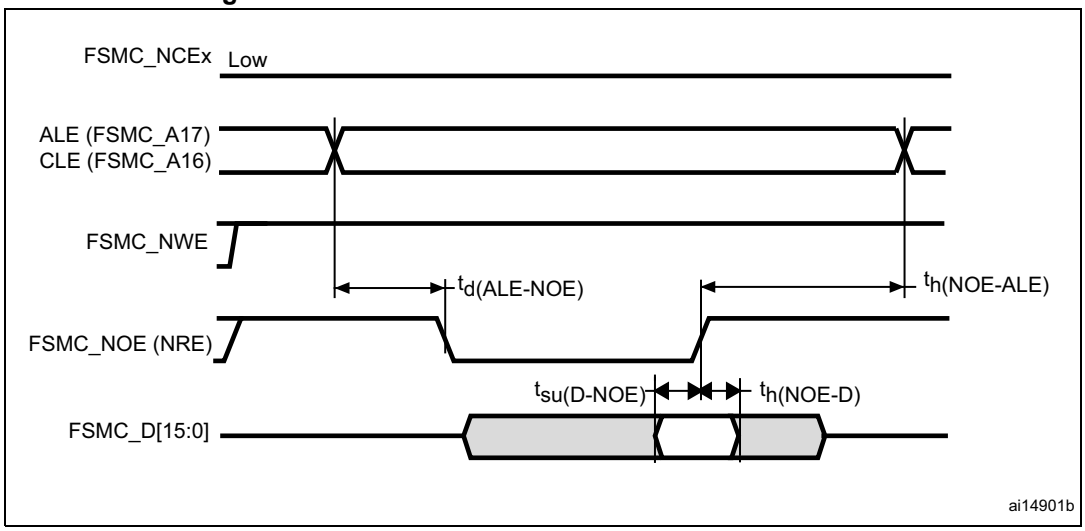
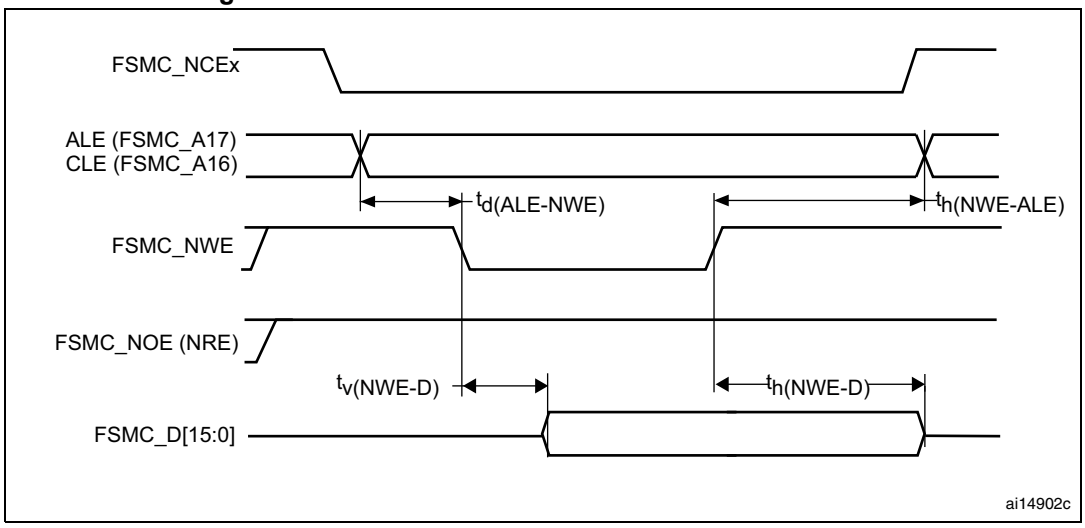


Figure 37. NAND controller waveforms for write access



5.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 49* are derived from tests performed under the conditions summarized in *Table 10*. All I/Os are CMOS and TTL compliant.

Table 49. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Standard IO input low level voltage	-	–0.3	-	0.28*(V_{DD}-2 V)+0.8 V	V
	IO FT(1) input low level voltage		–0.3	-	0.32*(V_{DD}-2 V)+0.75 V	V
V_{IH}	Standard IO input high level voltage	-	0.41*(V_{DD}-2 V)+1.3 V	-	V_{DD}+0.3	V
	IO FT(1) input high level voltage	V_{DD} > 2 V	0.42*(V_{DD}-2 V)+1 V	-	5.5	V
		$V_{DD} \leq$ 2 V			5.2	
V_{hys}	Standard IO Schmitt trigger voltage hysteresis(2)	-	200	-	-	mV
	IO FT Schmitt trigger voltage hysteresis(2)		5% V_{DD}(3)	-	-	mV
I_{lkg}	Input leakage current (4)	$V_{SS} \leq V_{IN} \leq V_{DD}$ Standard I/Os	-	-	±1	µA
		V_{IN}= 5 V, I/O FT	-	-	3	
R_{PU}	Weak pull-up equivalent resistor(5)	$V_{IN} = V_{SS}$	30	40	50	kΩ
R_{PD}	Weak pull-down equivalent resistor(5)	$V_{IN} = V_{DD}$	30	40	50	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. FT = Five-volt tolerant. In order to sustain a voltage higher than V_{DD}+0.3 the internal pull-up/pull-down resistors must be disabled.
2. Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.
3. With a minimum of 100 mV.
4. Leakage could be higher than max. if negative current is injected on adjacent pins.
5. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This MOS/NMOS contribution to the series resistance is minimum (~10% order).

All I/Os are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in *Figure 40* and *Figure 41* for standard I/Os, and in *Figure 42* and *Figure 43* for 5 V tolerant I/Os.

Figure 40. Standard I/O input characteristics - CMOS port

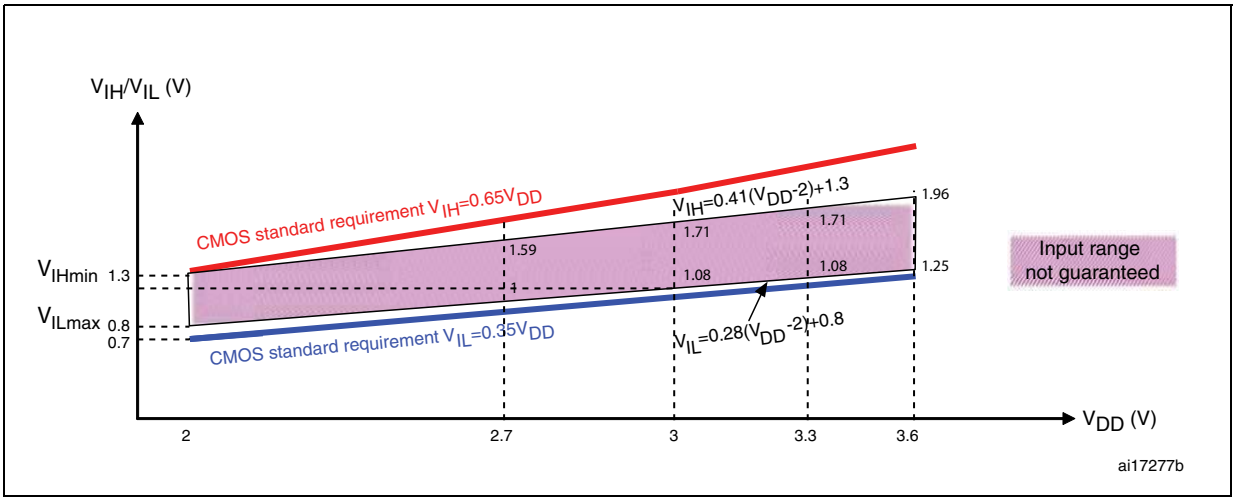


Figure 41. Standard I/O input characteristics - TTL port

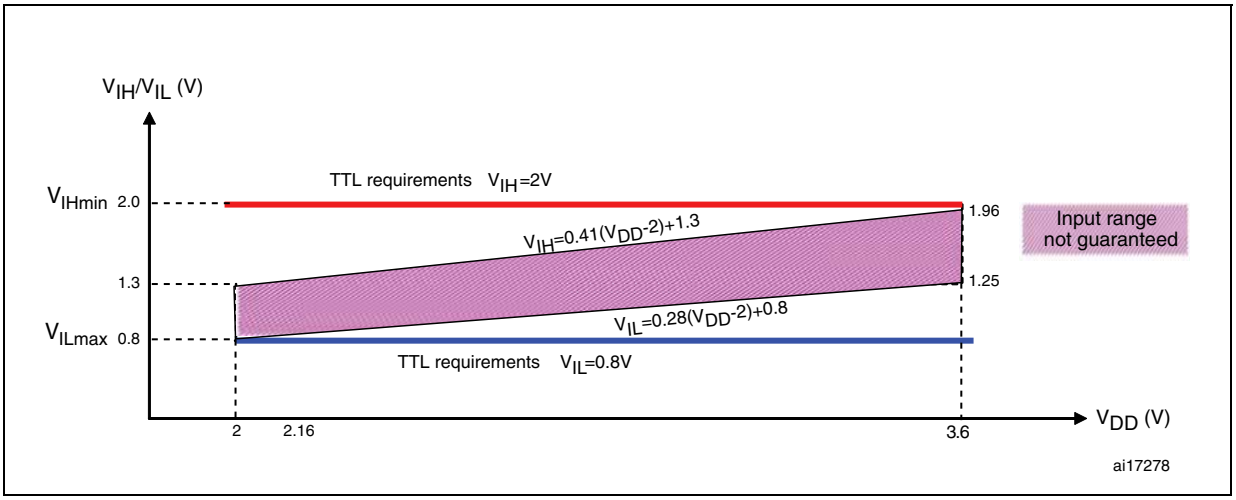
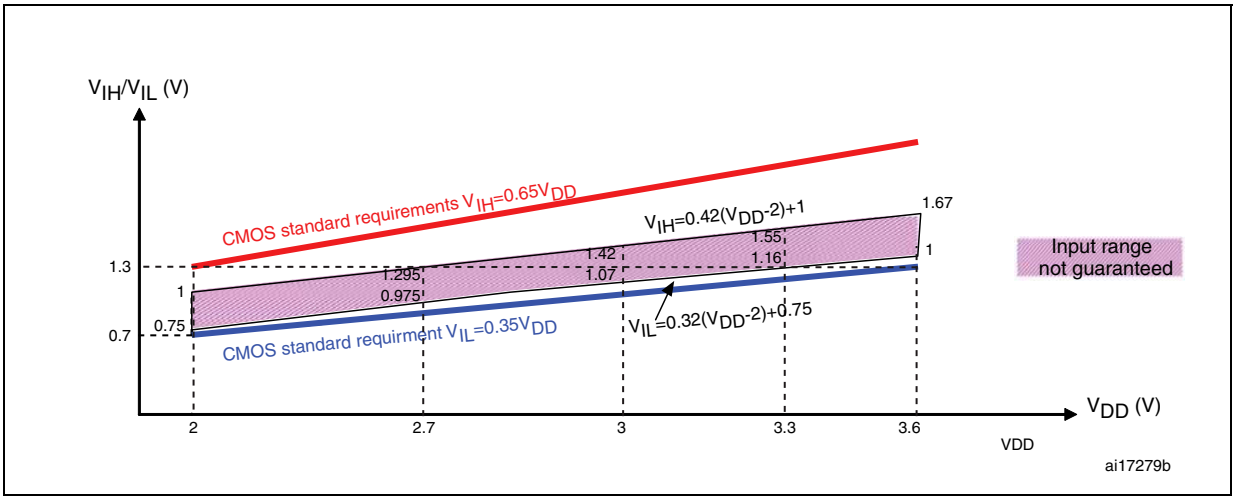


Figure 42. 5 V tolerant I/O input characteristics - CMOS port



SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 52. SDIO high-speed mode

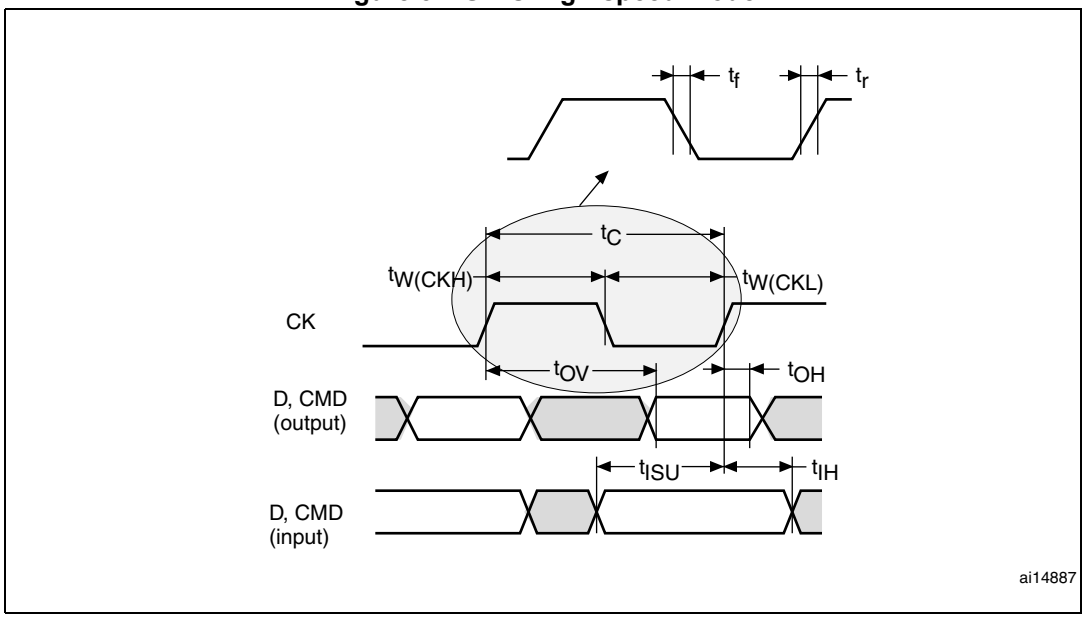


Figure 53. SD default mode

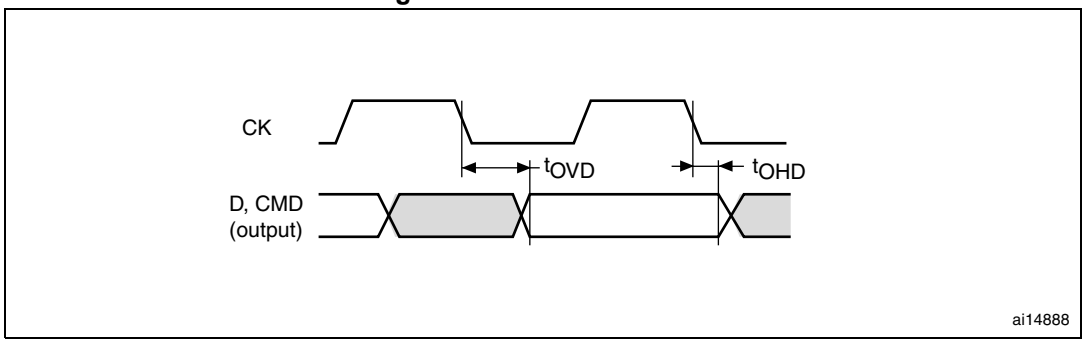
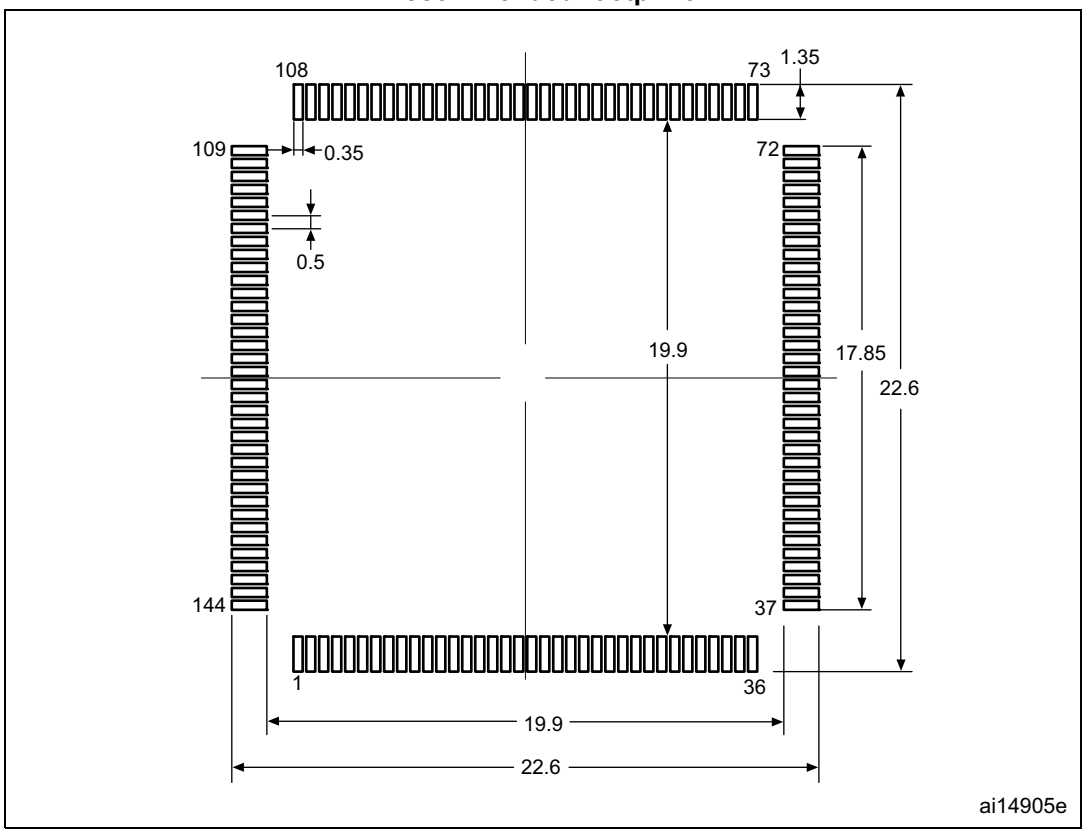


Table 58. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq$ 30 pF	0	48	MHz
tW(CKL)	Clock low time, f_{PP} = 16 MHz	$C_L \leq$ 30 pF	32	-	ns
tW(CKH)	Clock high time, f_{PP} = 16 MHz	$C_L \leq$ 30 pF	30	-	
t_r	Clock rise time	$C_L \leq$ 30 pF	-	4	
t_f	Clock fall time	$C_L \leq$ 30 pF	-	5	

Figure 63. LQFP144 - 144-pin,20 x 20 mm low-profile quad flat package recommended footprint



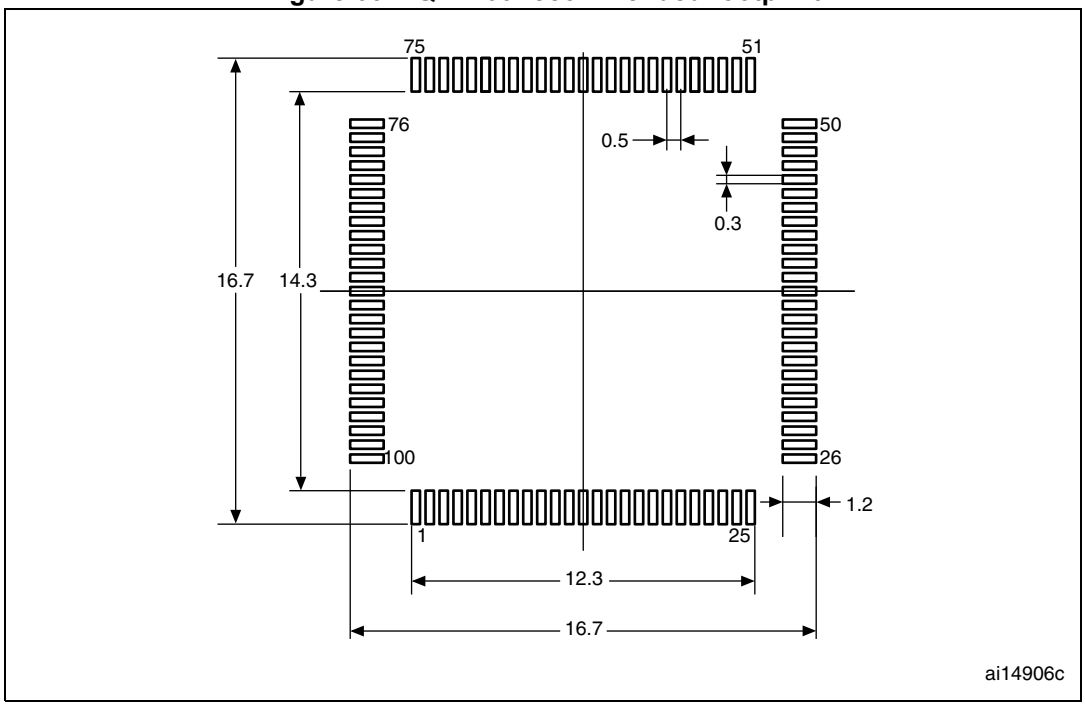
1. Dimensions are expressed in millimeters.

Table 70. LQPF100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.08	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 66. LQFP100 recommended footprint



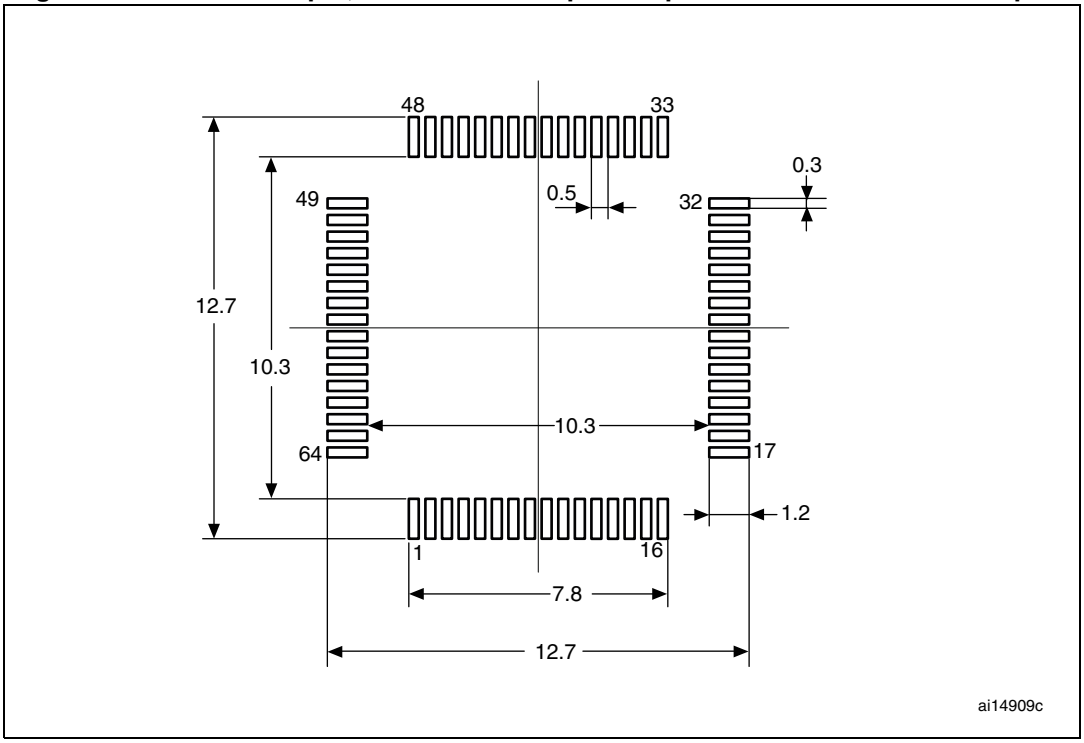
1. Dimensions are in millimeters.

Table 71. LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 69. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat recommended footprint



1. Dimensions are in millimeters.

6.5.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in *Table 73: STM32F103xF and STM32F103xG ordering information scheme*.

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F103xF and STM32F103xG at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 82 °C (measured according to JESD51-2), I_{DDmax} = 50 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V and maximum 8 I/Os used at the same time in output at low level with I_{OL} = 20 mA, V_{OL}= 1.3 V

P_{INTmax} = 50 mA × 3.5 V= 175 mW

P_{IOmax} = 20 × 8 mA × 0.4 V + 8 × 20 mA × 1.3 V = 272 mW

This gives: P_{INTmax} = 175 mW and P_{IOmax} = 272 mW:

P_{Dmax} = 175 + 272 = 447 mW

Thus: P_{Dmax} = 447 mW

Using the values obtained in *Table 72* T_{Jmax} is calculated as follows:

– For LQFP100, 46 °C/W

T_{Jmax} = 82 °C + (46 °C/W × 447 mW) = 82 °C + 20.6 °C = 102.6 °C

This is within the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 6 (see *Table 73: STM32F103xF and STM32F103xG ordering information scheme*).

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 115 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW