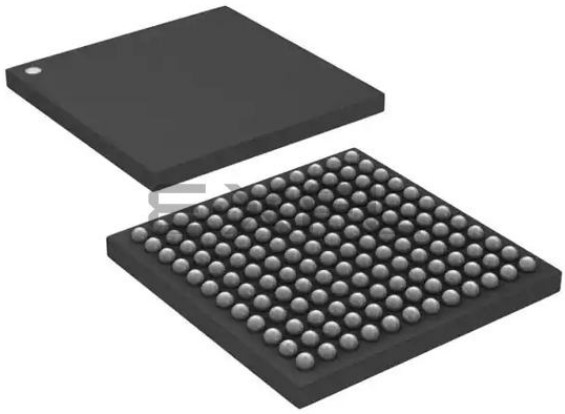

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LFBGA
Supplier Device Package	144-LFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zgh6jtr

1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F103xF and STM32F103xG XL-density performance line microcontrollers. For more details on the whole STMicroelectronics STM32F103xF/G family, please refer to *Section 2.2: Full compatibility throughout the family*.

The XL-density STM32F103xF/G datasheet should be read in conjunction with the STM32F10xxx reference manual.
For information on programming, erasing and protection of the internal Flash memory please refer to the *STM32F10xxx Flash programming manual.*
The reference and Flash programming manuals are both available from the STMicroelectronics website *www.st.com*.

For information on the Cortex®-M3 core please refer to the Cortex®-M3 Technical Reference Manual, available from the *www.arm.com* website at the following address: *http://infocenter.arm.com*.

2.3 Overview

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F103xF and STM32F103xG performance line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.3.3 Embedded Flash memory

768 Kbytes to 1 Mbyte of embedded Flash are available for storing programs and data. The Flash memory is organized as two banks. The first bank has a size of 512 Kbytes. The second bank is either 256 or 512 Kbytes depending on the device. This gives the device the capability of writing to one bank while executing code from the other bank (read-while-write capability).

2.3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.14 Voltage regulator

The regulator has three operation modes: main (MR), low-power (LPR) and power down.

- MR is used in the nominal regulation mode (Run)
- LPR is used in the Stop modes.
- Power down is used in Standby mode: the regulator output is in high impedance: the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost)

This regulator is always enabled after reset. It is disabled in Standby mode.

2.3.15 Low-power modes

The STM32F103xF and STM32F103xG performance line supports three low-power modes to achieve the best compromise between low-power consumption, short startup time and available wakeup sources:

- **Sleep** mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop** mode

  Stop mode achieves the lowest power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.
  The device can be woken up from Stop mode by any of the EXTI line. The EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm or the USB wakeup.

- **Standby** mode

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the Backup domain and Standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm occurs.

Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

2.3.16 DMA

The flexible 12-channel general-purpose DMAs (7 channels for DMA1 and 5 channels for DMA2) are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. The two DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2C, USART, general-purpose, basic and advanced-control timers TIMx, DAC, I^2S, SDIO and ADC.

2.3.17 RTC (real-time clock) and backup registers

The RTC and the backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are forty-two 16-bit registers used to store 84 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, and they are not reset when the device wakes up from the Standby mode.

The real-time clock provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and a periodic interrupt. It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 40 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation. The RTC features a 32-bit programmable counter for long term measurement using the Compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

2.3.18 Timers and watchdogs

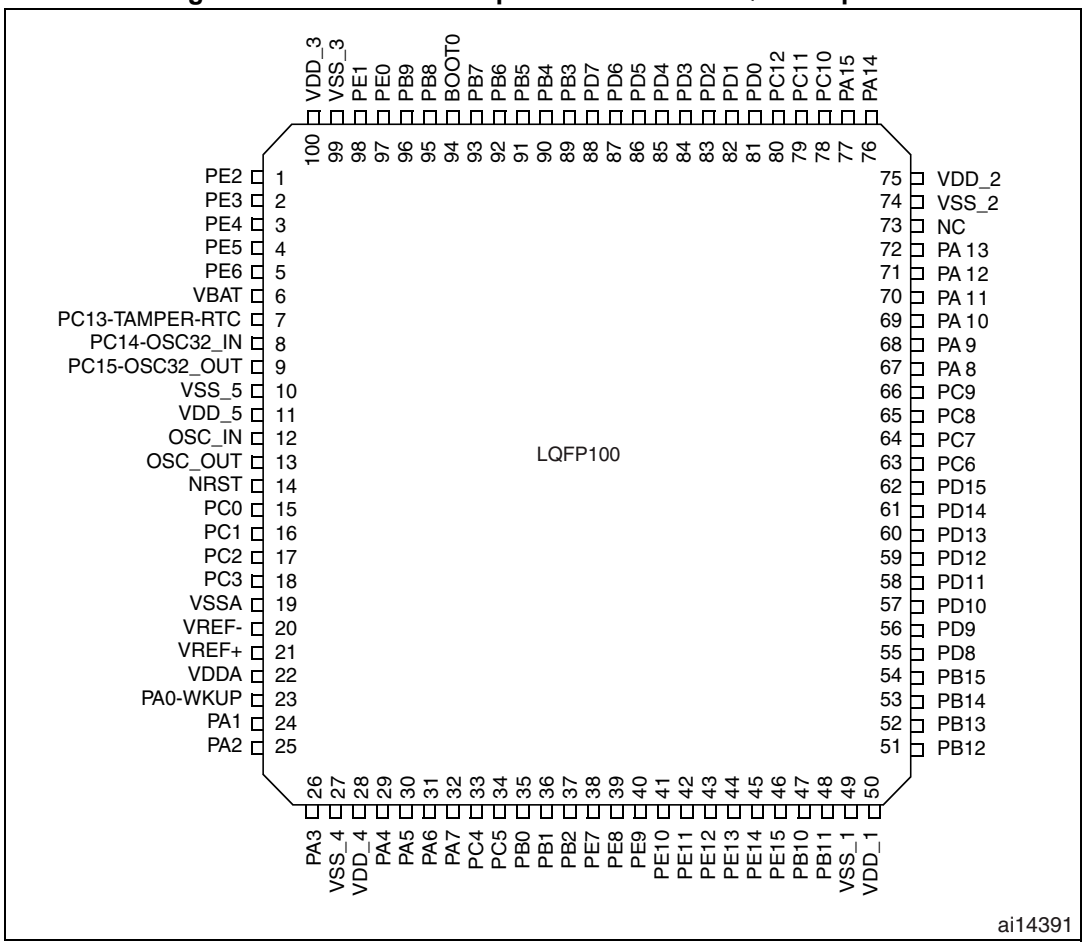
The XL-density STM32F103xF/G performance line devices include up to two advanced-control timers, up to ten general-purpose timers, two basic timers, two watchdog timers and a SysTick timer.

Table 4 compares the features of the advanced-control, general-purpose and basic timers.

Table 4. STM32F103xF and STM32F103xG timer feature comparison

Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
TIM1, TIM8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	Yes
TIM2, TIM3, TIM4, TIM5	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
TIM9, TIM12	16-bit	Up	Any integer between 1 and 65536	No	2	No
TIM10, TIM11 TIM13, TIM14	16-bit	Up	Any integer between 1 and 65536	No	1	No
TIM6, TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

Figure 5. STM32F103xF/G performance line LQFP100 pinout



1. The above figure shows the package top view.

Table 5. STM32F103xF and STM32F103xG pin definitions

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
A3	-	1	1	PE2	I/O	FT	PE2	TRACECK / FSMC_A23	-
A2	-	2	2	PE3	I/O	FT	PE3	TRACED0 / FSMC_A19	-
B2	-	3	3	PE4	I/O	FT	PE4	TRACED1/ FSMC_A20	-
B3	-	4	4	PE5	I/O	FT	PE5	TRACED2/ FSMC_A21	TIM9_CH1
B4	-	5	5	PE6	I/O	FT	PE6	TRACED3 / FSMC_A22	TIM9_CH2
C2	1	6	6	V_{BAT}	S		V_{BAT}	-	-
A1	2	7	7	PC13-TAMPER-RTC(5)	I/O		PC13(6)	TAMPER-RTC	-
B1	3	8	8	PC14-OSC32_IN(5)	I/O		PC14(6)	OSC32_IN	-
C1	4	9	9	PC15-OSC32_OUT(5)	I/O		PC15(6)	OSC32_OUT	-
C3	-	-	10	PF0	I/O	FT	PF0	FSMC_A0	-
C4	-	-	11	PF1	I/O	FT	PF1	FSMC_A1	-
D4	-	-	12	PF2	I/O	FT	PF2	FSMC_A2	-
E2	-	-	13	PF3	I/O	FT	PF3	FSMC_A3	-
E3	-	-	14	PF4	I/O	FT	PF4	FSMC_A4	-
E4	-	-	15	PF5	I/O	FT	PF5	FSMC_A5	-
D2	-	10	16	V_{SS_5}	S		V_{SS_5}	-	-
D3	-	11	17	V_{DD_5}	S		V_{DD_5}	-	-
F3	-	-	18	PF6	I/O		PF6	ADC3_IN4 / FSMC_NIORD	TIM10_CH1
F2	-	-	19	PF7	I/O		PF7	ADC3_IN5 / FSMC_NREG	TIM11_CH1
G3	-	-	20	PF8	I/O		PF8	ADC3_IN6 / FSMC_NIOWR	TIM13_CH1
G2	-	-	21	PF9	I/O		PF9	ADC3_IN7 / FSMC_CD	TIM14_CH1
G1	-	-	22	PF10	I/O		PF10	ADC3_IN8 / FSMC_INTR	-
D1	5	12	23	OSC_IN	I		OSC_IN	-	PD0(7)
E1	6	13	24	OSC_OUT	O		OSC_OUT	-	PD1(7)
F1	7	14	25	NRST	I/O		NRST	-	-
H1	8	15	26	PC0	I/O		PC0	ADC123_IN10	-
H2	9	16	27	PC1	I/O		PC1	ADC123_IN11	-

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

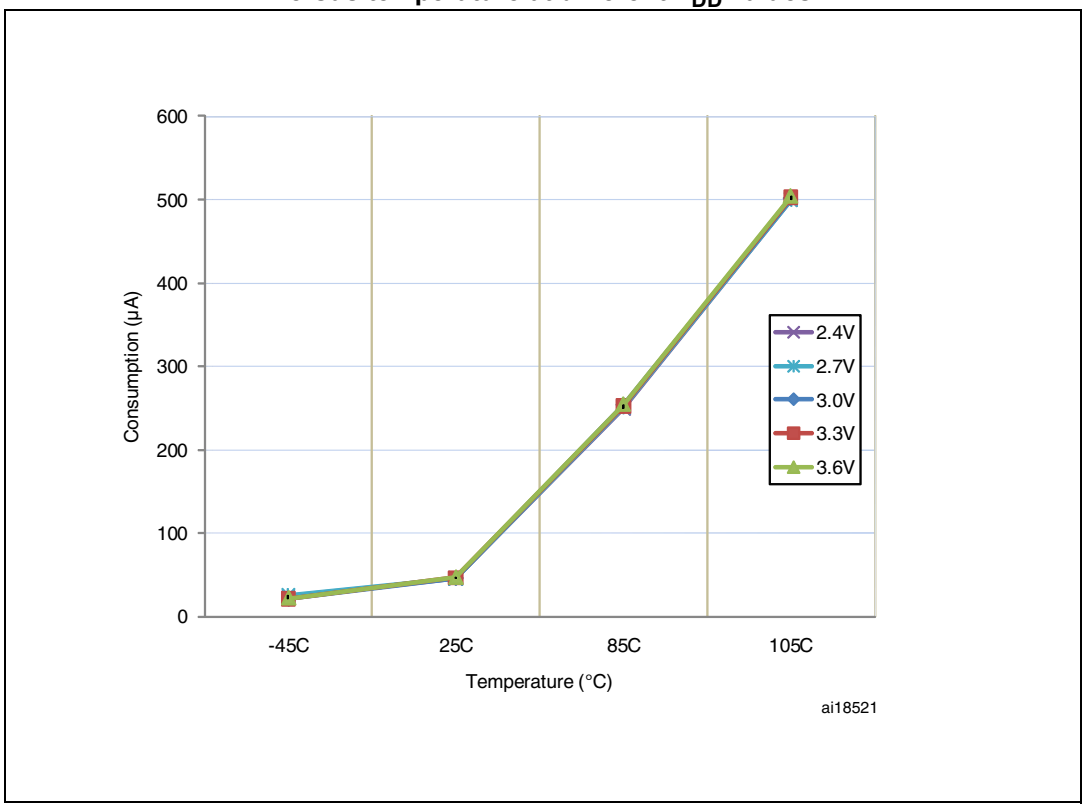
Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
E11	40	66	99	PC9	I/O	FT	PC9	TIM8_CH4 / SDIO_D1	TIM3_CH4
E12	41	67	100	PA8	I/O	FT	PA8	USART1_CK / TIM1_CH1(7) / MCO	-
D12	42	68	101	PA9	I/O	FT	PA9	USART1_TX(7) / TIM1_CH2(7)	-
D11	43	69	102	PA10	I/O	FT	PA10	USART1_RX(7) / TIM1_CH3(7)	-
C12	44	70	103	PA11	I/O	FT	PA11	USART1_CTS / USB_DM / CAN_RX(7) / TIM1_CH4(7)	-
B12	45	71	104	PA12	I/O	FT	PA12	USART1_RTS / USB_DP / CAN_TX(7) / TIM1_ETR(7)	-
A12	46	72	105	PA13	I/O	FT	JTMS-SWDIO	-	PA13
C11	-	73	106	Not connected					
G9	47	74	107	V_{SS_2}	S		V_{SS_2}	-	-
F9	48	75	108	V_{DD_2}	S		V_{DD_2}	-	-
A11	49	76	109	PA14	I/O	FT	JTCK-SWCLK	-	PA14
A10	50	77	110	PA15	I/O	FT	JTDI	SPI3_NSS / I2S3_WS	TIM2_CH1_ETR PA15/ SPI1_NSS
B11	51	78	111	PC10	I/O	FT	PC10	UART4_TX / SDIO_D2	USART3_TX
B10	52	79	112	PC11	I/O	FT	PC11	UART4_RX / SDIO_D3	USART3_RX
C10	53	80	113	PC12	I/O	FT	PC12	UART5_TX / SDIO_CK	USART3_CK
E10	-	81	114	PD0	I/O	FT	PD0	FSMC_D2(9)	CAN_RX
D10	-	82	115	PD1	I/O	FT	PD1	FSMC_D3(9)	CAN_TX
E9	54	83	116	PD2	I/O	FT	PD2	TIM3_ETR / UART5_RX / SDIO_CMD	-
D9	-	84	117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
C9	-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
B9	-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
E7	-	-	120	V_{SS_10}	S		V_{SS_10}	-	-
F7	-	-	121	V_{DD_10}	S		V_{DD_10}	-	-
A8	-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX

Table 6. FSMC pin definition (continued)

Pins	FSMC					LQFP100[1]
	CF	CF/IDE	NOR/PSRAM/ SRAM	NOR/PSRAM Mux	NAND 16 bit	
PD9	D14	D14	D14	DA14	D14	Yes
PD10	D15	D15	D15	DA15	D15	Yes
PD11	-	-	A16	A16	CLE	Yes
PD12	-	-	A17	A17	ALE	Yes
PD13	-	-	A18	A18		Yes
PD14	D0	D0	D0	DA0	D0	Yes
PD15	D1	D1	D1	DA1	D1	Yes
PG2	-	-	A12	-	-	-
PG3	-	-	A13	-	-	-
PG4	-	-	A14	-	-	-
PG5	-	-	A15	-	-	-
PG6	-	-	-	-	INT2	-
PG7	-	-	-	-	INT3	-
PD0	D2	D2	D2	DA2	D2	Yes
PD1	D3	D3	D3	DA3	D3	Yes
PD3	-	-	CLK	CLK	-	Yes
PD4	NOE	NOE	NOE	NOE	NOE	Yes
PD5	NWE	NWE	NWE	NWE	NWE	Yes
PD6	NWAIT	NWAIT	NWAIT	NWAIT	NWAIT	Yes
PD7	-	-	NE1	NE1	NCE2	Yes
PG9	-	-	NE2	NE2	NCE3	-
PG10	NCE4_1	NCE4_1	NE3	NE3	-	-
PG11	NCE4_2	NCE4_2	-	-	-	-
PG12	-	-	NE4	NE4	-	-
PG13	-	-	A24	A24	-	-
PG14	-	-	A25	A25	-	-
PB7	-	-	NADV	NADV	-	Yes
PE0	-	-	NBL0	NBL0	-	Yes
PE1	-	-	NBL1	NBL1	-	Yes

1. Ports F and G are not available in devices delivered in 100-pin packages.

Figure 15. Typical current consumption in Stop mode with regulator in run mode versus temperature at different V_{DD} values



Low-speed internal (LSI) RC oscillator

Table 26. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI}(2)	Frequency	30	40	60	kHz
$t_{su(LSI)}$(3)	LSI oscillator startup time	-	-	85	µs
$I_{DD(LSI)}$(3)	LSI oscillator power consumption	-	0.65	1.2	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization results, not tested in production.
3. Guaranteed by design, not tested in production.

Wakeup time from low-power mode

The wakeup times given in *Table 27* is measured on a wakeup phase with a 8-MHz HSI RC oscillator. The clock source used to wake up the device depends from the current operating mode:

- Stop or Standby mode: the clock source is the RC oscillator
- Sleep mode: the clock source is the clock that was set before entering Sleep mode.

All timings are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in *Table 10*.

Table 27. Low-power mode wakeup timings

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$(1)	Wakeup from Sleep mode	1.8	µs
t_{WUSTOP}(1)	Wakeup from Stop mode (regulator in run mode)	3.6	µs
	Wakeup from Stop mode (regulator in low-power mode)	5.4	
$t_{WUSTDBY}$(1)	Wakeup from Standby mode	50	µs

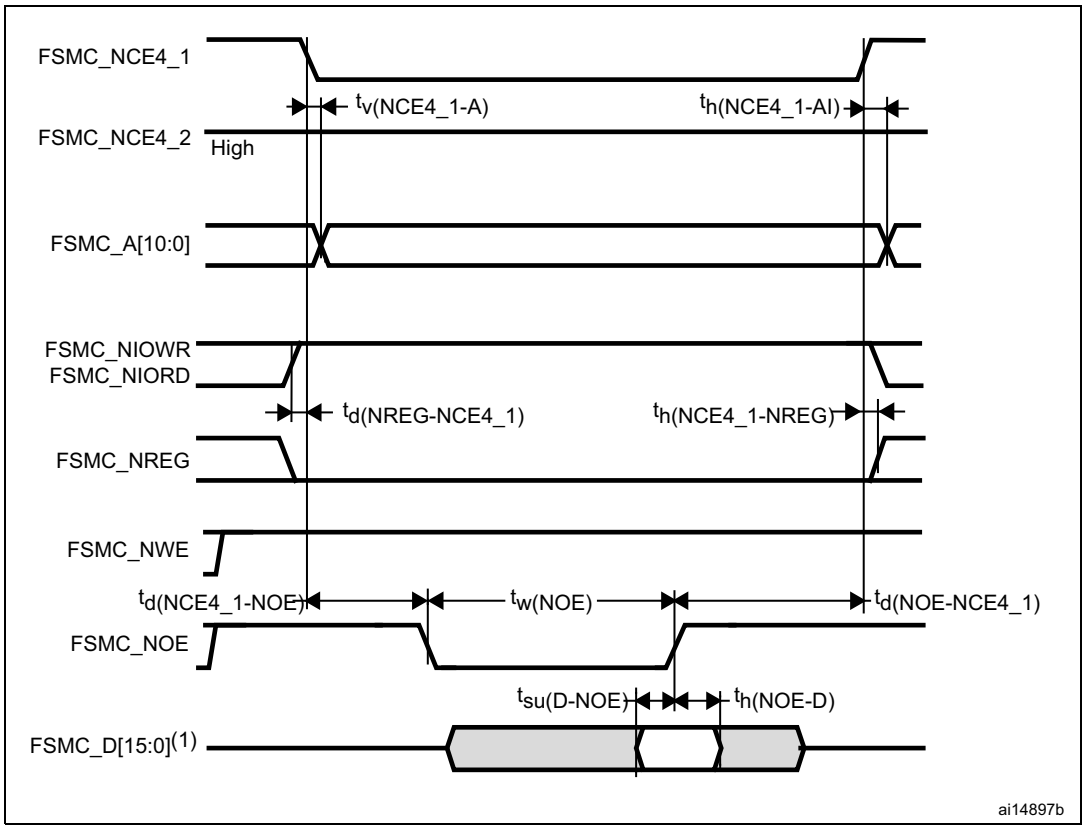
1. The wakeup times are measured from the wakeup event to the point in which the user application code reads the first instruction.

Table 30. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Value	Unit
			Min(1)	
N_{END}	Endurance	T_A = –40 to +85 °C (6 suffix versions) T_A = –40 to +105 °C (7 suffix versions)	10	kcycles
t_{RET}	Data retention	1 kcycle(2) at T_A = 85 °C	30	Years
		1 kcycle(2) at T_A = 105 °C	10	
		10 kcycles(2) at T_A = 55 °C	20	

1. Guaranteed by characterization results, not tested in production.
2. Cycling performed over the whole temperature range.

Figure 32. PC Card/CompactFlash controller waveforms for attribute memory read access



1. Only data bits 0...7 are read (bits 8...15 are disregarded).

Figure 35. PC Card/CompactFlash controller waveforms for I/O space write access

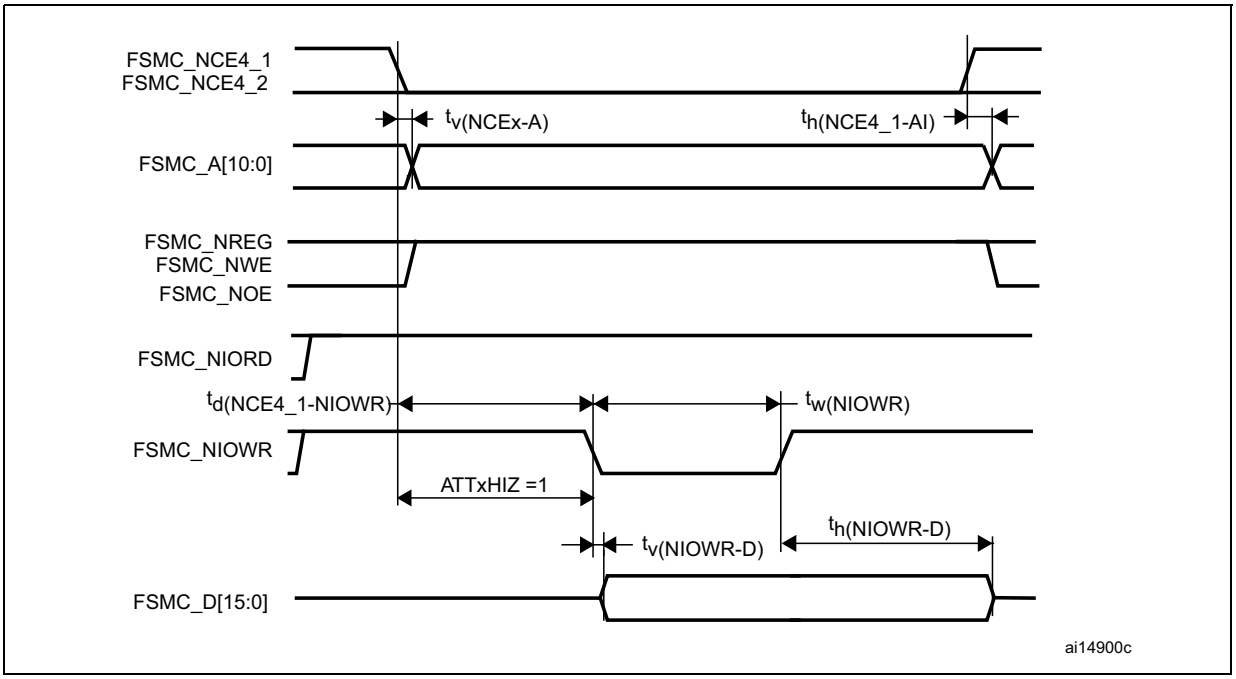


Table 40. Switching characteristics for PC Card/CF read and write cycles in attribute/common space

Symbol	Parameter	Min	Max	Unit
$t_{v(NCEx-A)}$	FSMC_NCEx low to FSMC_Ay valid	-	0	ns
$t_{h(NCEx-AI)}$	FSMC_NCEx high to FSMC_Ax invalid	0	-	
$t_{d(NREG-NCEx)}$	FSMC_NCEx low to FSMC_NREG valid	-	2	
$t_{h(NCEx-NREG)}$	FSMC_NCEx high to FSMC_NREG invalid	t_{HCLK} + 4	-	
$t_{d(NCEx\_NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5t_{HCLK}$ + 1	
$t_{d(NCEx\_NOE)}$	FSMC_NCEx low to FSMC_NOE low	-	$5t_{HCLK}$ + 1	
$t_{w(NOE)}$	FSMC_NOE low width	$8t_{HCLK}$ - 0.5	$8t_{HCLK}$ + 1	
$t_{d(NOE-NCEx}$	FSMC_NOE high to FSMC_NCEx high	$5t_{HCLK}$ - 0.5	-	
$t_{su(D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	32	-	
$t_{h(NOE-D)}$	FSMC_NOE high to FSMC_D[15:0] invalid	t_{HCLK}	-	
$t_{w(NWE)}$	FSMC_NWE low width	$8t_{HCLK}$ – 1	$8t_{HCLK}$ + 4	
$t_{d(NWE\_NCEx)}$	FSMC_NWE high to FSMC_NCEx high	$5t_{HCLK}$ + 1.5	-	
$t_{d(NCEx-NWE)}$	FSMC_NCEx low to FSMC_NWE low	-	$5t_{HCLK}$ + 1	
$t_{v(NWE-D)}$	FSMC_NWE low to FSMC_D[15:0] valid	-	0	
$t_{h(NWE-D)}$	FSMC_NWE high to FSMC_D[15:0] invalid	$11t_{HCLK}$	-	
$t_{d(D-NWE)}$	FSMC_D[15:0] valid before FSMC_NWE high	$13t_{HCLK}$ + 2.5	-	

SD/SDIO MMC card host interface (SDIO) characteristics

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 10*.

Refer to *Section 5.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (D[7:0], CMD, CK).

Figure 52. SDIO high-speed mode

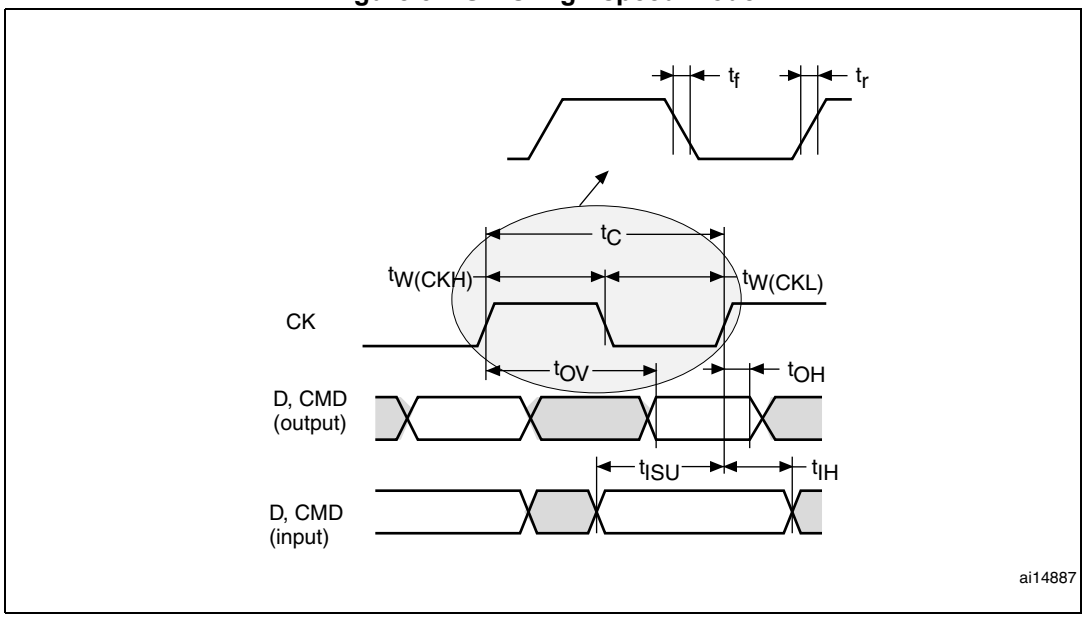


Figure 53. SD default mode

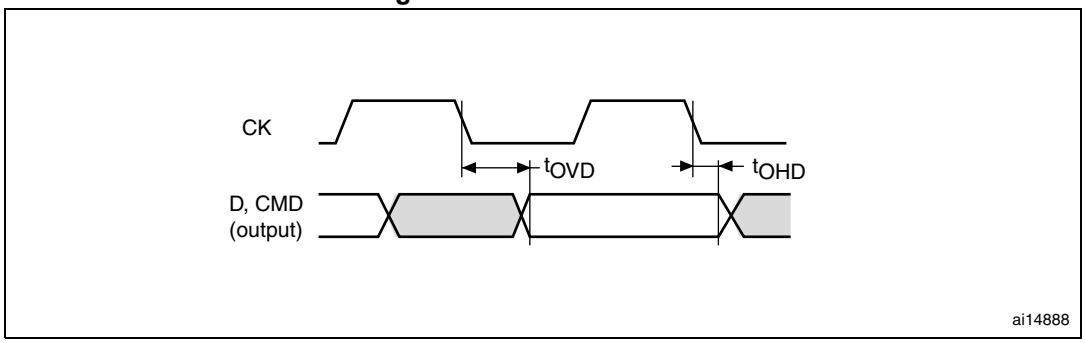


Table 58. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	$C_L \leq$ 30 pF	0	48	MHz
tW(CKL)	Clock low time, f_{PP} = 16 MHz	$C_L \leq$ 30 pF	32	-	ns
tW(CKH)	Clock high time, f_{PP} = 16 MHz	$C_L \leq$ 30 pF	30	-	
t_r	Clock rise time	$C_L \leq$ 30 pF	-	4	
t_f	Clock fall time	$C_L \leq$ 30 pF	-	5	

Table 58. SD / MMC characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
CMD, D inputs (referenced to CK)					
t_{ISU}	Input setup time	$C_L \leq 30$ pF	2	-	ns
t_{IH}	Input hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode					
t_{OV}	Output valid time	$C_L \leq 30$ pF	-	6	ns
t_{OH}	Output hold time	$C_L \leq 30$ pF	0	-	
CMD, D outputs (referenced to CK) in SD default mode(1)					
t_{OVD}	Output valid default time	$C_L \leq 30$ pF	-	7	ns
t_{OHD}	Output hold default time	$C_L \leq 30$ pF	0.5	-	

1. Refer to SDIO_CLKCR, the SDI clock control register to control the CK output.

USB characteristics

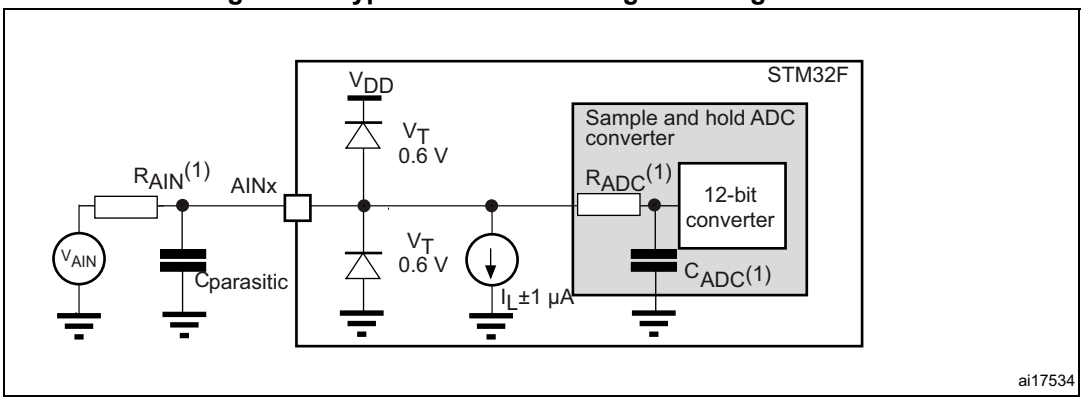
The USB interface is USB-IF certified (Full Speed).

Table 59. USB startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB transceiver startup time	1	µs

1. Guaranteed by design, not tested in production.

Figure 56. Typical connection diagram using the ADC

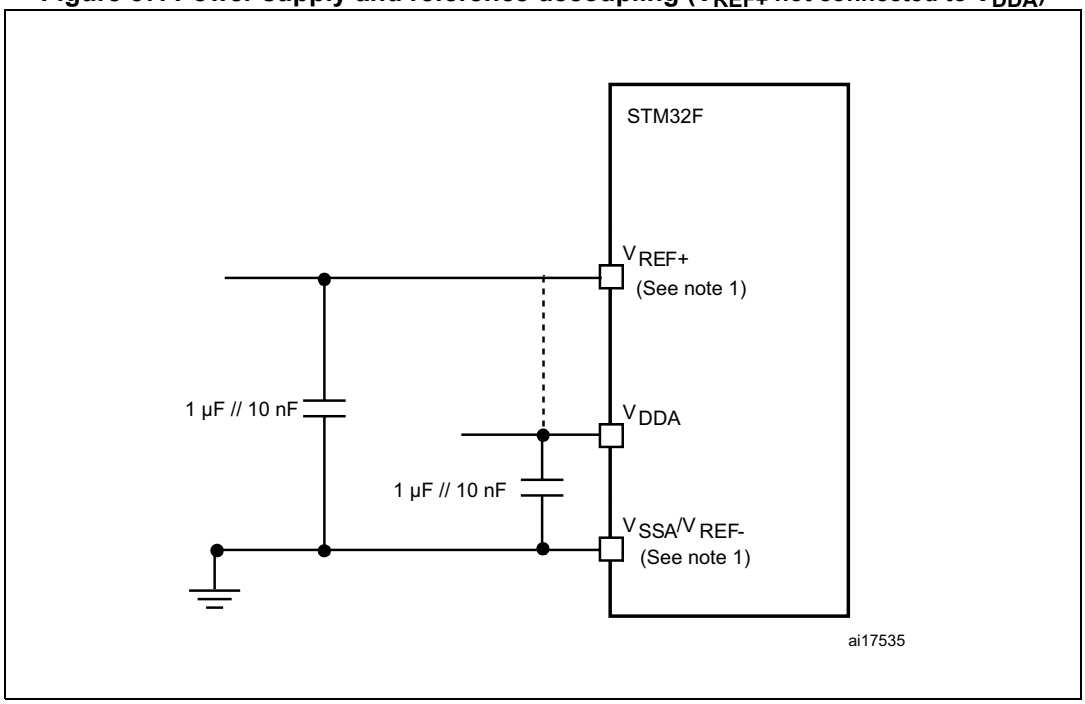


1. Refer to *Table 62* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 57* or *Figure 58*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 10 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 57. Power supply and reference decoupling (V_{REF+} not connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Table 66. DAC characteristics (continued)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
INL(2)	Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023)	-	-	±1	LSB	Given for the DAC in 10-bit configuration
		-	-	±4	LSB	Given for the DAC in 12-bit configuration
Offset(2)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	±10	mV	
		-	-	±3	LSB	Given for the DAC in 10-bit at V_{REF+} = 3.6 V
		-	-	±12	LSB	Given for the DAC in 12-bit at V_{REF+} = 3.6 V
Gain error(2)	Gain error	-	-	±0.5	%	Given for the DAC in 12bit configuration
$t_{SETTLING}$(2)	Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±1LSB	-	3	4	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB)	-	-	1	MS/s	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ
t_{WAKEUP}(2)	Wakeup time from off state (Setting the ENx bit in the DAC Control register)	-	6.5	10	µs	$C_{LOAD} \leq$ 50 pF, $R_{LOAD} \geq$ 5 kΩ input code between lowest and highest possible ones.
PSRR+ (1)	Power supply rejection ratio (to V_{DDA}) (static DC measurement	-	–67	–40	dB	No R_{LOAD}, C_{LOAD} = 50 pF

1. Guaranteed by design, not tested in production.
2. The quiescent mode corresponds to a state where the DAC maintains a stable output level to ensure that no dynamic consumption occurs.
3. Preliminary values.

Table 68. LFBGA144 – 144-ball low profile fine pitch ball grid array, 10 x 10 mm, 0.8 mm pitch, package mechanical data (continued)

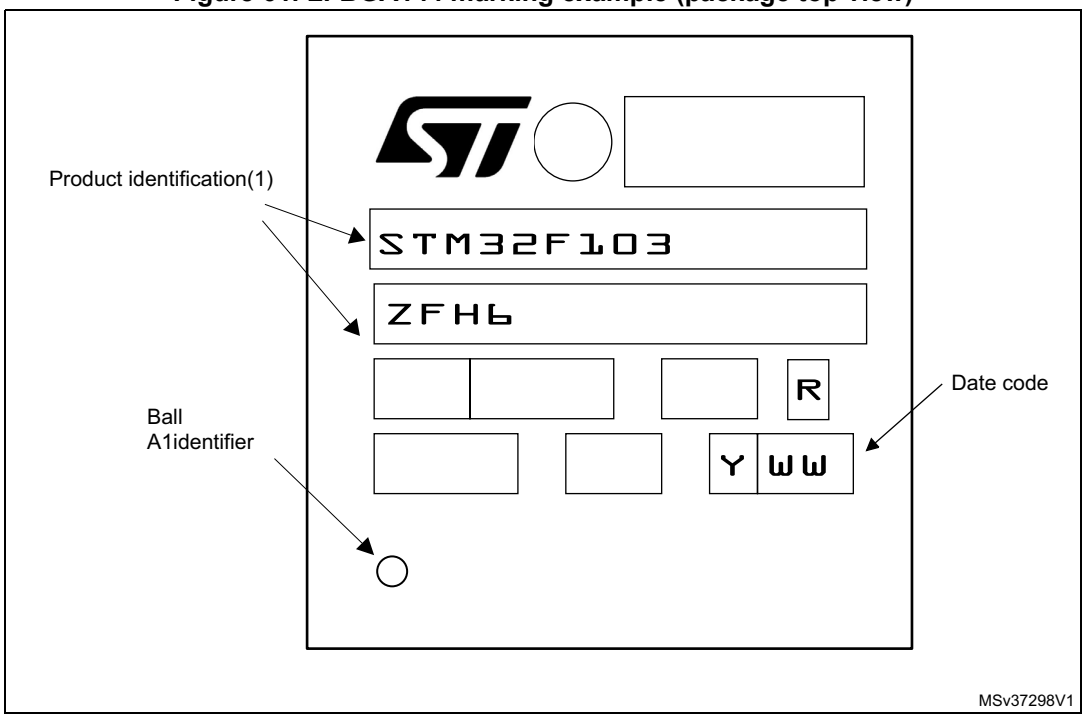
Symbol	millimeters			inches[1]		
	Min	Typ	Max	Typ	Min	Max
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. STATSChipPAC package dimensions.

Device marking for LFBGA144 package

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 61. LFBGA144 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 69. LQFP144 - 144-pin, 20 x 20 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	21.800	22.000	22.200	0.8583	0.8661	0.8740
D1	19.800	20.000	20.200	0.7795	0.7874	0.7953
D3	-	17.500	-	-	0.6890	-
E	21.800	22.000	22.200	0.8583	0.8661	0.8740
E1	19.800	20.000	20.200	0.7795	0.7874	0.7953
E3	-	17.500	-	-	0.6890	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0°	3.5°	7°	0°	3.5°	7°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Table 74. Document revision history

Date	Revision	Changes
15-May-2015	4	Added document status on first page. Replace DAC1_OUT/DAC2_OUT by DAC_OUT1/DAC_OUT2, and updated TIM5 in *Figure 1: STM32F103xF and STM32F103xG performance line block diagram on page 12*. Replaced USBDP/USBDM by USB_DP/USB_DM in the whole document. Updated notes related to electrical values guaranteed by characterization results. Updated *Table 20: Peripheral current consumption*. Updated *Table 36: Synchronous multiplexed NOR/PSRAM read timings* to *Table 39: Synchronous non-multiplexed PSRAM write timings*(added FSMC_NWAIT timings). Updated *Figure 26: Synchronous multiplexed NOR/PSRAM read timings on page 73* and *Figure 28: Synchronous non-multiplexed NOR/PSRAM read timings on page 77* and *Figure 35: PC Card/CompactFlash controller waveforms for I/O space write access on page 83*. Updated CDM class in *Table 46: ESD absolute maximum ratings*. Updated *Figure 44: I/O AC characteristics definition on page 96* and *Figure 45: Recommended NRST pin protection on page 97*. Updated *Figure 49: SPI timing diagram - master mode(1) on page 96*. Modified note 3 in *Table 56: SPI characteristics*. *Section : I2C interface characteristics*: Updated introduction, updated *Table 54: I^2C characteristics* and *Figure 46: I^2C bus AC waveforms and measurement circuit on page 99*. Modified note 2 in *Table 64: ADC accuracy - limited test conditions*, *Figure 55: ADC accuracy characteristics on page 110* and *Figure 56: Typical connection diagram using the ADC on page 111*. Updated *Figure 57: Power supply and reference decoupling (V_{REF+} not connected to V_{DDA}) on page 111* and *Figure 58: Power supply and reference decoupling (V_{REF+} connected to V_{DDA}) on page 112*. Updated I_{DDA} description and Offset comment in *Table 66: DAC characteristics*. Updated *Section 6.1: LFBGA144 package information* and added *Section : Device marking for LFBGA144 package*. Updated *Section 6.2: LQFP144 package information* and added *Section : Device marking for LQFP144 package*. Updated *Section 6.3: LQFP100 package information* and added *Section : Device marking for LQFP100 package*. Updated *Section 6.4: LQFP64 package information* and added *Section : Device marking for LQFP64 package*.