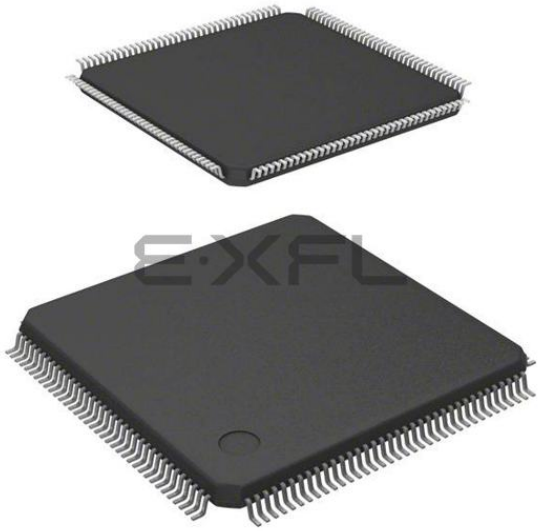

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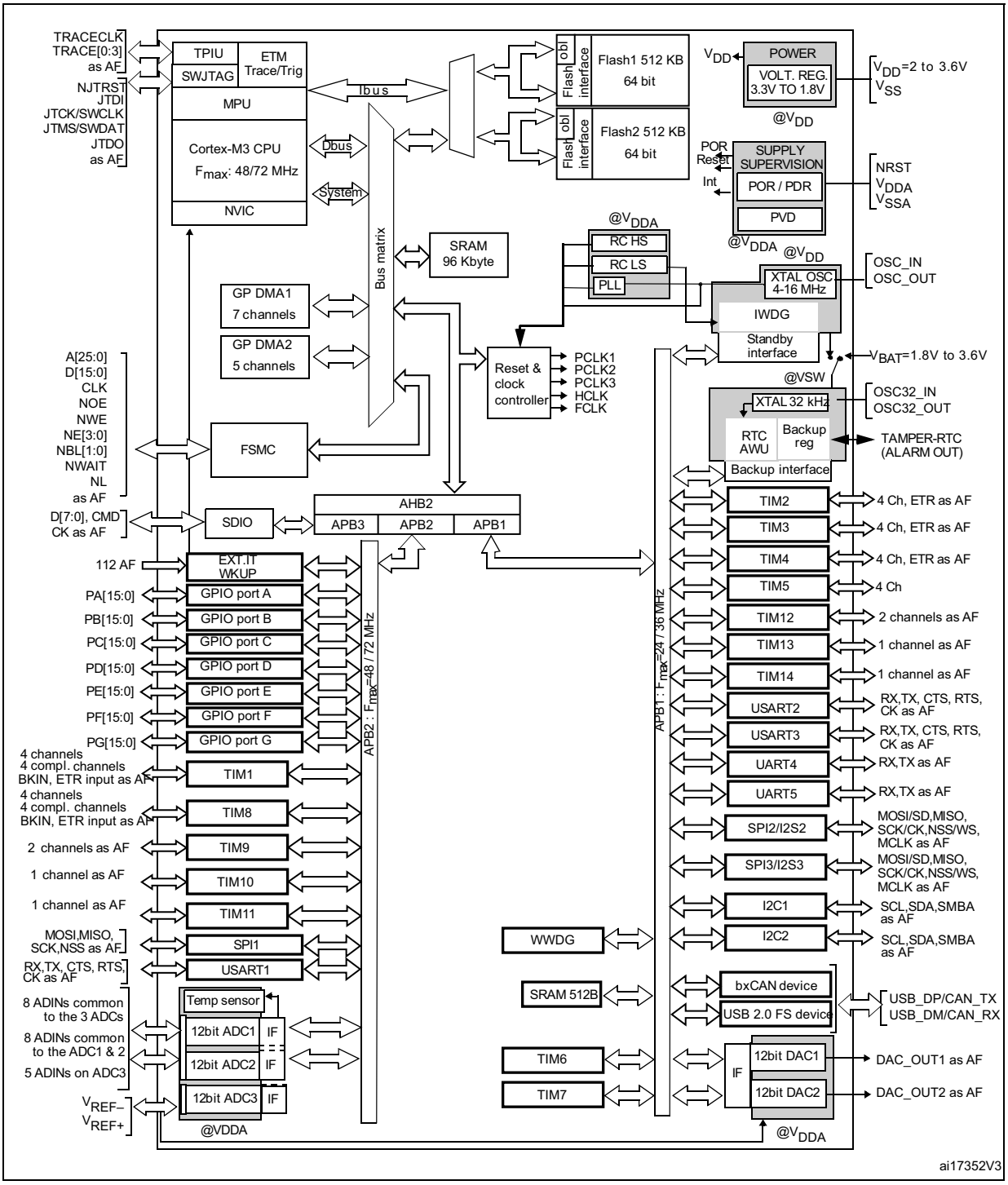
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART, USB
Peripherals	DMA, Motor Control PWM, PDR, POR, PVD, PWM, Temp Sensor, WDT
Number of I/O	112
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 21x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f103zgt6j

Figure 1. STM32F103xF and STM32F103xG performance line block diagram



1. T_A = –40 °C to +85 °C (suffix 6, see *Table 73*) or –40 °C to +105 °C (suffix 7, see *Table 73*), junction temperature up to 105 °C or 125 °C, respectively.
2. AF = alternate function on I/O port pin.9

2.3 Overview

2.3.1 ARM® Cortex®-M3 core with embedded Flash and SRAM

The ARM Cortex®-M3 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM Cortex®-M3 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

With its embedded ARM core, STM32F103xF and STM32F103xG performance line family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

2.3.2 Memory protection unit

The memory protection unit (MPU) is used to separate the processing of tasks from the data protection. The MPU can manage up to 8 protection areas that can all be further divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The memory protection unit is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

2.3.3 Embedded Flash memory

768 Kbytes to 1 Mbyte of embedded Flash are available for storing programs and data. The Flash memory is organized as two banks. The first bank has a size of 512 Kbytes. The second bank is either 256 or 512 Kbytes depending on the device. This gives the device the capability of writing to one bank while executing code from the other bank (read-while-write capability).

2.3.4 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

2.3.10 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-16 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example with failure of an indirectly used external oscillator).

Several prescalers allow the configuration of the AHB frequency, the high speed APB (APB2) and the low speed APB (APB1) domains. The maximum frequency of the AHB and the high speed APB domains is 72 MHz. The maximum allowed frequency of the low speed APB domain is 36 MHz. See *Figure 2* for details on the clock tree.

2.3.11 Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from user Flash: you have an option to boot from any of two memory banks. By default, boot from Flash memory bank 1 is selected. You can choose to boot from Flash memory bank 2 by setting a bit in the option bytes.
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1.

2.3.12 Power supply schemes

- V_{DD} = 2.0 to 3.6 V: external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 2.0 to 3.6 V: external analog power supplies for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to VDDA is 2.4 V when the ADC or DAC is used). V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.8 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to *Figure 10: Power supply scheme*.

2.3.13 Power supply supervisor

The device has an integrated power-on reset (POR)/power-down reset (PDR) circuitry. It is always active, and ensures proper operation starting from/down to 2 V. The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software. Refer to *Table 12: Embedded reset and power control block characteristics* for the values of $V_{POR/PDR}$ and V_{PVD}.

Basic timers TIM6 and TIM7

These timers are mainly used for DAC trigger generation. They can also be used as a generic 16-bit time base.

Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0.
- Programmable clock source

2.3.19 I²C bus

Up to two I²C bus interfaces can operate in multimaster and slave modes. They can support standard and fast modes.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.3.20 Universal synchronous/asynchronous receiver transmitters (USARTs)

The STM32F103xF and STM32F103xG performance line embeds three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART3) and two universal asynchronous receiver transmitters (UART4 and UART5).

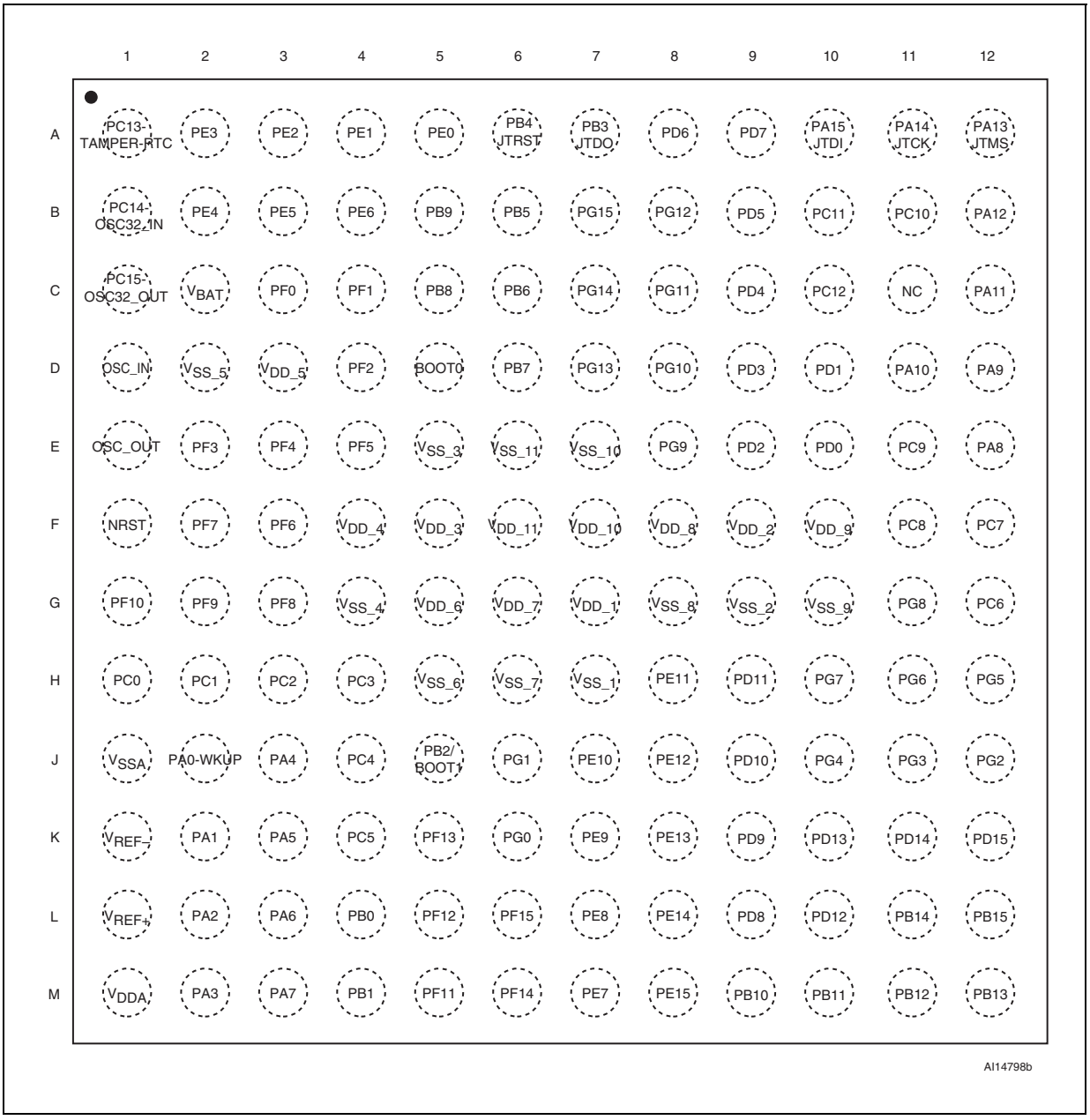
These five interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability.

The USART1 interface is able to communicate at speeds of up to 4.5 Mbit/s. The other available interfaces communicate at up to 2.25 Mbit/s.

USART1, USART2 and USART3 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller except for UART5.

3 Pinouts and pin descriptions

Figure 3. STM32F103xF/G BGA144 ballout



1. The above figure shows the package top view.

Table 5. STM32F103xF and STM32F103xG pin definitions

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
A3	-	1	1	PE2	I/O	FT	PE2	TRACECK / FSMC_A23	-
A2	-	2	2	PE3	I/O	FT	PE3	TRACED0 / FSMC_A19	-
B2	-	3	3	PE4	I/O	FT	PE4	TRACED1/ FSMC_A20	-
B3	-	4	4	PE5	I/O	FT	PE5	TRACED2/ FSMC_A21	TIM9_CH1
B4	-	5	5	PE6	I/O	FT	PE6	TRACED3 / FSMC_A22	TIM9_CH2
C2	1	6	6	V_{BAT}	S		V_{BAT}	-	-
A1	2	7	7	PC13-TAMPER-RTC(5)	I/O		PC13(6)	TAMPER-RTC	-
B1	3	8	8	PC14-OSC32_IN(5)	I/O		PC14(6)	OSC32_IN	-
C1	4	9	9	PC15-OSC32_OUT(5)	I/O		PC15(6)	OSC32_OUT	-
C3	-	-	10	PF0	I/O	FT	PF0	FSMC_A0	-
C4	-	-	11	PF1	I/O	FT	PF1	FSMC_A1	-
D4	-	-	12	PF2	I/O	FT	PF2	FSMC_A2	-
E2	-	-	13	PF3	I/O	FT	PF3	FSMC_A3	-
E3	-	-	14	PF4	I/O	FT	PF4	FSMC_A4	-
E4	-	-	15	PF5	I/O	FT	PF5	FSMC_A5	-
D2	-	10	16	V_{SS_5}	S		V_{SS_5}	-	-
D3	-	11	17	V_{DD_5}	S		V_{DD_5}	-	-
F3	-	-	18	PF6	I/O		PF6	ADC3_IN4 / FSMC_NIORD	TIM10_CH1
F2	-	-	19	PF7	I/O		PF7	ADC3_IN5 / FSMC_NREG	TIM11_CH1
G3	-	-	20	PF8	I/O		PF8	ADC3_IN6 / FSMC_NIOWR	TIM13_CH1
G2	-	-	21	PF9	I/O		PF9	ADC3_IN7 / FSMC_CD	TIM14_CH1
G1	-	-	22	PF10	I/O		PF10	ADC3_IN8 / FSMC_INTR	-
D1	5	12	23	OSC_IN	I		OSC_IN	-	PD0(7)
E1	6	13	24	OSC_OUT	O		OSC_OUT	-	PD1(7)
F1	7	14	25	NRST	I/O		NRST	-	-
H1	8	15	26	PC0	I/O		PC0	ADC123_IN10	-
H2	9	16	27	PC1	I/O		PC1	ADC123_IN11	-

Table 5. STM32F103xF and STM32F103xG pin definitions (continued)

Pins				Pin name	Type(1)	I / O level(2)	Main function(3) (after reset)	Alternate functions(4)	
LFBGA144	LQFP64	LQFP100	LQFP144					Default	Remap
E11	40	66	99	PC9	I/O	FT	PC9	TIM8_CH4 / SDIO_D1	TIM3_CH4
E12	41	67	100	PA8	I/O	FT	PA8	USART1_CK / TIM1_CH1(7) / MCO	-
D12	42	68	101	PA9	I/O	FT	PA9	USART1_TX(7) / TIM1_CH2(7)	-
D11	43	69	102	PA10	I/O	FT	PA10	USART1_RX(7) / TIM1_CH3(7)	-
C12	44	70	103	PA11	I/O	FT	PA11	USART1_CTS / USB_DM / CAN_RX(7) / TIM1_CH4(7)	-
B12	45	71	104	PA12	I/O	FT	PA12	USART1_RTS / USB_DP / CAN_TX(7) / TIM1_ETR(7)	-
A12	46	72	105	PA13	I/O	FT	JTMS-SWDIO	-	PA13
C11	-	73	106	Not connected					
G9	47	74	107	V_{SS_2}	S		V_{SS_2}	-	-
F9	48	75	108	V_{DD_2}	S		V_{DD_2}	-	-
A11	49	76	109	PA14	I/O	FT	JTCK-SWCLK	-	PA14
A10	50	77	110	PA15	I/O	FT	JTDI	SPI3_NSS / I2S3_WS	TIM2_CH1_ETR PA15/ SPI1_NSS
B11	51	78	111	PC10	I/O	FT	PC10	UART4_TX / SDIO_D2	USART3_TX
B10	52	79	112	PC11	I/O	FT	PC11	UART4_RX / SDIO_D3	USART3_RX
C10	53	80	113	PC12	I/O	FT	PC12	UART5_TX / SDIO_CK	USART3_CK
E10	-	81	114	PD0	I/O	FT	PD0	FSMC_D2(9)	CAN_RX
D10	-	82	115	PD1	I/O	FT	PD1	FSMC_D3(9)	CAN_TX
E9	54	83	116	PD2	I/O	FT	PD2	TIM3_ETR / UART5_RX / SDIO_CMD	-
D9	-	84	117	PD3	I/O	FT	PD3	FSMC_CLK	USART2_CTS
C9	-	85	118	PD4	I/O	FT	PD4	FSMC_NOE	USART2_RTS
B9	-	86	119	PD5	I/O	FT	PD5	FSMC_NWE	USART2_TX
E7	-	-	120	V_{SS_10}	S		V_{SS_10}	-	-
F7	-	-	121	V_{DD_10}	S		V_{DD_10}	-	-
A8	-	87	122	PD6	I/O	FT	PD6	FSMC_NWAIT	USART2_RX

5 Electrical characteristics

5.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

5.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3Σ).

5.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 2 V £ V_{DD} £ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2Σ).

5.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

5.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 8*.

5.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 9*.

Figure 8. Pin loading conditions

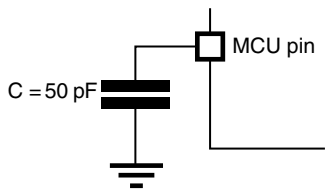
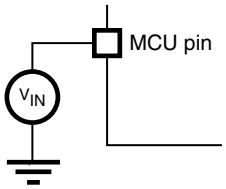
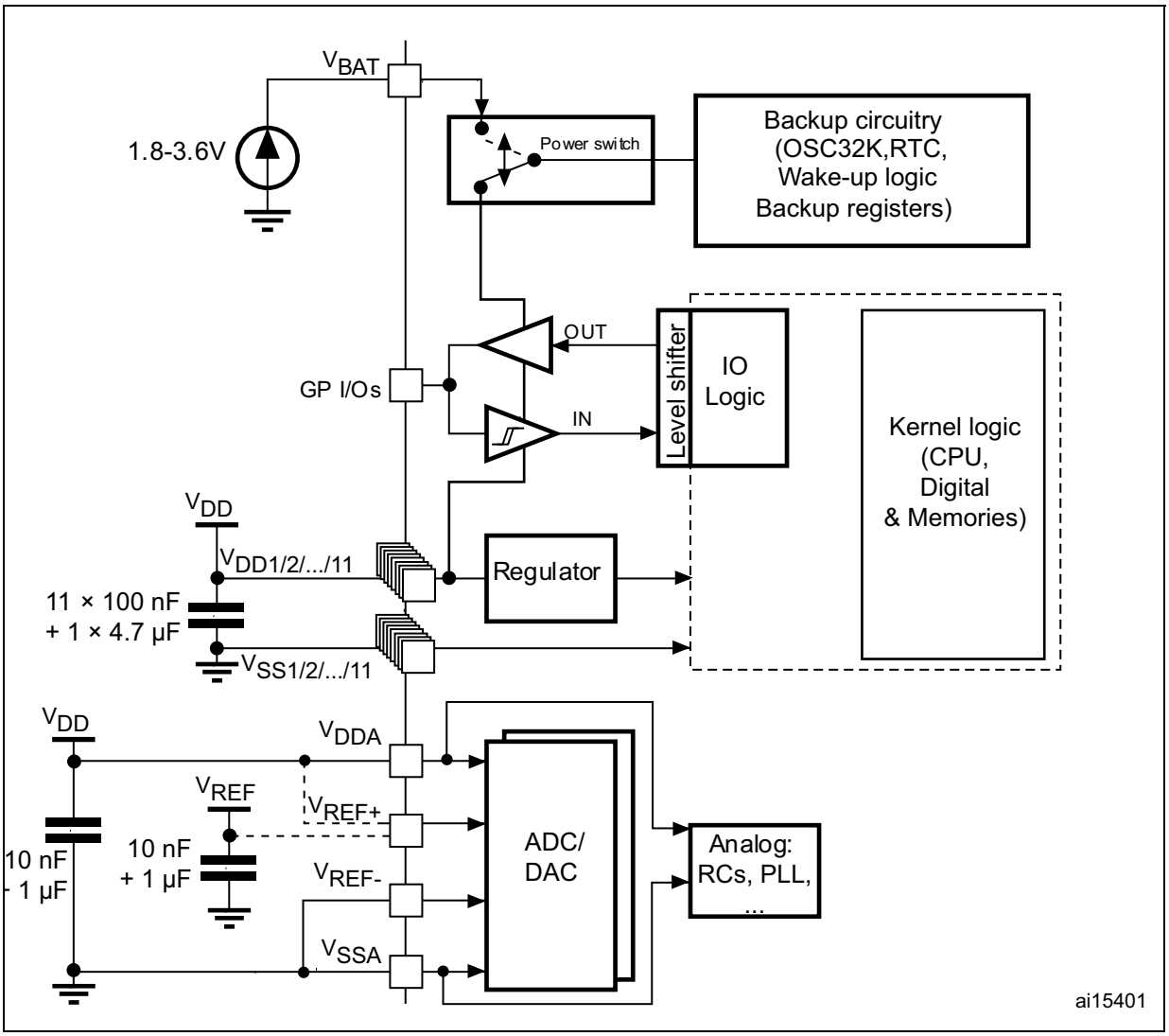


Figure 9. Pin input voltage



5.1.6 Power supply scheme

Figure 10. Power supply scheme



Caution: In *Figure 10*, the 4.7 µF capacitor must be connected to V_{DD3}.

Table 14. Maximum current consumption in Run mode, code with data processing running from Flash

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	68	69	mA
			48 MHz	51	51	
			36 MHz	41	41	
			24 MHz	29	30	
			16 MHz	22	22.5	
			8 MHz	12.5	14	
		External clock(2), all peripherals disabled	72 MHz	39	39	
			48 MHz	29.5	30	
			36 MHz	24	24.5	
			24 MHz	17.5	19	
			16 MHz	14	15	
			8 MHz	8.5	10.5	

1. Guaranteed by characterization results, not tested in production.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Table 15. Maximum current consumption in Run mode, code with data processing running from RAM

Symbol	Parameter	Conditions	f_{HCLK}	Max(1)		Unit
				T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	External clock(2), all peripherals enabled	72 MHz	65	65.5	mA
			48 MHz	46.5	47	
			36 MHz	37	37	
			24 MHz	26.5	27	
			16 MHz	19	20	
			8 MHz	11.5	13	
		External clock(2), all peripherals disabled	72 MHz	34.5	36	
			48 MHz	25	26	
			36 MHz	20.5	21	
			24 MHz	15	16	
			16 MHz	11	13	
			8 MHz	7.5	9	

1. Guaranteed by characterization results, not tested in production at V_{DD} max, f_{HCLK} max.
2. External clock is 8 MHz and PLL is on when f_{HCLK} > 8 MHz.

Figure 12. Typical current consumption in Run mode versus frequency (at 3.6 V) - code with data processing running from RAM, peripherals enabled

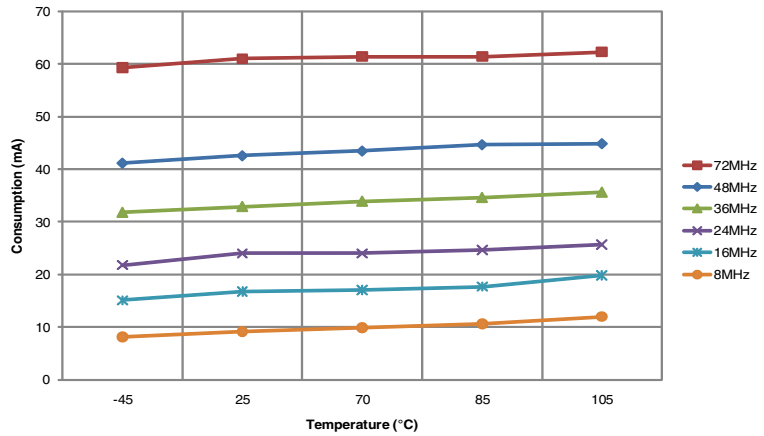
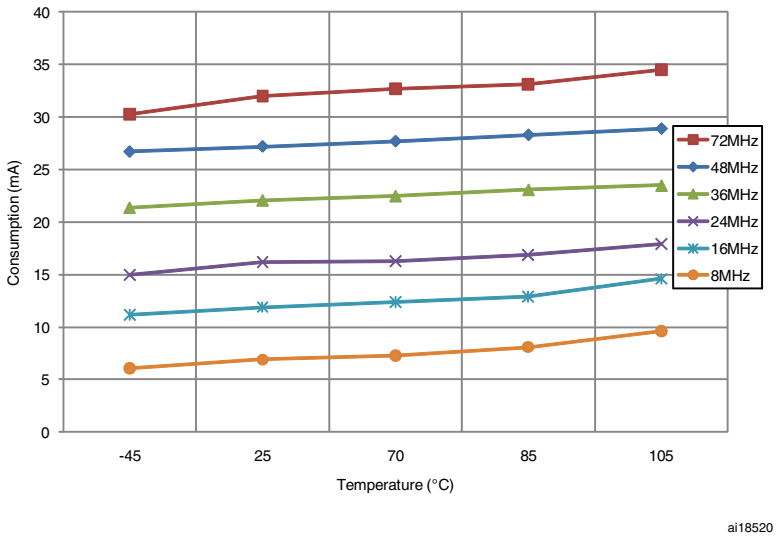


Figure 13. Typical current consumption in Run mode versus frequency (at 3.6 V)- code with data processing running from RAM, peripherals disabled



On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 20*. The MCU is placed under the following conditions:

- all I/O pins are in input mode with a static value at V_{DD} or V_{SS} (no load)
- all peripherals are disabled unless otherwise mentioned
- the given value is calculated by measuring the current consumption
  - with all peripherals clocked off
  - with only one peripheral clocked on
- ambient operating temperature and V_{DD} supply voltage conditions summarized in *Table 7*

Table 20. Peripheral current consumption(1)

Peripheral		Current consumption
AHB (up to 72 MHz)	DMA1	23,06
	DMA2	18,47
	FSMC	55,14
	CRC	2,08
	SDIO	32,22
	BusMatrix(2)	11,67

Figure 24. Asynchronous multiplexed PSRAM/NOR read waveforms

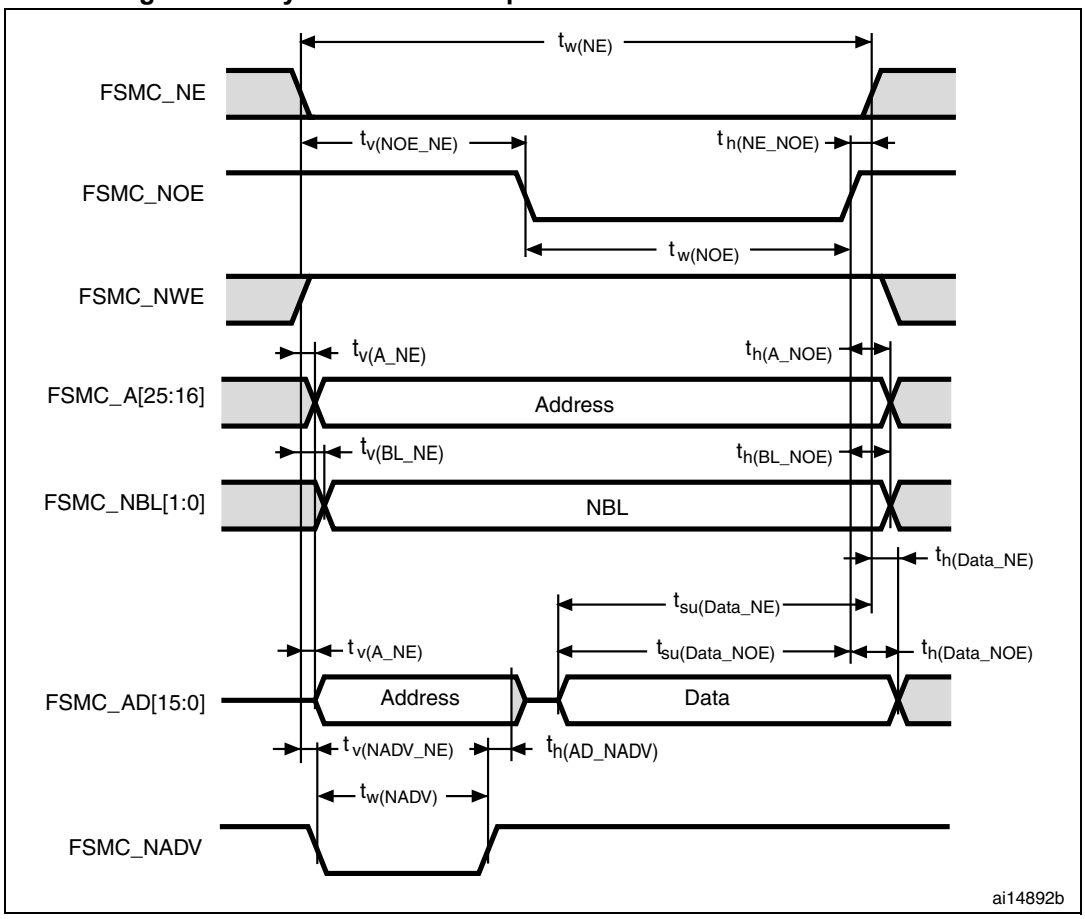


Table 34. Asynchronous multiplexed PSRAM/NOR read timings(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	FSMC_NE low time	$7t_{HCLK}$ + 0.5	$7t_{HCLK}$ + 2	ns
$t_{v(NOE\_NE)}$	FSMC_NEx low to FSMC_NOE low	$3t_{HCLK}$ + 0.5	$3t_{HCLK}$ + 1.5	ns
$t_{w(NOE)}$	FSMC_NOE low time	$4t_{HCLK}$ – 1	$4t_{HCLK}$ + 1	ns
$t_{h(NE\_NOE)}$	FSMC_NOE high to FSMC_NE high hold time	0.5	-	ns
$t_{v(A\_NE)}$	FSMC_NEx low to FSMC_A valid	-	0	ns
$t_{v(NADV\_NE)}$	FSMC_NEx low to FSMC_NADV low	0	1	ns
$t_{w(NADV)}$	FSMC_NADV low time	t_{HCLK} + 0.5	t_{HCLK} + 2	ns
$t_{h(AD\_NADV)}$	FSMC_AD (address) valid hold time after FSMC_NADV high	t_{HCLK}	-	ns
$t_{h(A\_NOE)}$	Address hold time after FSMC_NOE high	t_{HCLK} -2	-	ns
$t_{h(BL\_NOE)}$	FSMC_BL hold time after FSMC_NOE high	0.5	-	ns
$t_{v(BL\_NE)}$	FSMC_NEx low to FSMC_BL valid	-	0	ns
$t_{su(Data\_NE)}$	Data to FSMC_NEx high setup time	$4t_{HCLK}$ - 0.5	-	ns
$t_{su(Data\_NOE)}$	Data to FSMC_NOE high setup time	$4t_{HCLK}$ - 1	-	ns

Figure 26. Synchronous multiplexed NOR/PSRAM read timings

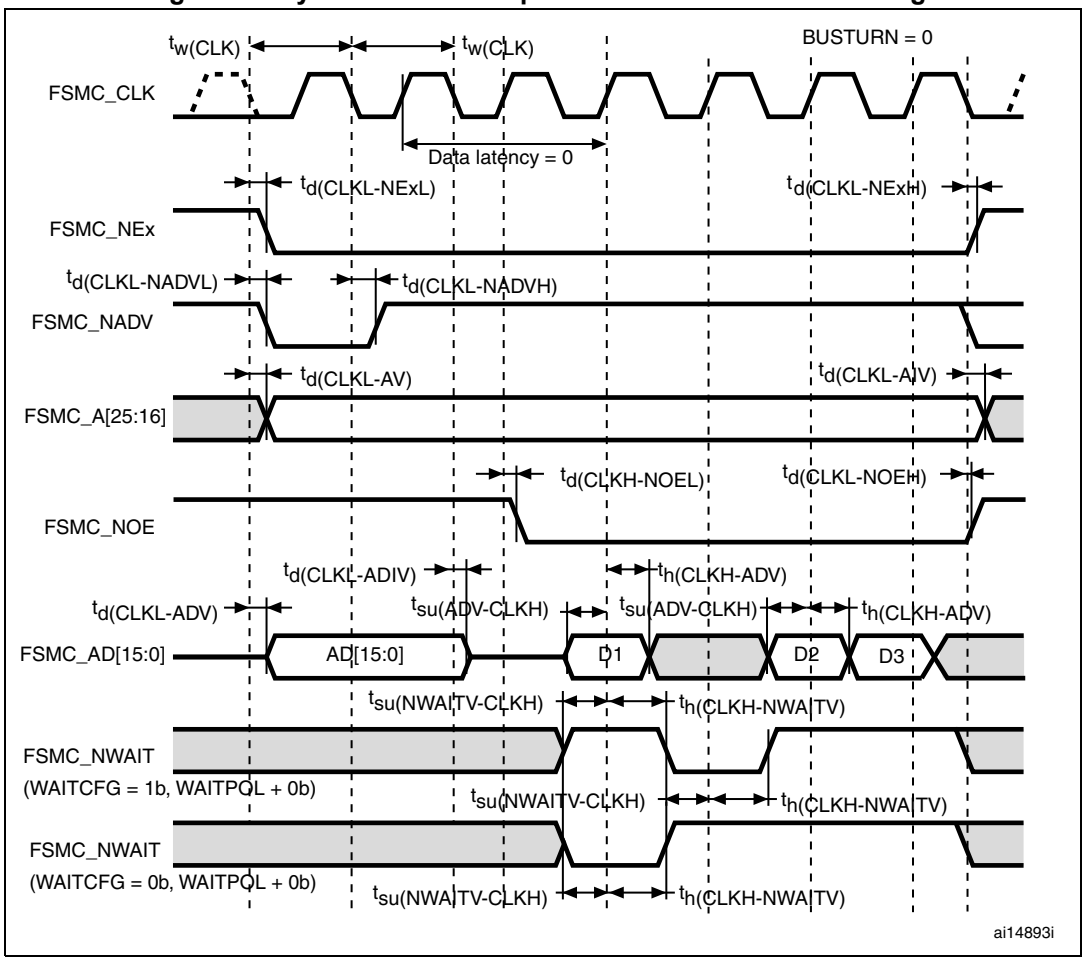
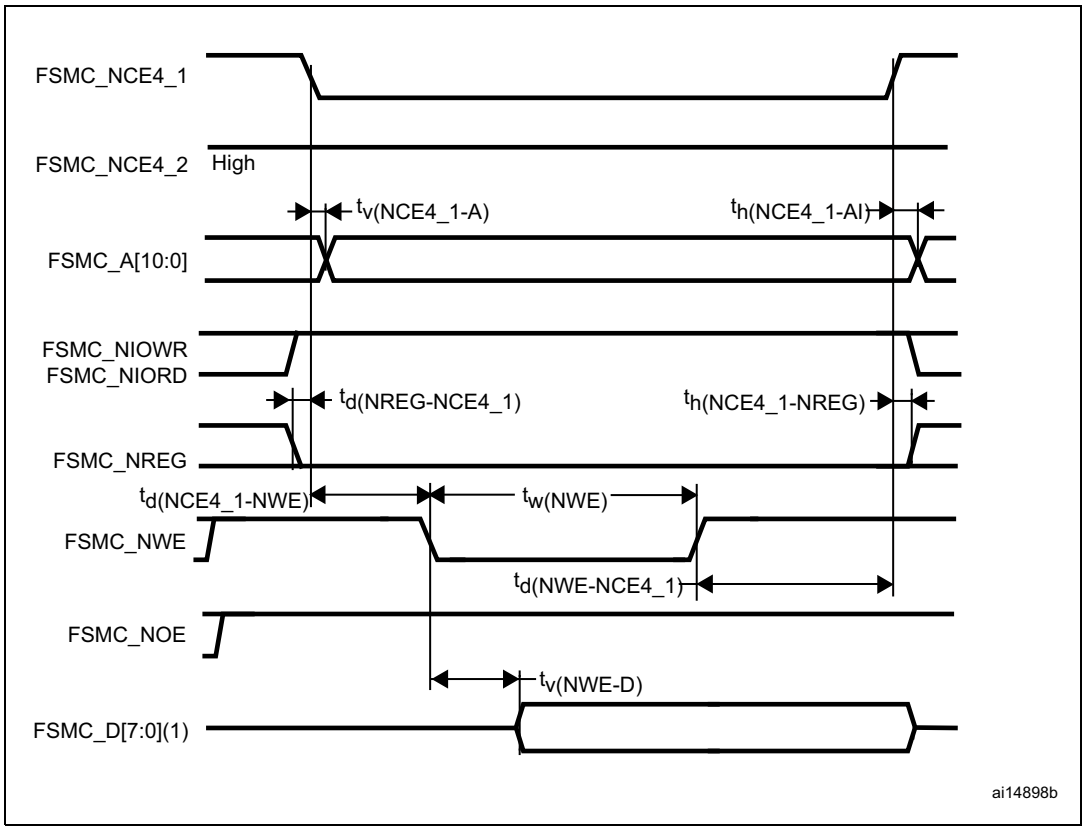


Figure 33. PC Card/CompactFlash controller waveforms for attribute memory write access



1. Only data bits 0...7 are driven (bits 8...15 remains HiZ).

Figure 34. PC Card/CompactFlash controller waveforms for I/O space read access

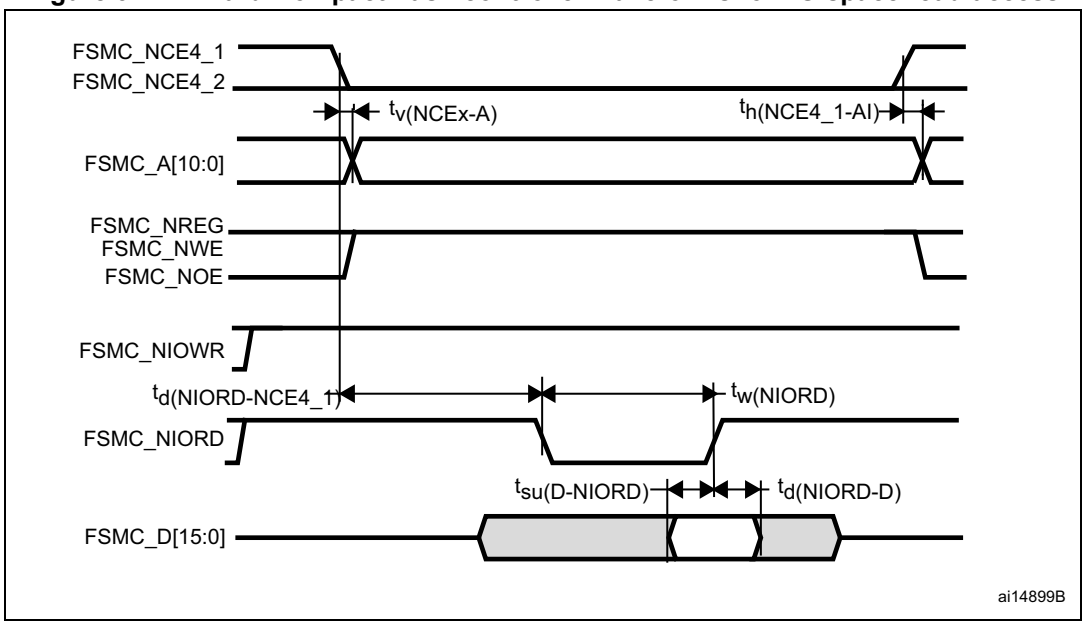


Figure 38. NAND controller waveforms for common memory read access

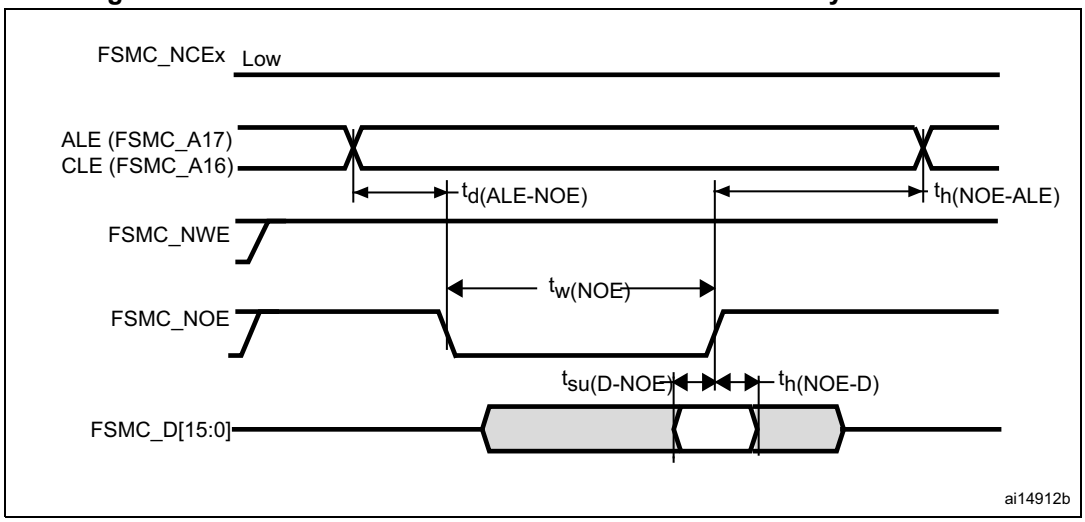


Figure 39. NAND controller waveforms for common memory write access

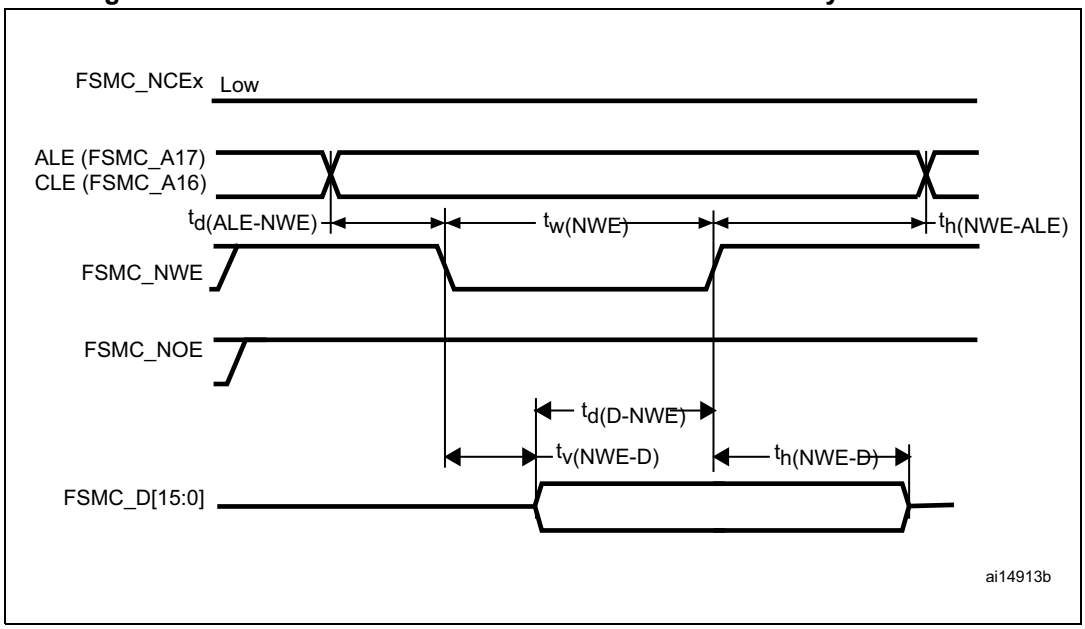
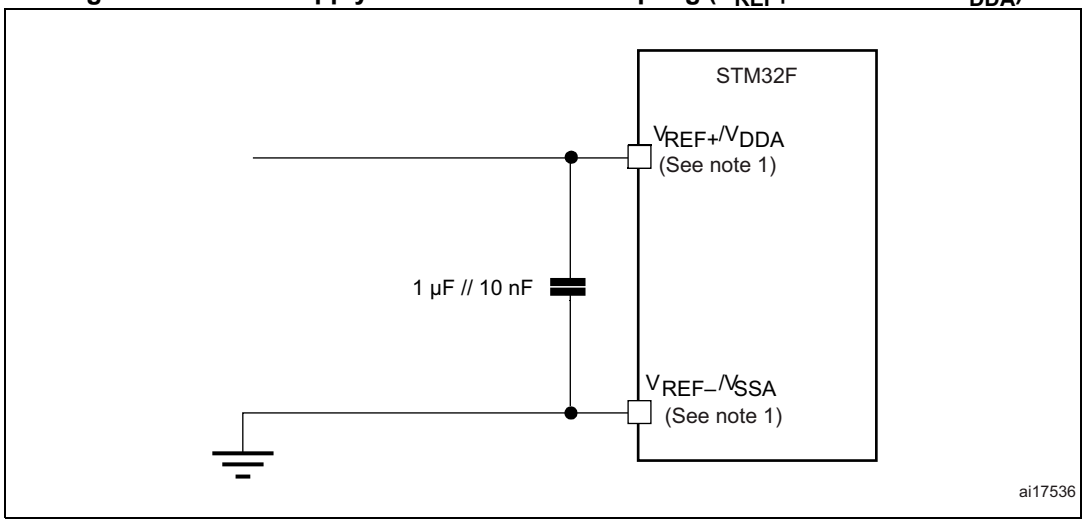


Table 42. Switching characteristics for NAND Flash read cycles(1)

Symbol	Parameter	Min	Max	Unit
$t_{w(NOE)}$	FSMC_NOE low width	$3t_{HCLK} - 1$	$3t_{HCLK} + 1$	ns
$t_{su(D-NOE)}$	FSMC_D[15:0] valid data before FSMC_NOE high	13	-	ns
$t_{h(NOE-D)}$	FSMC_D[15:0] valid data after FSMC_NOE high	0	-	ns
$t_{d(ALE-NOE)}$	FSMC_ALE valid before FSMC_NOE low	-	$2t_{HCLK}$	ns
$t_{h(NOE-ALE)}$	FSMC_NWE high to FSMC_ALE invalid	$2t_{HCLK}$	-	ns

1. C_L = 15 pF.

Figure 58. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})

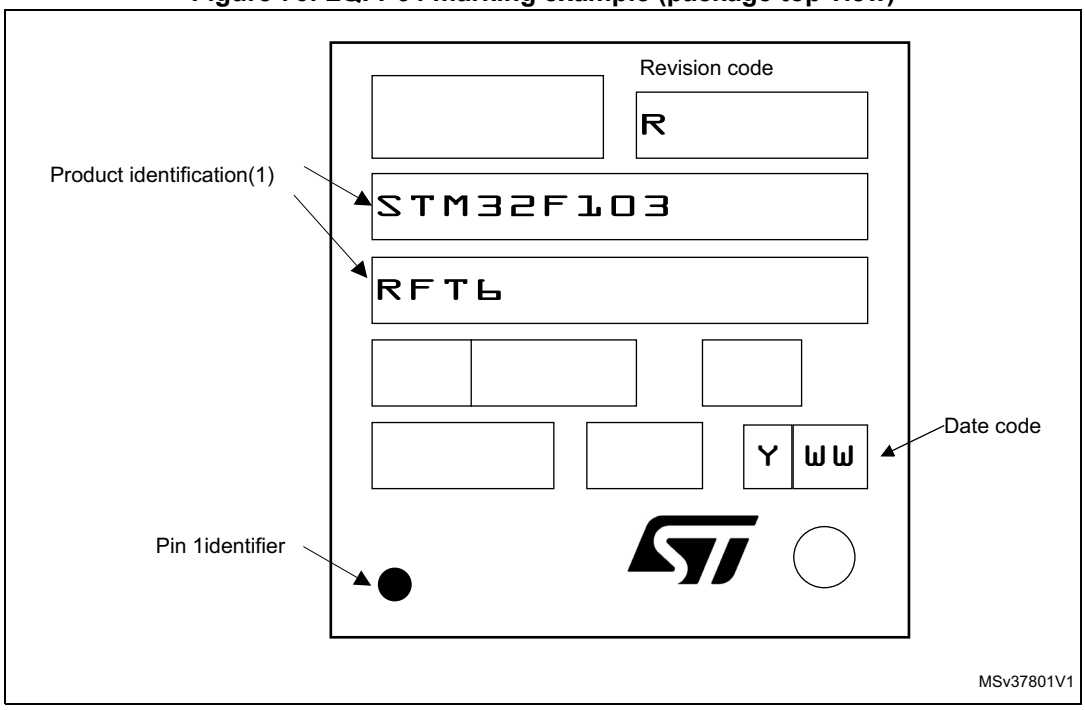


1. V_{REF+} and V_{REF-} inputs are available only on 100-pin packages.

Device marking for LQFP64 package

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 70. LQFP64 marking example (package top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 74. Document revision history

Date	Revision	Changes
18-Jan-2012	3	*Asynchronous waveforms and timings*: added notes about t_{HCLK} clock period and FSMC_BusTurnAroundDuration; updated conditions, modified *Table 31: Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings*, *Table 32: Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings*, *Table 34: Asynchronous multiplexed PSRAM/NOR read timings*, and *Table 35: Asynchronous multiplexed PSRAM/NOR write timings*; added *Table 33: Asynchronous multiplexed read timings*. *Synchronous waveforms and timings*: updated *Figure 27: Synchronous multiplexed PSRAM write timings*; updated *Table 36: Synchronous multiplexed NOR/PSRAM read timings*, *Table 37: Synchronous multiplexed PSRAM write timings*, *Table 38: Synchronous non-multiplexed NOR/PSRAM read timings*, and *Table 39: Synchronous non-multiplexed PSRAM write timings*. *PC Card/CompactFlash controller waveforms and timings*: updated *Figure 35: PC Card/CompactFlash controller waveforms for I/O space write access*; split switching characteristics into *Table 40: Switching characteristics for PC Card/CF read and write cycles in attribute/common space* and *Table 41: Switching characteristics for PC Card/CF read and write cycles in I/O space*, modified values, and removed footnote concerning preliminary values. *NAND controller waveforms and timings*: updated conditions, split switching characteristics into *Table 42: Switching characteristics for NAND Flash read cycles* and *Table 43: Switching characteristics for NAND Flash write cycles*, and values modified. *Section 5.3.14: I/O port characteristics*: updated footnote*1* of *Table 49: I/O static characteristics*; updated *Output driving current*. *Table 50: Output voltage characteristics*: swapped “TTL and “CMOS” ports in the conditions column. *Table 54: I^2C characteristics*: updated footnote *2.* Updated *Table 58: SD / MMC characteristics*. *Table 62: ADC characteristics*: updated footnote *1.* *Table 64: ADC accuracy - limited test conditions*: updated footnote *3.* *Table 67: TS characteristics*: updated footnote *1.*