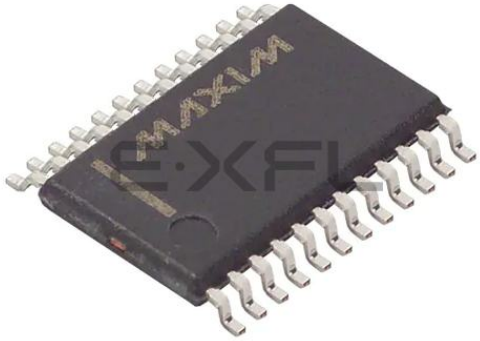

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	3.6MHz
Connectivity	-
Peripherals	LED, Power-Fail Reset, POR, PWM, WDT
Number of I/O	15
Program Memory Size	2KB (1K x 16)
Program Memory Type	EEPROM
EEPROM Size	128 x 8
RAM Size	64 x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	24-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq3212-ejx

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = $V_{DD(MIN)}$ to $V_{DD(MAX)}$, C_{VDD} = 10µF + 0.1µF, T_A = -40¡C to +85¡C. Typical values are at T_A = +25¡C.) (Note 1)

PARAMETER
ANALOG VOLTAGE COMPAR
Input Offset Voltage
Input Common-Mode Voltage
Common-Mode Rejection Ratio
Response Time
Comparator Mode Change to Output Valid
DC Input-Leakage Current
DIGITAL I/O AND OSCILLATO
Input High Voltage: Px.x and HFXIN
Input Low Voltage: Px.x and HFXIN
Output High Voltage: Px.x
Output Low Voltage: Px.x (except P0.7)
Output Low Voltage: P0.7
Input Low Current (All Ports)
Input Low Current (All Ports)
CLOCK SOURCES
External-Clock Frequency
Internal Ring Oscillator
JTAG PROGRAMMING
TCK Frequency
MEMORY CHARACTERISTICS
EEPROM Write/Erase Cycles

Stack Memory

A 16-bit-wide internal stack provides storage for program return addresses and general-purpose use. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced. The PUSH, POP, and POPI instructions can also be used explicitly to store and retrieve data to/from the stack. For the MAXQ3212, the stack is four levels deep.

On reset, the stack pointer, SP, initializes to the top of the stack (03h). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the stack location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at the stack location pointed to by SP, and then decrement SP.

Utility ROM

Table 2. System Register Bit Functions

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									Ñ	Ñ	Ñ	Ñ	AP (4 bits)			
APC									CLR	IDS	Ñ	Ñ	Ñ	MOD2	MOD1	MOD0
PSF									Z	S	Ñ	GPF1	GPF0	OV	C	E
IC									Ñ	Ñ	CGDS	Ñ	Ñ	Ñ	INS	IGE
IMR									IMS	Ñ	Ñ	Ñ	Ñ	Ñ	IM1	IM0
SC									TAP	Ñ	Ñ	Ñ	Ñ	ROD	PWL	Ñ
IIR									IIS	Ñ	Ñ	Ñ	Ñ	Ñ	II1	II0
CKCN									XT/$\overline{RC}$	RGSL	RGMD	STOP	SWB	PMME	CD1	CD0
WDCN									POR	EWDI	Ñ	Ñ	WDIF	WTRF	EWT	RWT
A[n] (0..15)									A[n] (8 bits)							
PFX	PFX (16 bits)															
IP	IP (16 bits)															
SP	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	SP (2 bits)		
IV	IV (16 bits)															
LC[0]	LC[0] (16 bits)															
LC[1]	LC[1] (16 bits)															
Offs									Offs (8 bits)							
DPC	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	Ñ	WBS2	WBS1	WBS0	SDPS1	SDPS0	
GR	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
GRL									GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
BP	BP (16 bits)															
GRS	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
GRH									GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
GRXL	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
BP[offs]	FP (16 bits)															
DP[0]	DP[0] (16 bits)															
DP[1]	DP[1] (16 bits)															

Table 3. System Register Bit Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									0	0	0	0	0	0	0	0
APC									0	0	0	0	0	0	0	0
PSF									1	0	0	0	0	0	0	0
IC									0	0	0	0	0	0	0	0
IMR									0	0	0	0	0	0	0	0
SC									1	0	i	i	i	0	s	0
IIR									0	0	0	0	0	0	0	0
CKCN									s	s	s	0	0	0	0	0
WDCN									s	s	0	0	0	s	s	0
A[n] (0..15)									0	0	0	0	0	0	0	0
PFX	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IP	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
IV	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[0]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[1]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Offs									0	0	0	0	0	0	0	0
DPC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GR	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRL									0	0	0	0	0	0	0	0
BP	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRH									0	0	0	0	0	0	0	0
GRXL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
BP[offs]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Note: *Bits marked with an ÒiÓ have an indeterminate value upon reset. Bits marked with an ÒsÓ have special behavior upon reset. Refer to the MAXQ Family UserÕs Guide: MAXQ3210/MAXQ3212 Supplement for more details.*

Table 4. Peripheral Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)		
	M0 (x0h)	M1 (x1h)	M2 (x2h)
0xh	PO0	CMPC	Ñ
1xh	PO1	Ñ	Ñ
2xh	Ñ	Ñ	Ñ
3xh	Ñ	Ñ	Ñ
4xh	Ñ	T2CNA	Ñ
5xh	Ñ	T2H	Ñ
6xh	Ñ	T2RH	Ñ
7xh	EIE0	T2CH	Ñ
8xh	*PI0*	T2CNB	Ñ
9xh	*PI1*	**T2V**	Ñ
Axh	Ñ	**T2R**	Ñ
Bxh	Ñ	**T2C**	Ñ
Cxh	Ñ	Ñ	Ñ
Dxh	PWCN	Ñ	Ñ
Exh	WUTC	Ñ	Ñ
Fxh	**WUT**	Ñ	Ñ

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)		
	M0 (x0h)	M1 (x1h)	M2 (x2h)
10xh	PD0	T2CFG	Ñ
11xh	PD1	Ñ	Ñ
12xh	Ñ	Ñ	Ñ
13xh	Ñ	Ñ	Ñ
14xh	KEN0	Ñ	Ñ
15xh	KEN1	Ñ	Ñ
16xh	Ñ	Ñ	Ñ
17xh	Ñ	Ñ	Ñ
18xh	Ñ	Ñ	Ñ
19xh	Ñ	Ñ	Ñ
1Axh	Ñ	Ñ	Ñ
1Bxh	ICDF	Ñ	Ñ
1Cxh	Ñ	Ñ	Ñ
1Dxh	Ñ	Ñ	Ñ
1Exh	Ñ	Ñ	Ñ
1Fxh	Ñ	Ñ	Ñ

Note: *Names that appear in italics indicate that all bits of a register are read-only. Names that appear in bold indicate that a regi ster is 16 bits wide.*

Microcontroller with Analog Comparator and LED Driver

Table 5. Peripheral Register Bit Functions

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0									PO0.7	PO0.6	PO0.5	PO0.4	PO0.3	PO0.2	PO0.1	PO0.0
PO1									Ñ	PO1.6	PO1.5	PO1.4	PO1.3	PO1.2	PO1.1	PO1.0
EI0									Ñ	Ñ	Ñ	Ñ	Ñ	IT0	EX0	IE0
PI0									PI0.7	PI0.6	PI0.5	PI0.4	PI0.3	PI0.2	PI0.1	PI0.0
PI1									Ñ	PI1.6	PI1.5	PI1.4	PI1.3	PI1.2	PI1.1	PI1.0
PWCN									Ñ	Ñ	RSTD	REFO	LBF	LBIE	LBDE	BOD
WUTC									Ñ	Ñ	Ñ	Ñ	XTE	WTCS	WTF	WTE
WUT	WT19	WT18	WT17	WT16	WT15	WT14	WT13	WT12	WT11	WT10	WT9	WT8	WT7	WT6	WT5	WT4
PD0									PD0.7	PD0.6	PD0.5	PD0.4	PD0.3	PD0.2	PD0.1	PD0.0
PD1									Ñ	PD1.6	PD1.5	PD1.4	PD1.3	PD1.2	PD1.1	PD1.0
KEN0									KEN0.7	KEN0.6	KEN0.5	KEN0.4	KEN0.3	KEN0.2	KEN0.1	KEN0.0
KEN1									Ñ	KEN1.6	KEN1.5	KEN1.4	KEN1.3	KEN1.2	KEN1.1	KEN1.0
ICDF									Ñ	Ñ	Ñ	Ñ	PSS1	PSS0	SPE	TXC
CMPC									CMON	ECMF	CMF	CMM	ECMO	CMO	CPOL	EXRF
T2CNA									ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
T2H									T2V.15	T2V.14	T2V.13	T2V.12	T2V.11	T2V.10	T2V.9	T2V.8
T2RH									T2R.15	T2R.14	T2R.13	T2R.12	T2R.11	T2R.10	T2R.9	T2R.8
T2CH									T2C.15	T2C.14	T2C.13	T2C.12	T2C.11	T2C.10	T2C.9	T2C.8
T2CNB									ET2L	T2OE1	T2POL1	TR2L	TF2	TCC2	TF2L	TC2L
T2V	T2V.15	T2V.14	T2V.13	T2V.12	T2V.11	T2V.10	T2V.9	T2V.8	T2V.7	T2V.6	T2V.5	T2V.4	T2V.3	T2V.2	T2V.1	T2V.0
T2R	T2R.15	T2R.14	T2R.13	T2R.12	T2R.11	T2R.10	T2R.9	T2R.8	T2R.7	T2R.6	T2R.5	T2R.4	T2R.3	T2R.2	T2R.1	T2R.0
T2C	T2C.15	T2C.14	T2C.13	T2C.12	T2C.11	T2C.10	T2C.9	T2C.8	T2C.7	T2C.6	T2C.5	T2C.4	T2C.3	T2C.2	T2C.1	T2C.0
T2CFG									Ñ	DIV2	DIV1	DIV0	T2MD	CCF1	CCF0	C/T2

Table 6. Peripheral Register Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0									1	1	1	1	1	1	1	1
PO1									0	1	1	1	1	1	1	1
EI0									0	0	0	0	0	0	0	0
PI0									s	s	s	s	s	s	s	s
PI1									0	s	s	s	s	s	s	s
PWCN									0	0	s	s	s	0	0	s
WUTC									0	0	0	0	0	0	0	0
WUT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PD0									0	0	0	0	0	0	0	0
PD1									0	0	0	0	0	0	0	0
KEN0									0	0	0	0	0	0	0	0
KEN1									0	0	0	0	0	0	0	0
ICDF									0	0	0	0	s	s	s	0
CMPC									0	0	1	0	0	0	0	0
T2CNA									0	0	0	0	0	0	0	0
T2H									0	0	0	0	0	0	0	0
T2RH									0	0	0	0	0	0	0	0
T2CH									0	0	0	0	0	0	0	0
T2CNB									0	0	0	0	0	0	0	0
T2V	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG									0	0	0	0	0	0	0	0

Power Management

Advanced power-management features minimize power consumption by dynamically matching the processing speed of the device to the required performance level. This means device operation can be slowed and power consumption minimized during periods of reduced activity. When more processing power is required, the microcontroller can increase its operating frequency. Software-selectable clock-divide operations allow flexibility, selecting whether a system clock cycle (SYSCLK) is 1, 2, 4, or 8 oscillator cycles. By performing this function in software, a lower power state can be entered without the cost of additional hardware.

For extremely power-sensitive applications, additional low-power modes are available.

- ¥ Divide-by-256 power-management mode (PMM) (PMME = 1, CD1:0 = 00b)
- ¥ Stop mode (STOP = 1)

In PMM, one system clock is 256 oscillator cycles, significantly reducing power consumption while the microcontroller functions at reduced speed. The optional switchback feature allows enabled interrupt sources including external interrupts to quickly exit the power-management modes and return to a faster internal clock rate.

Power consumption reaches its minimum in stop mode. In this mode the external oscillator, system clock, and all processing activity is halted. Stop mode is exited when an enabled external interrupt pin is triggered, the enabled wake-up timer expires, or an external reset signal is applied to the $\overline{\text{RESET}}$ pin. Upon exiting stop mode, the microcontroller starts execution immediately from its internal 8kHz (approximately) ring oscillator while the warmup period completes.

Interrupts

Multiple reset sources are available for quick response to internal and external events. The MAXQ architecture uses a single interrupt vector (IV), single interrupt-service routine (ISR) design. For maximum flexibility, interrupts can be enabled globally, individually, or by module. When an interrupt condition occurs, its individual flag is set, even if the interrupt source is disabled at the local, module, or global level. Interrupt flags must be cleared within the user-interrupt routine to avoid repeated interrupts from the same source. Application software must ensure a delay between the write to the flag and the RETI instruction to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, software jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up, so if it is not changed to a different address, the user program must determine whether a jump to 0000h came from a reset or interrupt source.

Once software control has been transferred to the ISR, the interrupt identification register (IIR) can be used to determine if a system register or peripheral register was the source of the interrupt. The specified module can then be interrogated for the specific interrupt source and software can take appropriate action. Because the interrupts are evaluated by user software, the user can define a unique interrupt priority scheme for each application. The following interrupt sources are available.

- ¥ Watchdog Interrupt
- ¥ External Interrupt 0
- ¥ Timer 2 Low Compare, Low Overflow, Capture/Compare, and Overflow Interrupts
- ¥ Analog Comparator Interrupt
- ¥ Wake-Up Interrupt

Reset Sources

Several reset sources are provided for microcontroller control. Although code execution is halted in the reset state, the high-frequency oscillator and the ring oscillator continue to oscillate.

Power-On Reset/Brownout Reset

An internal power-on reset circuit enhances system reliability. This circuit forces the device to perform a power-on reset whenever a rising voltage on V_{DD} climbs above approximately V_{RST}. Additionally, the device performs a brownout reset whenever V_{DD} drops below V_{RST}, a feature that can be optionally disabled in stop mode. The following events occur during a power-on reset.

- ¥ All registers and circuits enter their power-on reset state
- ¥ I/O pins revert to their reset state, with logic-1 states tracking V_{DD}
- ¥ The power-on reset flag is set to indicate the source of the reset
- ¥ The ring oscillator becomes the clock source
- ¥ The external high-speed oscillator begins its warmup
- ¥ Code execution begins at location 8000h

Microcontroller with Analog Comparator and LED Driver

Watchdog Timer Reset

The watchdog timer functions are described in the *MAXQ Family UserÕs Guide*Software can determine if a reset is caused by a watchdog timeout by checking the Watchdog Timer Reset Flag (WTRF) in the WDCN register. Execution resumes at location 8000h following a watchdog timer reset.

External System Reset

Asserting the external $\overline{\text{RESET}}$ pin low causes the device to enter the reset state. The external reset functions as described in the *MAXQ Family UserÕs Guide* Execution resumes at location 8000h after the $\overline{\text{RESET}}$ pin is released. The external system reset function is enabled by default on a power-on reset, but can be disabled and the pin used as general-purpose I/O by setting the Reset Pin Disable (RSTD) bit. The system designer is cautioned not to disable the reset pin early in the software as it could disable future JTAG access and/or bootloader capability.

I/O Ports

The microcontroller uses a form of Type D bidirectional I/O pins described in the *MAXQ Family UserÕs Guide* Each port has eight independent, general-purpose I/O pins and three configure/control registers. Many pins support alternate functions such as timers or interrupts, which are enabled, controlled, and monitored by dedicated peripheral registers. Using the alternate function automatically converts the pin to that function. The I/O pins on this device employ an optional ÒkeeperÓ latch that helps to maintain the input pin state in the absence of external drive sources.

Port 0.7 is a special pin with a stronger pulldown capability to drive devices such as LEDs. It operates and is configured the same as other pins.

Type D port pins have Schmitt Trigger receivers and full CMOS output drivers, and can support special functions. The pin is either tri-stated or weak pullup when defined as an input, dependent on the state of the corresponding bit in the output register. One pin of the device has interrupt capability.

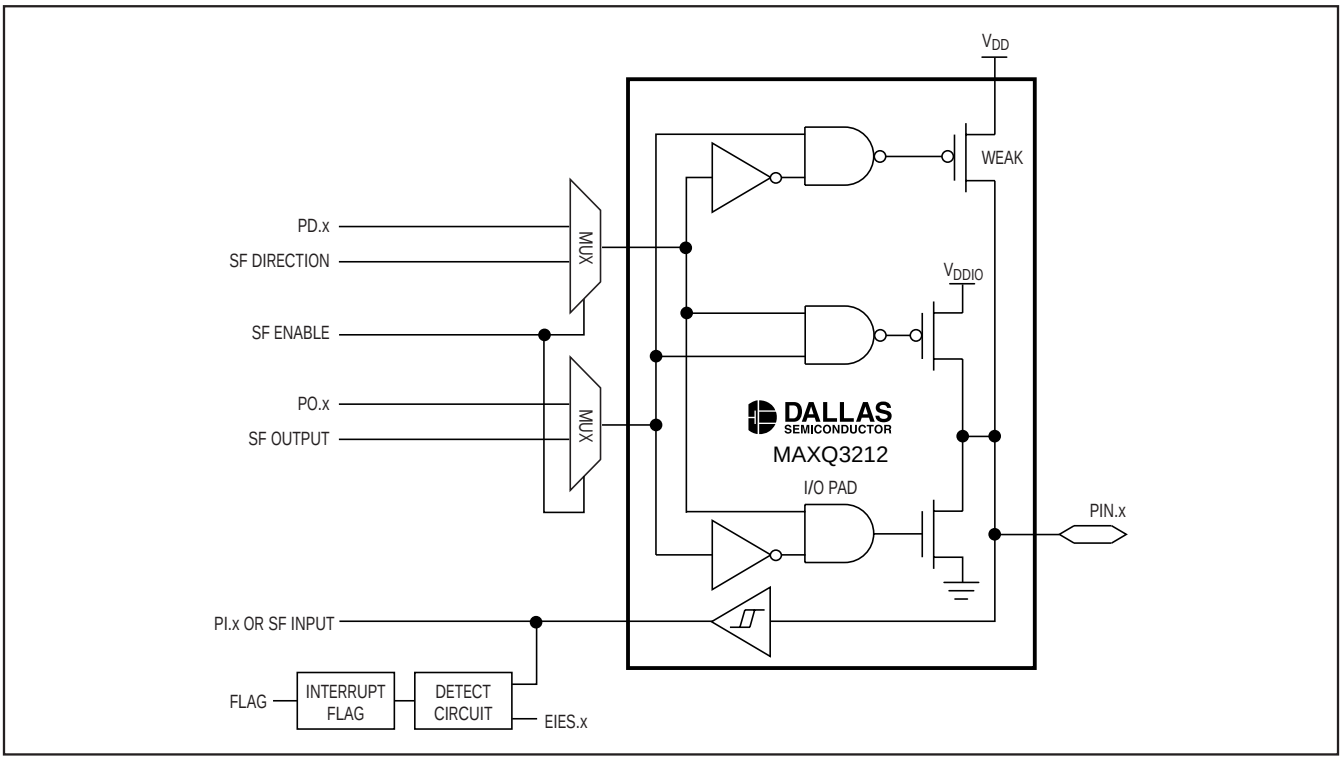


Figure 3. Type D Port Pin Schematic

Programmable Timer

The microcontroller incorporates one 16-bit programmable timer/counter. The type 2 timer (timer 2) can be used in counter/timer/capture/compare/PWM functions, allowing precise control of internal and external events. It also supports optional single-shot, external gating, and polarity control options.

Timer 2

The timer 2 peripheral includes the following:

- ¥ 16-bit auto-reload timer/counter
- ¥ 16-bit capture
- ¥ 16-bit counter
- ¥ 8-bit capture and 8-bit timer
- ¥ 8-bit counter and 8-bit timer

Wake-Up Timer

The microcontroller includes a simple 20-bit wake-up timer that can be used to measure long intervals. The user-selectable timer period can be used to generate a long-period interrupt or wake the device out of stop mode. The timer can be clocked from either the currently active system clock or the 8kHz ring oscillator. In stop mode, only the 8kHz ring oscillator is available as the wake-up timer clock source. As an interrupt, the feature increases overall performance by reducing many shorter timer interruptions to a single interrupt to measure the same long period. When used in stop mode, it provides the energy savings of the lowest power mode with periodic wake-up ability.

Watchdog Timer

An internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer is controlled through bits in the WDCN register. Its timeout period can be set to one of four programmable intervals ranging from 2^{12} to 2^{21} system clocks in its default clock mode, allowing flexibility to support different types of applications. The interrupt occurs 512 system clocks before the reset, allowing the system to execute an interrupt and place the system in a known, safe state before the device performs a total system reset. At 3.58MHz, watchdog timeout periods can be programmed from 1.14ms to 149.94s, depending on the system clock mode.

Analog Comparator

The analog comparator is a 1-bit, analog-to-digital comparator. The comparator input can be connected to a wide range of peripherals, including chemical sensors and motion or proximity detectors, or any other appropriate analog input. The comparator measures the analog input against either an external voltage reference or the internal +2.5V reference. When the level on the comparator input, CMPI, rises above the selected voltage reference, the CMO bit in the CMPC register is changed to the desired level. The device then responds by asserting an external signal and/or activating an internal interrupt request. The polarity of the external signal asserted is programmable. When not in use, the pins associated with the comparator are usable as general-purpose I/O.

In addition, the +2.5V reference is configurable to be output on the V_{REF} pin. This provides an absolute voltage reference for use with data converters or other precision devices.

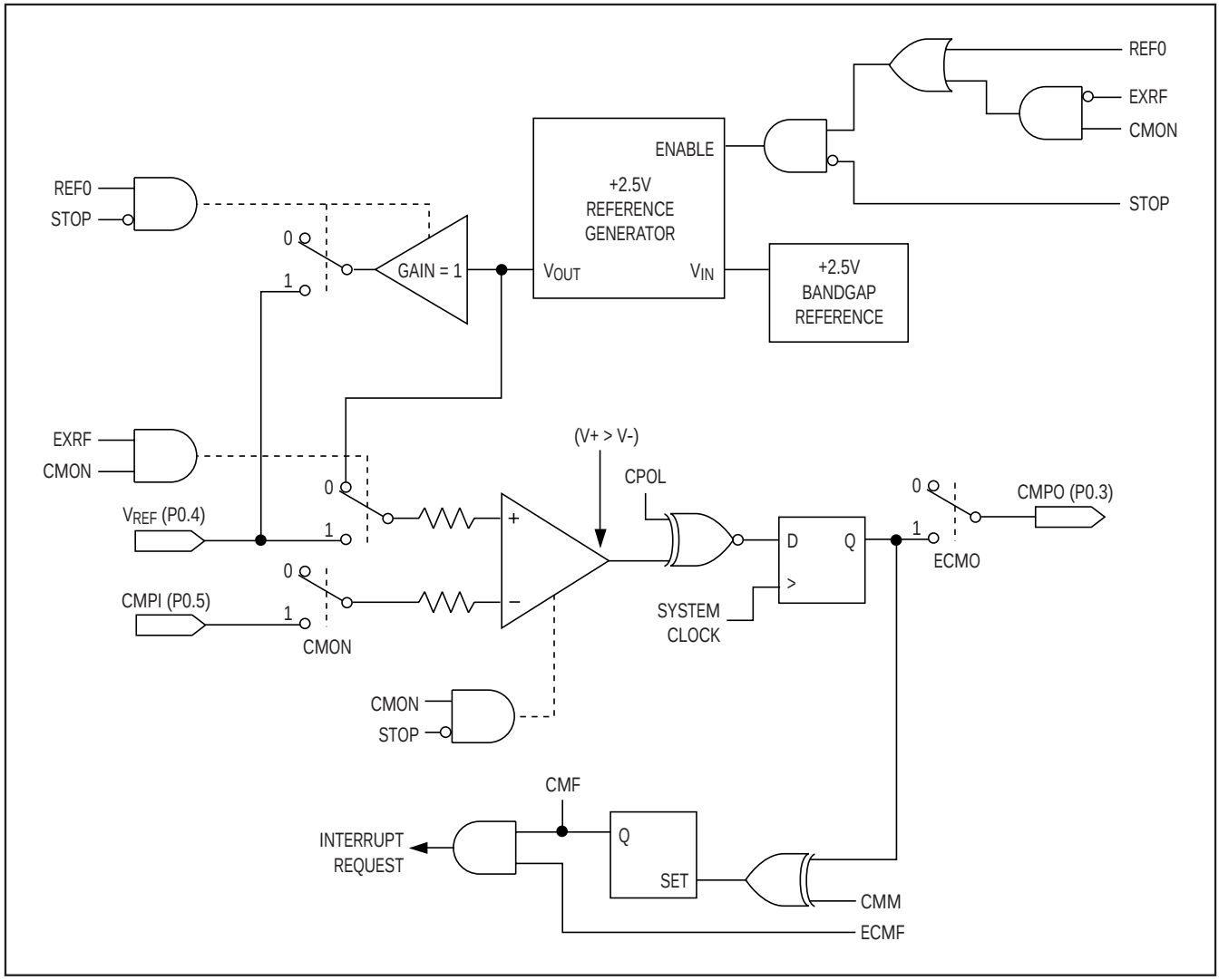


Figure 4. MAXQ3212 Analog Comparator

In-Circuit Debug

Embedded debugging capability is available through the JTAG-compatible Test Access Port. Embedded debug hardware and embedded ROM firmware provide in-circuit debugging capability to the user application, eliminating the need for an expensive in-circuit emulator. Figure 5 shows a block diagram of the in-circuit debugger. The in-circuit debug features include:

- ¥ Hardware debug engine
- ¥ Set of registers able to set breakpoints on register, code, or data accesses
- ¥ Set of debug service routines stored in the utility ROM

The embedded hardware debug engine is an independent hardware block in the microcontroller. The debug engine can monitor internal activities and interact with selected internal registers while the CPU is executing user code. Collectively, the hardware and software features allow two basic modes of in-circuit debugging:

- ¥ Background mode allows the host to configure and set up the in-circuit debugger while the CPU continues to execute the application software at full speed. Debug mode can be invoked from background mode.
- ¥ Debug mode allows the debug engine to take control of the CPU, providing read/write access to internal registers and memory, and single-step trace operation.

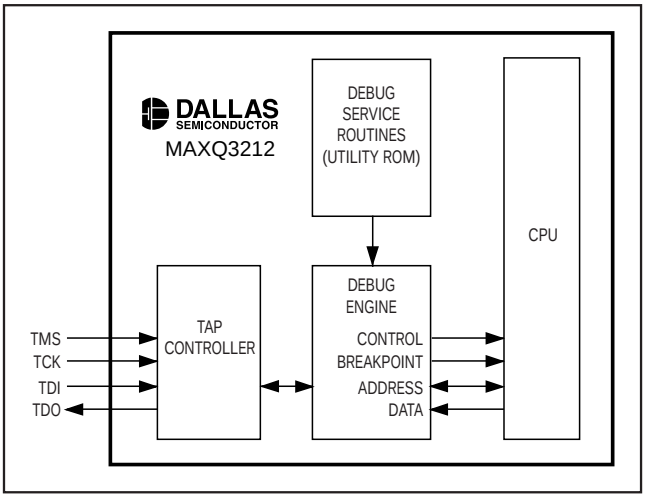


Figure 5. In-Circuit Debugger

Applications Information

Grounds and Bypassing

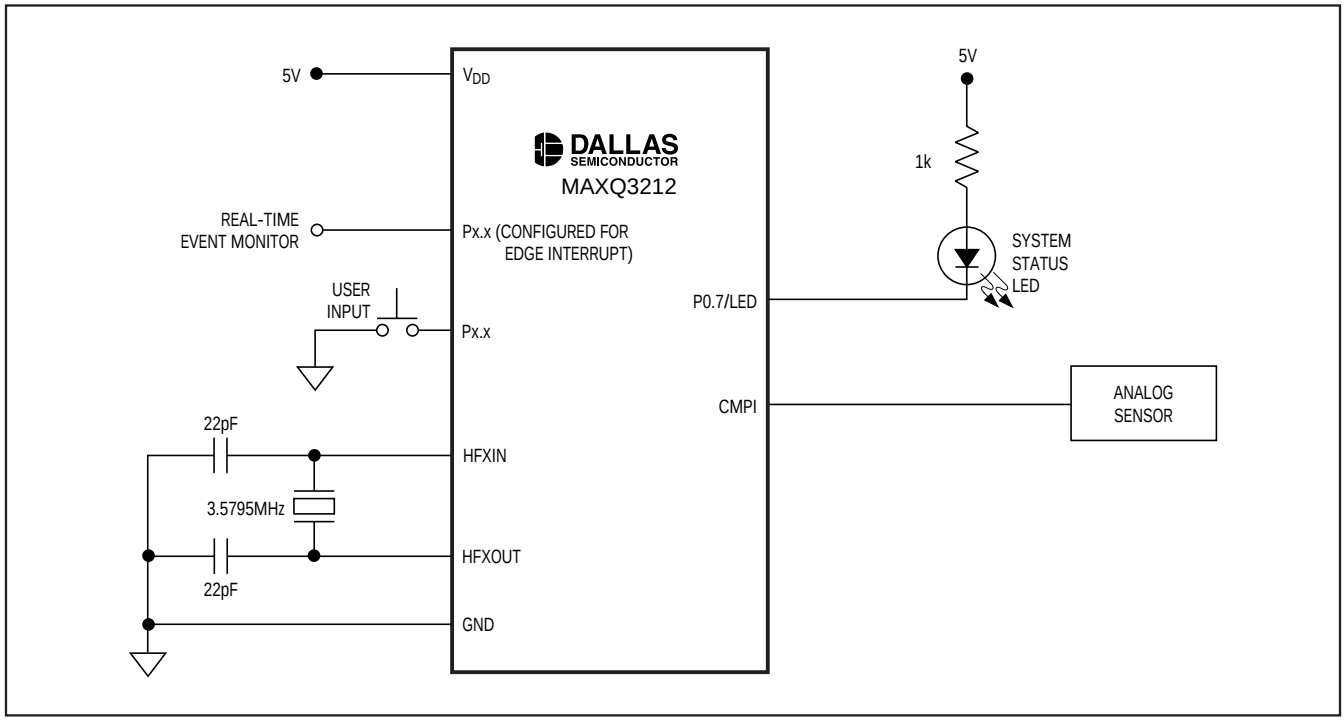
Careful PC board layout significantly minimizes crosstalk among the reference input, comparator outputs, and digital inputs. Keep digital and analog lines separate, and use ground traces as shields between them where possible. Separate CMPI and V_{REF} from each other by running a ground trace between these pins. Bypass V_{DD} with a capacitor as low as 1µF and keep bypass capacitor leads short for best noise rejection.

Applications

The low-power, high-performance RISC architecture of the MAXQ3212 makes it an excellent fit for many portable or battery-powered applications that require cost-effective computing. The analog comparator can function as an analog-to-digital converter (ADC) when simple analog measurements are necessary, and the high-current I/O pin can drive a power or status LED.

This device can also be used as a low-cost ADC. The single-slope conversion method can be easily implemented using the internal comparator and an internal timer. The basic implementation of such a converter is illustrated below. One of the benefits of this approach is the small number of external components required: the transistor creates a constant current source, a ramp capacitor times the conversion, and a resistor and capacitor on the comparator input acting as a simple filter. The result is the addition of A/D capability to the end system at virtually no additional cost.

Typical Operating Circuit



Ordering Information

PART	TEMP RANGE	NOMINAL V_{DD} (V)	MEMORY	PIN-PACKAGE
MAXQ3212-EJX	-40¡C to +85¡C	5	1kWord EEPROM	24 TSSOP
MAXQ3212-EJX+	-40¡C to +85¡C	5	1kWord EEPROM	24 TSSOP
MAXQ3212-EMX	-40¡C to +85¡C	5	1kWord EEPROM	24 PDIP
MAXQ3212-EMX+	-40¡C to +85¡C	5	1kWord EEPROM	24 PDIP

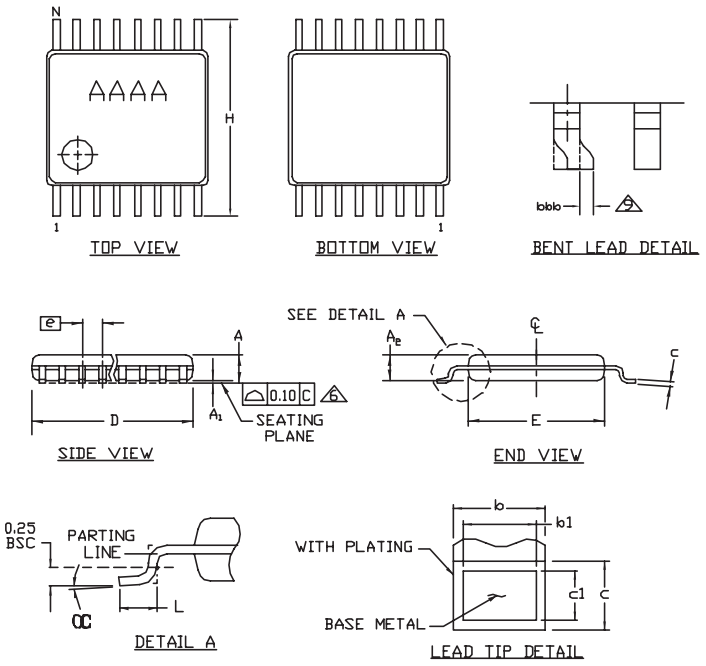
+Denotes a Pb-free/RoHS-compliant package.

Microcontroller with Analog Comparator and LED Driver

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline info rmation go to **www.maxim-ic.com/packages**.)

TSSOP4.40mm.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	——	1.10		.043
A_1	0.05	0.15	.002	.006
A_2	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b_1	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c_1	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	0.10 MAX			

JEDEC MO-153	N		PKG. CODES	VARIATIONS			
				MILLIMETERS		INCHES	
				MIN.	MAX.	MIN.	MAX.
AB-1	14	D	U14-1; U14-2	4.90	5.10	.193	.201
AB	16	D	U16-1; U16-2	4.90	5.10	.193	.201
AC	20	D	U20-2; U20-3	6.40	6.60	.252	.260
AD	24	D	U24-1	7.70	7.90	.303	.311
AE	28	D	U28-1; U28-2; U28-3	9.60	9.80	.378	.386

NOTES
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS
6. LEAD COPLANARITY 0.10 MM MAX.
7. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY
9. BENT LEAD 0.10 MM MAX.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

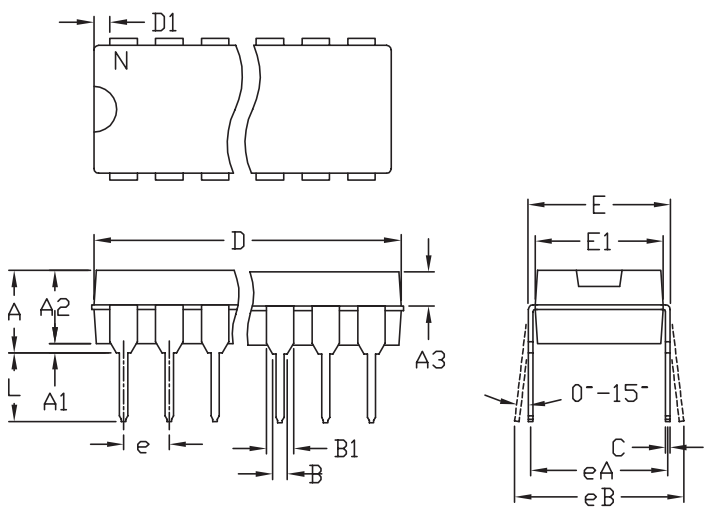
TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0066	I	1/1

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline info rmation go to **www.maxim-ic.com/packages**.)

PDIPN.EPS



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.180	---	4.572
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.015	0.022	0.381	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.014	0.2	0.355
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100 BSC.		2.54 BSC.	
eA	0.300 BSC.		7.62 BSC.	
eB	0.400 BSC.		10.16 BSC.	
L	0.115	0.150	2.921	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	*5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION | PACKAGE FAMILY OUTLINE: PDIP .300" (TITLE) | 1/1 | 21-0043 D (DOCUMENT CONTROL NUMBER) REV

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