AMD Xilinx - XC2S100-5FG256I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

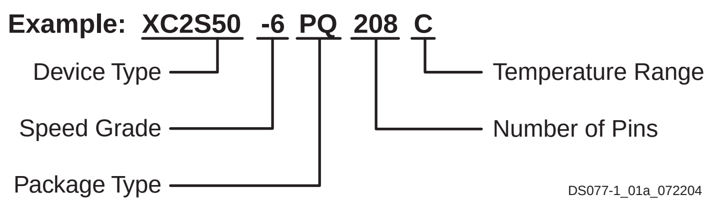
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	40960
Number of I/O	176
Number of Gates	100000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s100-5fg256i

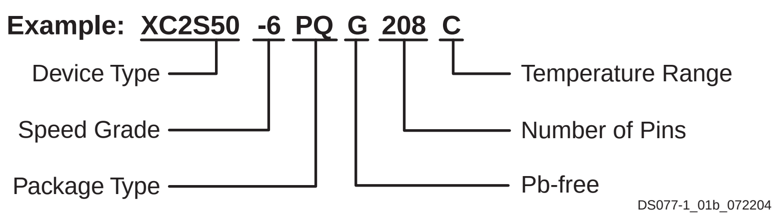
Ordering Information

Spartan-II devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

Standard Packaging



Pb-Free Packaging



Device Ordering Options

Device
XC2S15
XC2S30
XC2S50
XC2S100
XC2S150
XC2S200

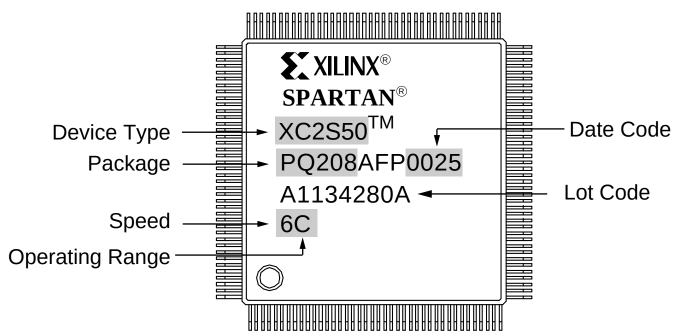
Speed Grade	
-5	Standard Performance
-6	Higher Performance(1)

Number of Pins / Package Type	
VQ(G)100	100-pin Plastic Very Thin QFP
CS(G)144	144-ball Chip-Scale BGA
TQ(G)144	144-pin Plastic Thin QFP
PQ(G)208	208-pin Plastic QFP
FG(G)256	256-ball Fine Pitch BGA
FG(G)456	456-ball Fine Pitch BGA

Temperature Range (T_J)	
C = Commercial	0°C to +85°C
I = Industrial	–40°C to +100°C

Notes:
1. The -6 speed grade is exclusively available in the Commercial temperature range.

Device Part Marking



Sample package with part marking for XC2S50-6PQ208C.

ds001-1_02_090303

Spartan-II FPGA Family: Functional Description

DS001-2 (v2.8) June 13, 2008

Product Specification

Architectural Description

Spartan-II FPGA Array

The Spartan®-II field-programmable gate array, shown in Figure 2, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 2, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

Input/Output Block

The Spartan-II FPGA IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. Table 3 lists several of the standards which are supported along with the required reference, output and termination voltages needed to meet the standard.

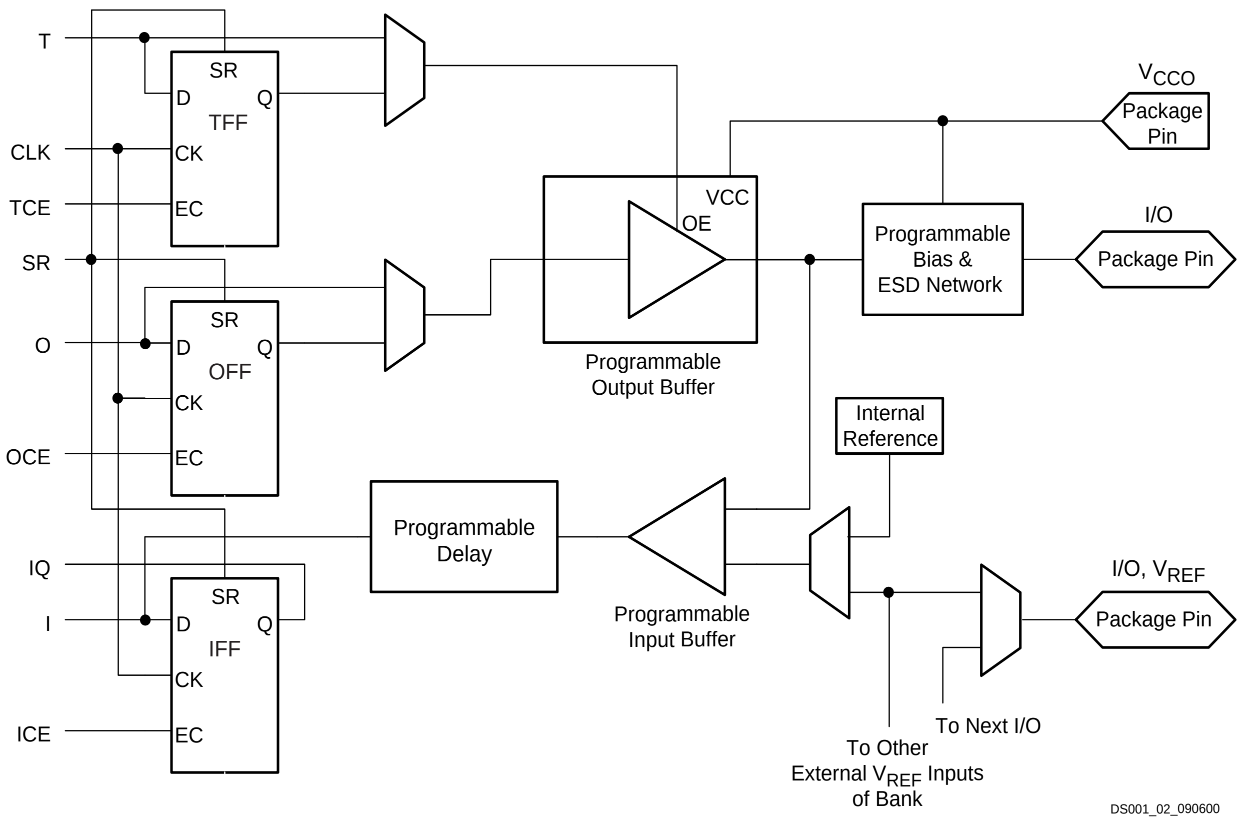


Figure 2: **Spartan-II FPGA Input/Output Block (IOB)**

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drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage is determined by the output standards in use.

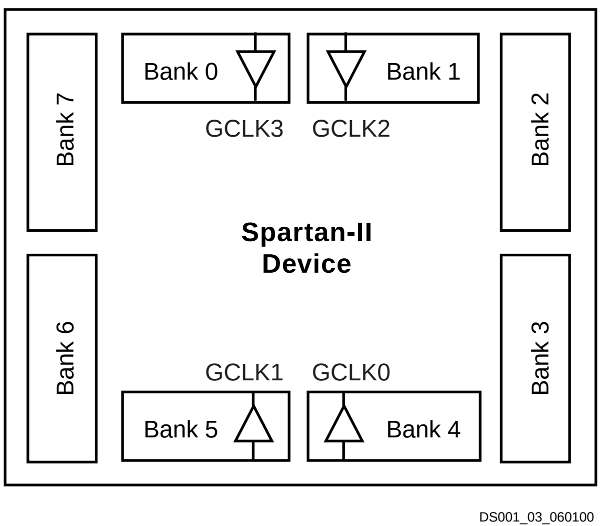


Figure 3: **Spartan-II I/O Banks**

Within a bank, output standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 4: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. About one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

In a bank, inputs requiring V_{REF} can be mixed with those that do not but only one V_{REF} voltage may be used within a bank. Input buffers that use V_{REF} are not 5V tolerant. LVTTL, LVCMOS2, and PCI are 5V tolerant. The V_{CCO} and V_{REF} pins for each bank appear in the device pinout tables.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device. All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

Independent Banks Available

Package	VQ100 PQ208	CS144 TQ144	FG256 FG456
Independent Banks	1	4	8

Configurable Logic Block

The basic building block of the Spartan-II FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. Output from the function generator in each LC drives the CLB output and the D input of the flip-flop. Each Spartan-II FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 4.

In addition to the four basic LCs, the Spartan-II FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

Look-Up Tables

Spartan-II FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-II FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

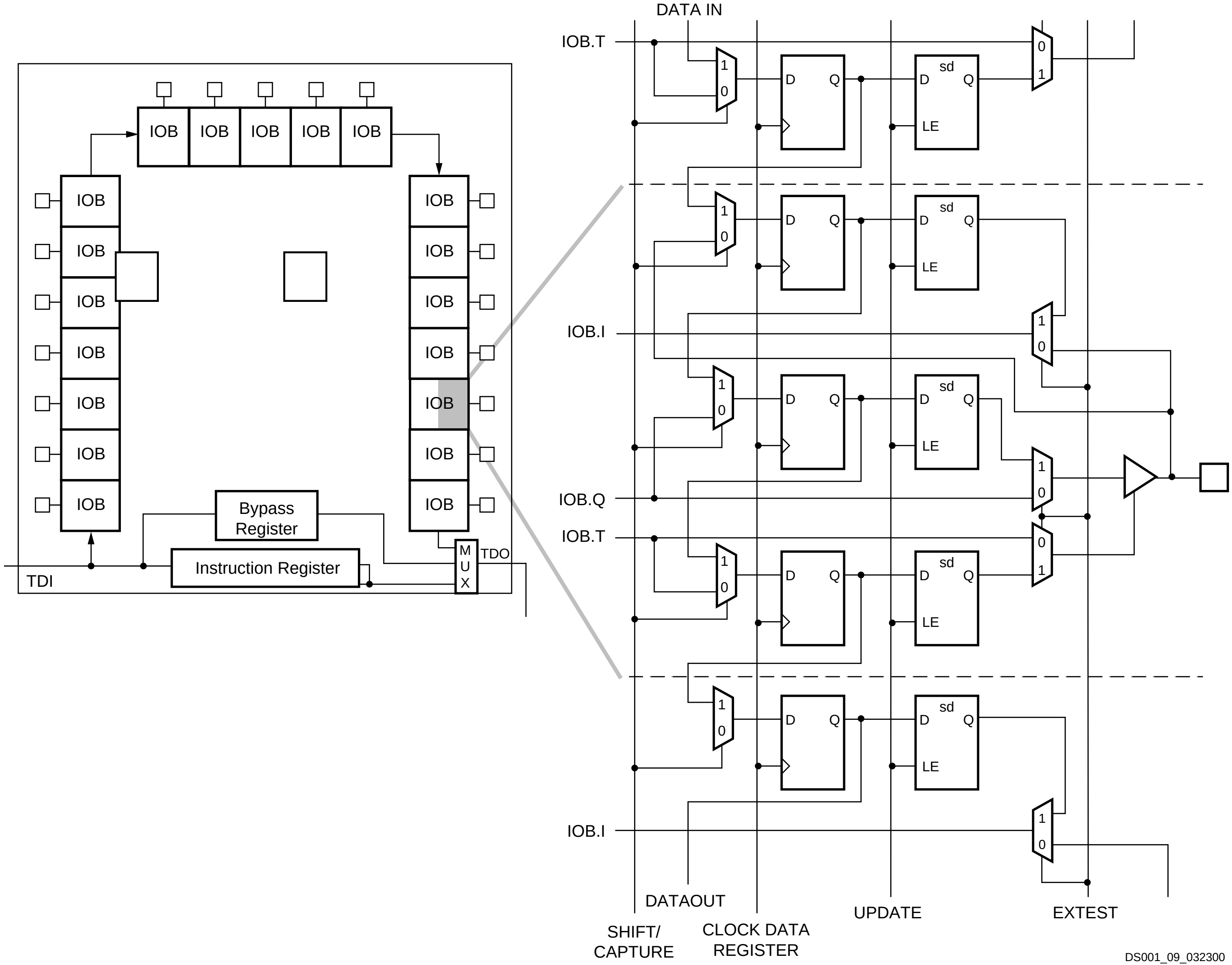


Figure 9: **Spartan-II Family Boundary Scan Logic**

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the Downloads area.

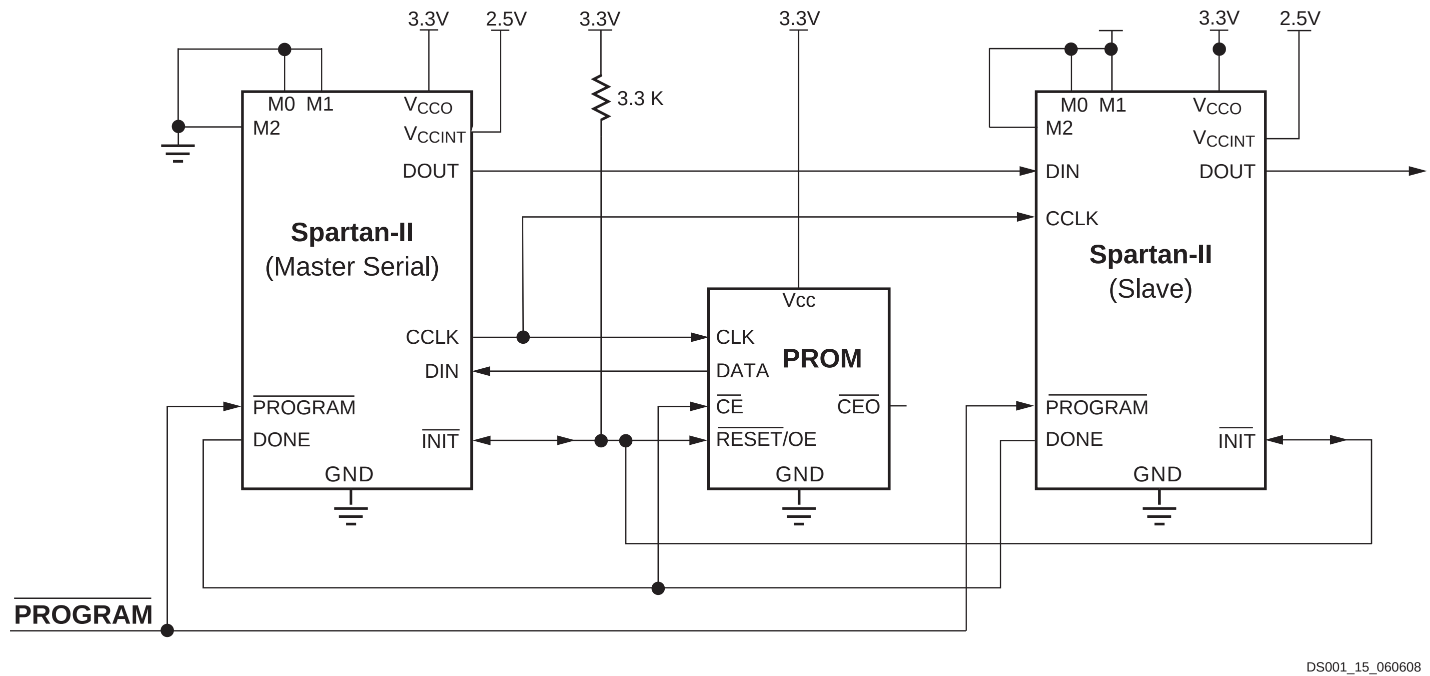
Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is $2^{20}-1$ (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until INIT pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.



Notes:

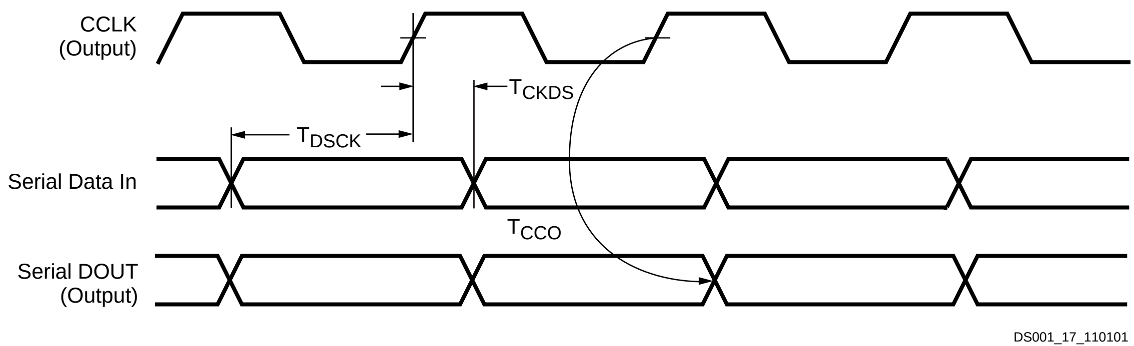
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 15: **Master/Slave Serial Configuration Circuit Diagram**

Master Serial Mode

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 15 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by INIT, and CE input is driven by DONE. The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx software. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point, the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The frequency of the CCLK signal created by the internal oscillator has a variance of +45%, –30% from the specified value.

Figure 17 shows the timing for Master Serial configuration. The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.



Symbol		Description		Units
T_{DSCK}	CCLK	DIN setup	5.0	ns, min
T_{CKDS}		DIN hold	0.0	ns, min
		Frequency tolerance with respect to nominal	+45%, –30%	-

Figure 17: **Master Serial Mode Timing**

Slave Parallel Mode

The Slave Parallel mode is the fastest configuration option. Byte-wide data is written into the FPGA. A BUSY flag is provided for controlling the flow of data at a clock frequency F_{CCNH} above 50 MHz.

Figure 18, page 24 shows the connections for two Spartan-II devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

If a configuration file of the format .bit, .rbt, or non-swapped HEX is used for parallel programming, then the most significant bit (i.e. the left-most bit of each configuration byte, as displayed in a text editor) must be routed to the D0 input on the FPGA.

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by de-asserting WRITE. See "Readback," page 25.

If CCLK is slower than F_{CCNH}, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

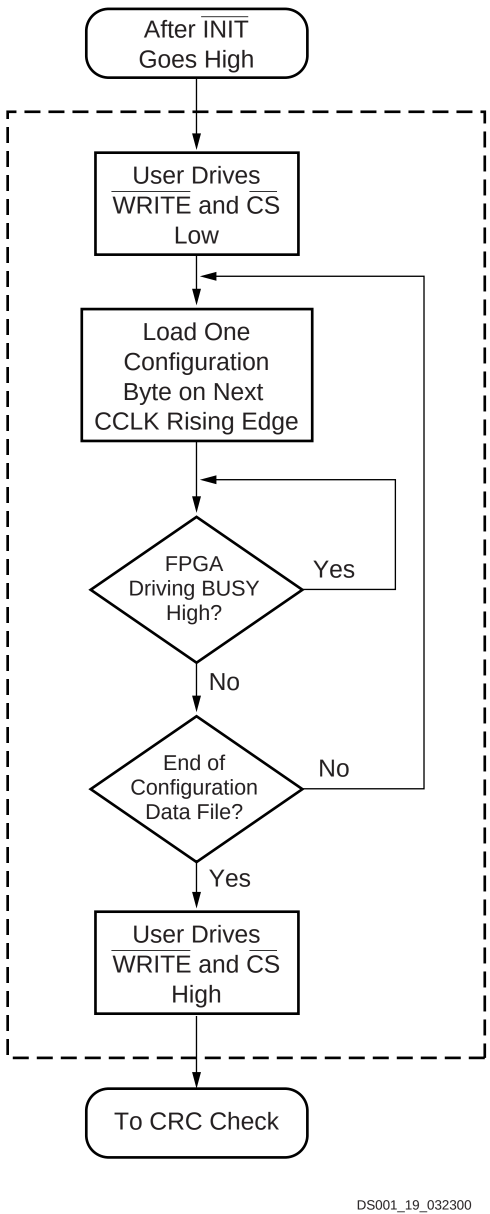


Figure 19: **Loading Configuration Data for the Slave Parallel Mode**

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of CS.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the CS signal may be de-asserted until the next byte is valid on D0-D7. While CS is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, WRITE must continue to be asserted while CS is asserted.

Abort

To abort configuration during a write sequence, de-assert WRITE while holding CS Low. The abort operation is initiated at the rising edge of CCLK, as shown in Figure 21, page 26. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

Boundary-Scan Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

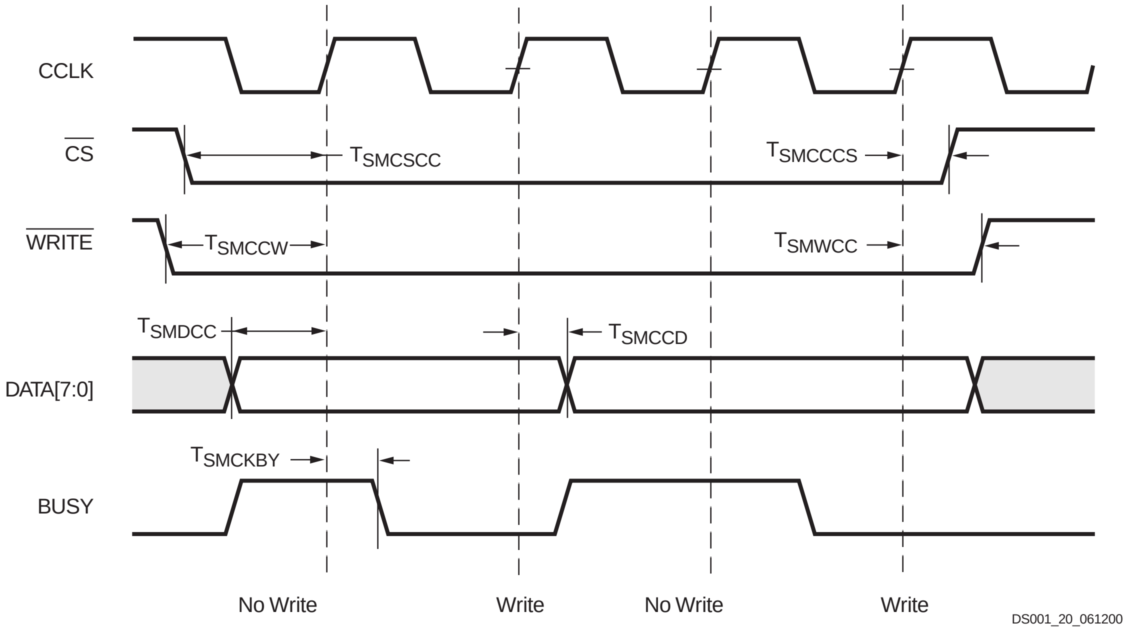
1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2).

Readback

The configuration data stored in the Spartan-II FPGA configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see XAPP176, *Spartan-II FPGA Family Configuration and Readback.*



Symbol		Description		Units
T_{SMDCC}	CCLK	D0-D7 setup/hold	5	ns, min
T_{SMCCD}		D0-D7 hold	0	ns, min
T_{SMCSCC}		$\overline{\text{CS}}$ setup	7	ns, min
T_{SMCCCS}		$\overline{\text{CS}}$ hold	0	ns, min
T_{SMCCW}		$\overline{\text{WRITE}}$ setup	7	ns, min
T_{SMWCC}		$\overline{\text{WRITE}}$ hold	0	ns, min
T_{SMCKBY}		BUSY propagation delay	12	ns, max
F_{CC}		Maximum frequency	66	MHz, max
F_{CCNH}		Maximum frequency with no handshake	50	MHz, max

Figure 20: **Slave Parallel Write Timing**

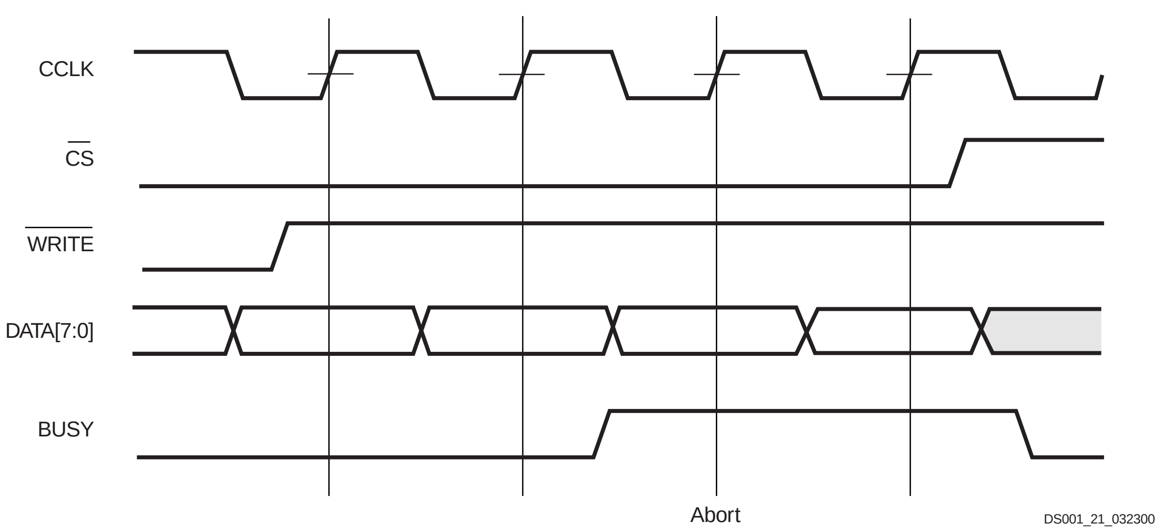


Figure 21: **Slave Parallel Write Abort Waveforms**

Using Block RAM Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block RAM memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block RAM memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Block RAM memory supports two operating modes.

- Read Through
- Write Back

Read Through (One Clock Edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (One Clock Edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

Block RAM Characteristics

1. All inputs are registered with the port clock and have a setup to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The block RAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

Library Primitives

Figure 31 and Figure 32 show the two generic library block RAM primitives. Table 11 describes all of the available primitives for synthesis and simulation.

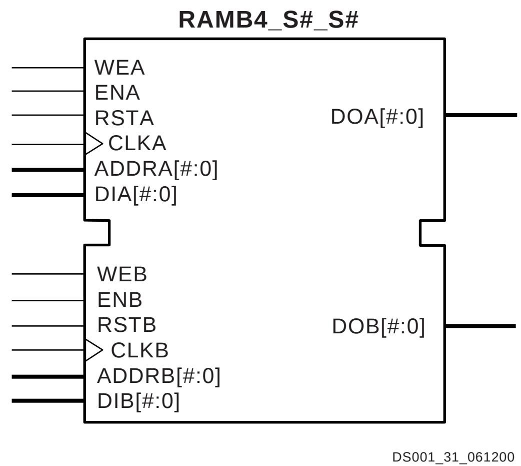


Figure 31: **Dual-Port Block RAM Memory**

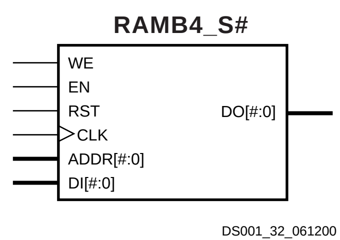


Figure 32: **Single-Port Block RAM Memory**

Table 11: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16

property. This property could have one of the following seven values.

DRIVE=2

DRIVE=4

DRIVE=6

DRIVE=8

DRIVE=12 (Default)

DRIVE=16

DRIVE=24

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36, page 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The V_{CCO} supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined V_{CCO} supply. The TQ144 and the CS144 packages provide four independent V_{CCO} supplies. The FG256 and the FG456 provide eight independent V_{CCO} supplies.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques:

None
Series
Parallel (Shunt)
Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None
Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 41.

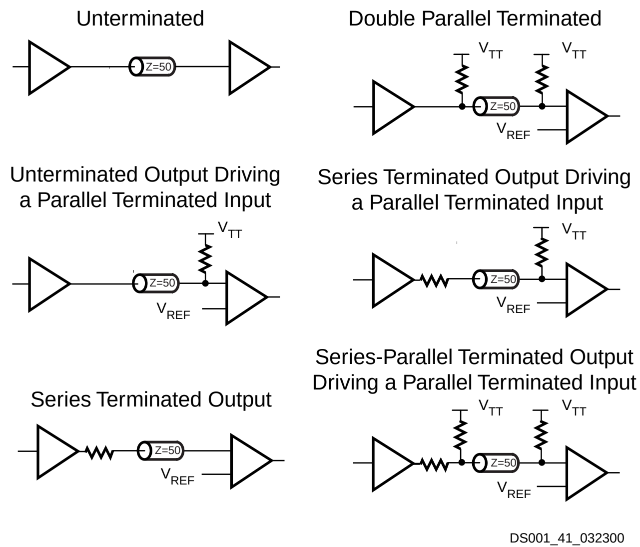


Figure 41: **Overview of Standard Input and Output Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 51. DC voltage specifications appear in Table 29 for the CTT standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics .

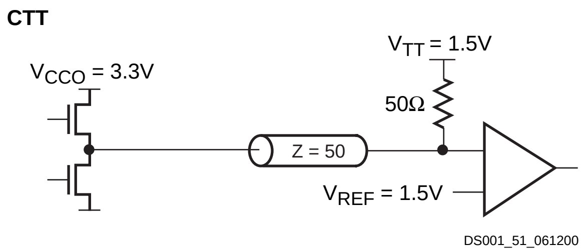


Figure 51: **Terminated CTT**

Table 29: **CTT Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.05(1)	3.3	3.6
V_{REF}	1.35	1.5	1.65
V_{TT}	1.35	1.5	1.65
$V_{IH} \geq V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} \leq V_{REF} - 0.2$	-	1.3	1.45
$V_{OH} \geq V_{REF} + 0.4$	1.75	1.9	-
$V_{OL} \leq V_{REF} - 0.4$	-	1.1	1.25
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1. Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 and PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 30 for the PCI33_3 and PCI66_3 standards. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 30: **PCI33_3 and PCI66_3 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
$V_{IH} = 0.5 \times V_{CCO}$	1.5	1.65	V_{CCO}+ 0.5
$V_{IL} = 0.3 \times V_{CCO}$	–0.5	0.99	1.08
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL} = 0.1 \times V_{CCO}$	-	-	0.36
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Notes:
1. Tested according to the relevant specification.

PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in Table 31 for the PCI33_5 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 31: **PCI33_5 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.425	1.5	5.5
V_{IL}	–0.5	1.0	1.05
V_{OH}	2.4	-	-
V_{OL}	-	-	0.55
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Notes:
1. Tested according to the relevant specification.

Power-On Requirements

Spartan-II FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CCINT} lines for a successful power-on. If more current is available, the FPGA can consume more than I_{CCPO} minimum, though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Therefore the use of foldback/crowbar supplies and fuses deserves special attention. In these cases, limit the I_{CCPO} current to a level below the trip point for over-current protection in order to avoid inadvertently shutting down the supply.

Symbol	Description	Conditions		New Requirements(1) For Devices with Date Code 0321 or Later		Old Requirements(1) For Devices with Date Code before 0321		Units
		Junction Temperature(2)	Device Temperature Grade	Min	Max	Min	Max	
I_{CCPO}(3)	Total V_{CCINT} supply current required during power-on	–40°C ≤ T_J < –20°C	Industrial	1.50	-	2.00	-	A
		–20°C ≤ T_J < 0°C	Industrial	1.00	-	2.00	-	A
		0°C ≤ T_J ≤ 85°C	Commercial	0.25	-	0.50	-	A
		85°C < T_J ≤ 100°C	Industrial	0.50	-	0.50	-	A
T_{CCPO}(4,5)	V_{CCINT} ramp time	–40°C ≤ T_J ≤ 100°C	All	-	50	-	50	ms

Notes:
1. The date code is printed on the top of the device's package. See the "Device Part Marking" section in Module 1.
2. The expected T_J range for the design determines the I_{CCPO} minimum requirement. Use the applicable ranges in the junction temperature column to find the associated current values in the appropriate new or old requirements column according to the date code. Then choose the highest of these current values to serve as the minimum I_{CCPO} requirement that must be met. For example, if the junction temperature for a given design is -25°C ≤ T_J ≤ 75°C, then the new minimum I_{CCPO} requirement is 1.5A. If 5°C ≤ T_J ≤ 90°C, then the new minimum I_{CCPO} requirement is 0.5A.
3. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CCINT} ramps from 0 to 2.5V.
4. The ramp time is measured from GND to V_{CCINT} max on a fully loaded board.
5. During power-on, the V_{CCINT} ramp must increase steadily in voltage with no dips.
6. For more information on designing to meet the power-on specifications, refer to the application note **XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families"**

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	–0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3V	–0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)
PCI, 5.0V	–0.5	0.8	2.0	5.5	0.55	2.4	Note (2)	Note (2)
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	N/A	40	N/A
GTL+	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	N/A	36	N/A
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	15.2	–15.2

Revision History

Date	Version No.	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Updated timing to reflect the latest speed files. Added current supply numbers and XC2S200 -5 timing numbers. Approved -5 timing numbers as preliminary information with exceptions as noted.
11/02/00	2.1	Removed Power Down feature.
01/19/01	2.2	DC and timing numbers updated to Preliminary for the XC2S50 and XC2S100. Industrial power-on current specifications and -6 DLL timing numbers added. Power-on specification clarified.
03/09/01	2.3	Added note on power sequencing. Clarified power-on current requirement.
08/28/01	2.4	Added -6 preliminary timing. Added typical and industrial standby current numbers. Specified min. power-on current by junction temperature instead of by device type (Commercial vs. Industrial). Eliminated minimum V_{CCINT} ramp time requirement. Removed footnote limiting DLL operation to the Commercial temperature range.
07/26/02	2.5	Clarified that I/O leakage current is specified over the Recommended Operating Conditions for V_{CCINT} and V_{CCO}.
08/26/02	2.6	Added references for XAPP450 to Power-On Current Specification.
09/03/03	2.7	Added relaxed minimum power-on current (I_{CCPO}) requirements to page 53. On page 64, moved T_{RPW} values from maximum to minimum column.
06/13/08	2.8	Updated I/O measurement thresholds. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.

Table 36: **Spartan-II Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass[(1)] (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	60	0.5	16 x 16	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	92	0.5	22 x 22	1.60	1.4
CS144 / CSG144	144	Chip Scale Ball Grid Array (CSBGA)	92	0.8	12 x 12	1.20	0.3
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	140	0.5	30.6 x 30.6	3.70	5.3
FG256 / FGG256	256	Fine-pitch Ball Grid Array (FBGA)	176	1.0	17 x 17	2.00	0.9
FG456 / FGG456	456	Fine-pitch Ball Grid Array (FBGA)	284	1.0	23 x 23	2.60	2.2

Notes:
1. Package mass is ±10%.

Note: Some early versions of Spartan-II devices, including the XC2S15 and XC2S30 ES devices and the XC2S150 with date code 0045 or earlier, included a power-down pin. For more information, see Answer Record 10500.

VCCO Banks

Some of the I/O standards require specific V_{CCO} voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3 in Module 2). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. In the smaller packages, the V_{CCO} pins are connected between banks, effectively reducing the number of independent banks available (see Table 37). These interconnected banks are shown in the Pinout Tables with V_{CCO} pads for multiple banks connected to the same pin.

Table 37: **Independent VCCO Banks Available**

Package	VQ100 PQ208	CS144 TQ144	FG256 FG456
Independent Banks	1	4	8

Package Overview

Table 36 shows the six low-cost, space-saving production package styles for the Spartan-II family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS144" package becomes "CSG144" when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 38.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 38.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

Table 38: **Xilinx Package Documentation**

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
CS144	Package Drawing	PK149_CS144
CSG144		PK103_CSG144
PQ208	Package Drawing	PK166_PQ208
PQG208		PK123_PQG208
FG256	Package Drawing	PK151_FG256
FGG256		PK105_FGG256
FG456	Package Drawing	PK154_FG456
FGG456		PK109_FGG456

XC2S15 Device Pinouts *(Continued)*

XC2S15 Pad Name					
Function	Bank	VQ100	TQ144	CS144	Bndry Scan
GND	-	-	P61	J12	-
I/O (D5)	3	P57	P60	J13	245
I/O	3	P58	P59	H10	248
I/O, V_{REF}	3	P59	P58	H11	251
I/O (D4)	3	P60	P57	H12	254
I/O	3	-	P56	H13	257
V_{CCINT}	-	P61	P55	G12	-
I/O, TRDY[1]	3	P62	P54	G13	260
V_{CCO}	3	P63	P53	G11	-
V_{CCO}	2	P63	P53	G11	-
GND	-	P64	P52	G10	-
I/O, IRDY[1]	2	P65	P51	F13	263
I/O	2	-	P50	F12	266
I/O (D3)	2	P66	P49	F11	269
I/O, V_{REF}	2	P67	P48	F10	272
I/O	2	P68	P47	E13	275
I/O (D2)	2	P69	P46	E12	278
GND	-	-	P45	E11	-
I/O (D1)	2	P70	P44	E10	281
I/O	2	P71	P43	D13	284
I/O, V_{REF}	2	P72	P41	D11	287
I/O	2	-	P40	C13	290
I/O (DIN, D0)	2	P73	P39	C12	293
I/O (DOUT, BUSY)	2	P74	P38	C11	296
CCLK	2	P75	P37	B13	299
V_{CCO}	2	P76	P36	B12	-
V_{CCO}	1	P76	P35	A13	-
TDO	2	P77	P34	A12	-
GND	-	P78	P33	B11	-
TDI	-	P79	P32	A11	-
I/O ($\overline{CS}$)	1	P80	P31	D10	0
I/O ($\overline{WRITE}$)	1	P81	P30	C10	3
I/O	1	-	P29	B10	6
I/O, V_{REF}	1	P82	P28	A10	9
I/O	1	P83	P27	D9	12
I/O	1	P84	P26	C9	15
GND	-	-	P25	B9	-
V_{CCINT}	-	P85	P24	A9	-
I/O	1	-	P23	D8	18
I/O	1	-	P22	C8	21

XC2S15 Device Pinouts *(Continued)*

XC2S15 Pad Name					
Function	Bank	VQ100	TQ144	CS144	Bndry Scan
I/O, V_{REF}	1	P86	P21	B8	24
I/O	1	-	P20	A8	27
I/O	1	P87	P19	B7	30
I, GCK2	1	P88	P18	A7	36
GND	-	P89	P17	C7	-
V_{CCO}	1	P90	P16	D7	-
V_{CCO}	0	P90	P16	D7	-
I, GCK3	0	P91	P15	A6	37
V_{CCINT}	-	P92	P14	B6	-
I/O	0	-	P13	C6	44
I/O, V_{REF}	0	P93	P12	D6	47
I/O	0	-	P11	A5	50
I/O	0	-	P10	B5	53
V_{CCINT}	-	P94	P9	C5	-
GND	-	-	P8	D5	-
I/O	0	P95	P7	A4	56
I/O	0	P96	P6	B4	59
I/O, V_{REF}	0	P97	P5	C4	62
I/O	0	-	P4	A3	65
I/O	0	P98	P3	B3	68
TCK	-	P99	P2	C3	-
V_{CCO}	0	P100	P1	A2	-
V_{CCO}	7	P100	P144	B2	-

04/18/01

Notes:

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S15 Package Pins

VQ100

Not Connected Pins					
P28	P29	-	-	-	-

11/02/00

TQ144

Not Connected Pins					
P42	P64	P78	P101	P104	P105
P116	P138	-	-	-	-

11/02/00

CS144

Not Connected Pins					
D3	D12	J4	K13	M3	M4
M10	N3	-	-	-	-

11/02/00

XC2S30 Device Pinouts *(Continued)*

XC2S30 Pad Name						
Function	Bank	VQ100	TQ144	CS144	PQ208	Bndry Scan
V_{CCINT}	-	P85	P24	A9	P171	-
I/O	1	-	P23	D8	P172	24
I/O	1	-	P22	C8	P173	27
I/O	1	-	-	-	P174	30
I/O	1	-	-	-	P175	33
I/O	1	-	-	-	P176	36
GND	-	-	-	-	P177	-
I/O, V_{REF}	1	P86	P21	B8	P178	39
I/O	1	-	-	-	P179	42
I/O	1	-	P20	A8	P180	45
I/O	1	P87	P19	B7	P181	48
I, GCK2	1	P88	P18	A7	P182	54
GND	-	P89	P17	C7	P183	-
V_{CCO}	1	P90	P16	D7	P184	-
V_{CCO}	0	P90	P16	D7	P184	-
I, GCK3	0	P91	P15	A6	P185	55
V_{CCINT}	-	P92	P14	B6	P186	-
I/O	0	-	P13	C6	P187	62
I/O	0	-	-	-	P188	65
I/O, V_{REF}	0	P93	P12	D6	P189	68
GND	-	-	-	-	P190	-
I/O	0	-	-	-	P191	71
I/O	0	-	-	-	P192	74
I/O	0	-	-	-	P193	77
I/O	0	-	P11	A5	P194	80
I/O	0	-	P10	B5	P195	83
V_{CCINT}	-	P94	P9	C5	P196	-
V_{CCO}	0	-	-	-	P197	-
GND	-	-	P8	D5	P198	-
I/O	0	P95	P7	A4	P199	86
I/O	0	P96	P6	B4	P200	89
I/O	0	-	-	-	P201	92

XC2S30 Device Pinouts *(Continued)*

XC2S30 Pad Name						
Function	Bank	VQ100	TQ144	CS144	PQ208	Bndry Scan
I/O, V_{REF}	0	P97	P5	C4	P203	95
I/O	0	-	-	-	P204	98
I/O	0	-	P4	A3	P205	101
I/O	0	P98	P3	B3	P206	104
TCK	-	P99	P2	C3	P207	-
V_{CCO}	0	P100	P1	A2	P208	-
V_{CCO}	7	P100	P144	B2	P208	-

04/18/01

Notes:
1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S30 Package Pins

VQ100

Not Connected Pins					
P28	P29	-	-	-	-

11/02/00

TQ144

Not Connected Pins					
P104	P105	-	-	-	-

11/02/00

CS144

Not Connected Pins					
M3	N3	-	-	-	-

11/02/00

PQ208

Not Connected Pins					
P7	P13	P38	P44	P55	P56
P60	P97	P112	P118	P143	P149
P165	P202	-	-	-	-

11/02/00

Notes:
1. For the PQ208 package, P13, P38, P118, and P143, which are Not Connected Pins on the XC2S30, are assigned to V_{CCINT} on larger devices.

XC2S50 Device Pinouts

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
GND	-	P143	P1	GND*	-
TMS	-	P142	P2	D3	-
I/O	7	P141	P3	C2	149
I/O	7	-	-	A2	152
I/O	7	P140	P4	B1	155
I/O	7	-	-	E3	158
I/O	7	-	P5	D2	161
GND	-	-	-	GND*	-
I/O, V_{REF}	7	P139	P6	C1	164
I/O	7	-	P7	F3	167
I/O	7	-	-	E2	170
I/O	7	P138	P8	E4	173
I/O	7	P137	P9	D1	176
I/O	7	P136	P10	E1	179
GND	-	P135	P11	GND*	-
V_{CCO}	7	-	P12	V_{CCO} Bank 7*	-
V_{CCINT}	-	-	P13	V_{CCINT}*	-
I/O	7	P134	P14	F2	182
I/O	7	P133	P15	G3	185
I/O	7	-	-	F1	188
I/O	7	-	P16	F4	191
I/O	7	-	P17	F5	194
I/O	7	-	P18	G2	197
GND	-	-	P19	GND*	-
I/O, V_{REF}	7	P132	P20	H3	200
I/O	7	P131	P21	G4	203
I/O	7	-	-	H2	206
I/O	7	P130	P22	G5	209
I/O	7	-	P23	H4	212
I/O, IRDY(1)	7	P129	P24	G1	215
GND	-	P128	P25	GND*	-
V_{CCO}	7	P127	P26	V_{CCO} Bank 7*	-
V_{CCO}	6	P127	P26	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P126	P27	J2	218
V_{CCINT}	-	P125	P28	V_{CCINT}*	-
I/O	6	P124	P29	H1	224
I/O	6	-	-	J4	227
I/O	6	P123	P30	J1	230
I/O, V_{REF}	6	P122	P31	J3	233

XC2S50 Device Pinouts *(Continued)*

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
GND	-	-	P32	GND*	-
I/O	6	-	P33	K5	236
I/O	6	-	P34	K2	239
I/O	6	-	P35	K1	242
I/O	6	-	-	K3	245
I/O	6	P121	P36	L1	248
I/O	6	P120	P37	L2	251
V_{CCINT}	-	-	P38	V_{CCINT}*	-
V_{CCO}	6	-	P39	V_{CCO} Bank 6*	-
GND	-	P119	P40	GND*	-
I/O	6	P118	P41	K4	254
I/O	6	P117	P42	M1	257
I/O	6	P116	P43	L4	260
I/O	6	-	-	M2	263
I/O	6	-	P44	L3	266
I/O, V_{REF}	6	P115	P45	N1	269
GND	-	-	-	GND*	-
I/O	6	-	P46	P1	272
I/O	6	-	-	L5	275
I/O	6	P114	P47	N2	278
I/O	6	-	-	M4	281
I/O	6	P113	P48	R1	284
I/O	6	P112	P49	M3	287
M1	-	P111	P50	P2	290
GND	-	P110	P51	GND*	-
M0	-	P109	P52	N3	291
V_{CCO}	6	P108	P53	V_{CCO} Bank 6*	-
V_{CCO}	5	P107	P53	V_{CCO} Bank 5*	-
M2	-	P106	P54	R3	292
I/O	5	-	-	N5	299
I/O	5	P103	P57	T2	302
I/O	5	-	-	P5	305
I/O	5	-	P58	T3	308
GND	-	-	-	GND*	-
I/O, V_{REF}	5	P102	P59	T4	311
I/O	5	-	P60	M6	314
I/O	5	-	-	T5	317
I/O	5	P101	P61	N6	320
I/O	5	P100	P62	R5	323

XC2S50 Device Pinouts *(Continued)*

XC2S50 Pad Name					
Function	Bank	TQ144	PQ208	FG256	Bndry Scan
I/O	3	-	-	J14	503
I/O	3	P56	P127	K15	506
V_{CCINT}	-	P55	P128	V_{CCINT}*	-
I/O, TRDY(1)	3	P54	P129	J15	512
V_{CCO}	3	P53	P130	V_{CCO} Bank 3*	-
V_{CCO}	2	P53	P130	V_{CCO} Bank 2*	-
GND	-	P52	P131	GND*	-
I/O, IRDY(1)	2	P51	P132	H16	515
I/O	2	-	P133	H14	518
I/O	2	P50	P134	H15	521
I/O	2	-	-	J13	524
I/O (D3)	2	P49	P135	G16	527
I/O, V_{REF}	2	P48	P136	H13	530
GND	-	-	P137	GND*	-
I/O	2	-	P138	G14	533
I/O	2	-	P139	G15	536
I/O	2	-	P140	G12	539
I/O	2	-	-	F16	542
I/O	2	P47	P141	G13	545
I/O (D2)	2	P46	P142	F15	548
V_{CCINT}	-	-	P143	V_{CCINT}*	-
V_{CCO}	2	-	P144	V_{CCO} Bank 2*	-
GND	-	P45	P145	GND*	-
I/O (D1)	2	P44	P146	E16	551
I/O	2	P43	P147	F14	554
I/O	2	P42	P148	D16	557
I/O	2	-	-	F12	560
I/O	2	-	P149	E15	563
I/O, V_{REF}	2	P41	P150	F13	566
GND	-	-	-	GND*	-
I/O	2	-	P151	E14	569
I/O	2	-	-	C16	572
I/O	2	P40	P152	E13	575
I/O	2	-	-	B16	578
I/O (DIN, D0)	2	P39	P153	D14	581
I/O (DOUT, BUSY)	2	P38	P154	C15	584
CCLK	2	P37	P155	D15	587
V_{CCO}	2	P36	P156	V_{CCO} Bank 2*	-

XC2S50 Device Pinouts *(Continued)*

XC2S50 Pad Name					
Function	Bank	TQ144	PQ208	FG256	Bndry Scan
V_{CCO}	1	P35	P156	V_{CCO} Bank 1*	-
TDO	2	P34	P157	B14	-
GND	-	P33	P158	GND*	-
TDI	-	P32	P159	A15	-
I/O ($\overline{CS}$)	1	P31	P160	B13	0
I/O ($\overline{WRITE}$)	1	P30	P161	C13	3
I/O	1	-	-	C12	6
I/O	1	P29	P162	A14	9
I/O	1	-	-	D12	12
I/O	1	-	P163	B12	15
GND	-	-	-	GND*	-
I/O, V_{REF}	1	P28	P164	C11	18
I/O	1	-	P165	A13	21
I/O	1	-	-	D11	24
I/O	1	-	P166	A12	27
I/O	1	P27	P167	E11	30
I/O	1	P26	P168	B11	33
GND	-	P25	P169	GND*	-
V_{CCO}	1	-	P170	V_{CCO} Bank 1*	-
V_{CCINT}	-	P24	P171	V_{CCINT}*	-
I/O	1	P23	P172	A11	36
I/O	1	P22	P173	C10	39
I/O	1	-	P174	B10	45
I/O	1	-	P175	D10	48
I/O	1	-	P176	A10	51
GND	-	-	P177	GND*	-
I/O, V_{REF}	1	P21	P178	B9	54
I/O	1	-	P179	E10	57
I/O	1	-	-	A9	60
I/O	1	P20	P180	D9	63
I/O	1	P19	P181	A8	66
I, GCK2	1	P18	P182	C9	72
GND	-	P17	P183	GND*	-
V_{CCO}	1	P16	P184	V_{CCO} Bank 1*	-
V_{CCO}	0	P16	P184	V_{CCO} Bank 0*	-
I, GCK3	0	P15	P185	B8	73
V_{CCINT}	-	P14	P186	V_{CCINT}*	-
I/O	0	P13	P187	A7	80

XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O	6	P46	P1	T4	404
I/O	6	-	L5	W1	407
I/O	6	-	-	V2	410
I/O	6	-	-	U4	413
I/O	6	P47	N2	Y1	416
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	419
I/O	6	-	-	V3	422
I/O	6	-	-	V4	425
I/O	6	P48	R1	Y2	428
I/O	6	P49	M3	W3	431
M1	-	P50	P2	U5	434
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	435
V_{CCO}	6	P53	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
V_{CCO}	5	P53	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
M2	-	P54	R3	Y4	436
I/O	5	-	-	W5	443
I/O	5	-	-	AB3	446
I/O	5	-	N5	V7	449
GND	-	-	GND*	GND*	-
I/O	5	P57	T2	Y6	452
I/O	5	-	-	AA4	455
I/O	5	-	-	AB4	458
I/O	5	-	P5	W6	461
I/O	5	P58	T3	Y7	464
GND	-	-	GND*	GND*	-
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P59	T4	AA5	467
I/O	5	P60	M6	AB5	470
I/O	5	-	-	V8	473
I/O	5	-	-	AA6	476
I/O	5	-	T5	AB6	479
I/O	5	P61	N6	AA7	482
I/O	5	-	-	W7	485
I/O, V_{REF}	5	P62	R5	W8	488
I/O	5	P63	P6	Y8	491
GND	-	P64	GND*	GND*	-

XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
V_{CCO}	5	P65	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCINT}	-	P66	V_{CCINT}*	V_{CCINT}*	-
I/O	5	P67	R6	AA8	494
I/O	5	P68	M7	V9	497
I/O	5	-	-	W9	503
I/O	5	-	-	AB9	506
I/O	5	P69	N7	Y9	509
I/O	5	-	-	V10	512
I/O	5	P70	T6	W10	518
I/O	5	P71	P7	AB10	521
GND	-	P72	GND*	GND*	-
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P73	P8	Y10	524
I/O	5	P74	R7	V11	527
I/O	5	-	T7	W11	530
I/O	5	P75	T8	AB11	533
I/O	5	-	-	U11	536
V_{CCINT}	-	P76	V_{CCINT}*	V_{CCINT}*	-
I, GCK1	5	P77	R8	Y11	545
V_{CCO}	5	P78	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCO}	4	P78	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-
I, GCK0	4	P80	N8	W12	546
I/O	4	P81	N9	U12	550
I/O	4	-	-	V12	553
I/O	4	P82	R9	Y12	556
I/O	4	-	N10	AA12	559
I/O	4	P83	T9	AB13	562
I/O, V_{REF}	4	P84	P9	AA13	565
V_{CCO}	4	-	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P85	GND*	GND*	-
I/O	4	P86	M10	Y13	568
I/O	4	P87	R10	V13	571
I/O	4	-	-	W14	577
I/O	4	P88	P10	AA14	580
I/O	4	-	-	V14	583
I/O	4	-	-	Y14	586
I/O	4	P89	T10	AB15	592

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I, GCK0	4	P80	N8	W12	636
I/O	4	P81	N9	U12	640
I/O	4	-	-	V12	646
I/O	4	P82	R9	Y12	649
I/O	4	-	N10	AA12	652
I/O	4	-	-	W13	655
I/O	4	P83	T9	AB13	661
I/O, V_{REF}	4	P84	P9	AA13	664
V_{CCO}	4	-	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P85	GND*	GND*	-
I/O	4	P86	M10	Y13	667
I/O	4	P87	R10	V13	670
I/O	4	-	-	AB14	673
I/O	4	-	-	W14	676
I/O	4	P88	P10	AA14	679
GND	-	-	GND*	GND*	-
I/O	4	-	-	V14	682
I/O	4	-	-	Y14	685
I/O	4	-	-	W15	688
I/O	4	P89	T10	AB15	691
I/O	4	P90	R11	AA15	694
V_{CCINT}	-	P91	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	4	P92	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P93	GND*	GND*	-
I/O	4	P94	M11	Y15	697
I/O, V_{REF}	4	P95	T11	AB16	700
I/O	4	-	-	AB17	706
I/O	4	P96	N11	V15	709
GND	-	-	GND*	GND*	-
I/O	4	-	R12	Y16	712
I/O	4	-	-	AA17	715
I/O	4	-	-	W16	718
I/O	4	P97	P11	AB18	721
I/O, V_{REF}	4	P98	T12	AB19	724
V_{CCO}	4	-	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	-	GND*	GND*	-
I/O	4	P99	T13	Y17	727
I/O	4	-	N12	V16	730
I/O	4	-	-	AA18	733

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O	4	-	-	W17	739
I/O, V_{REF}	4	P100	R13	AB20	742
GND	-	-	GND*	GND*	-
I/O	4	-	P12	AA19	745
I/O	4	-	-	V17	748
I/O	4	-	-	Y18	751
I/O	4	P101	P13	AA20	757
I/O	4	P102	T14	W18	760
GND	-	P103	GND*	GND*	-
DONE	3	P104	R14	Y19	763
V_{CCO}	4	P105	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
V_{CCO}	3	P105	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
$\overline{\text{PROGRAM}}$	-	P106	P15	W20	766
I/O ($\overline{\text{INIT}}$)	3	P107	N15	V19	767
I/O (D7)	3	P108	N14	Y21	770
I/O	3	-	-	V20	776
I/O	3	-	-	AA22	779
I/O	3	-	T15	W21	782
GND	-	-	GND*	GND*	-
I/O, V_{REF}	3	P109	M13	U20	785
I/O	3	-	-	U19	788
I/O	3	-	-	V21	794
GND	-	-	GND*	GND*	-
I/O	3	-	R16	T18	797
I/O	3	P110	M14	W22	800
GND	-	-	GND*	GND*	-
V_{CCO}	3	-	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
I/O, V_{REF}	3	P111	L14	U21	803
I/O	3	P112	M15	T20	806
I/O	3	-	-	T19	809
I/O	3	-	-	V22	812
I/O	3	-	L12	T21	815
GND	-	-	GND*	GND*	-
I/O	3	P113	P16	R18	818
I/O	3	-	-	U22	821
I/O, V_{REF}	3	P114	L13	R19	827
I/O (D6)	3	P115	N16	T22	830
GND	-	P116	GND*	GND*	-