# AMD Xilinx - XC2S100-5FGG256I Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 600 |
| Number of Logic Elements/Cells | 2700 |
| Total RAM Bits | 40960 |
| Number of I/O | 176 |
| Number of Gates | 100000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 256-BGA |
| Supplier Device Package | 256-FBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s100-5fgg256i |

## General Overview

The Spartan-II family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-II FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes.

Spartan-II FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-II FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-II FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-II devices provide system clock rates up to 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-II FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

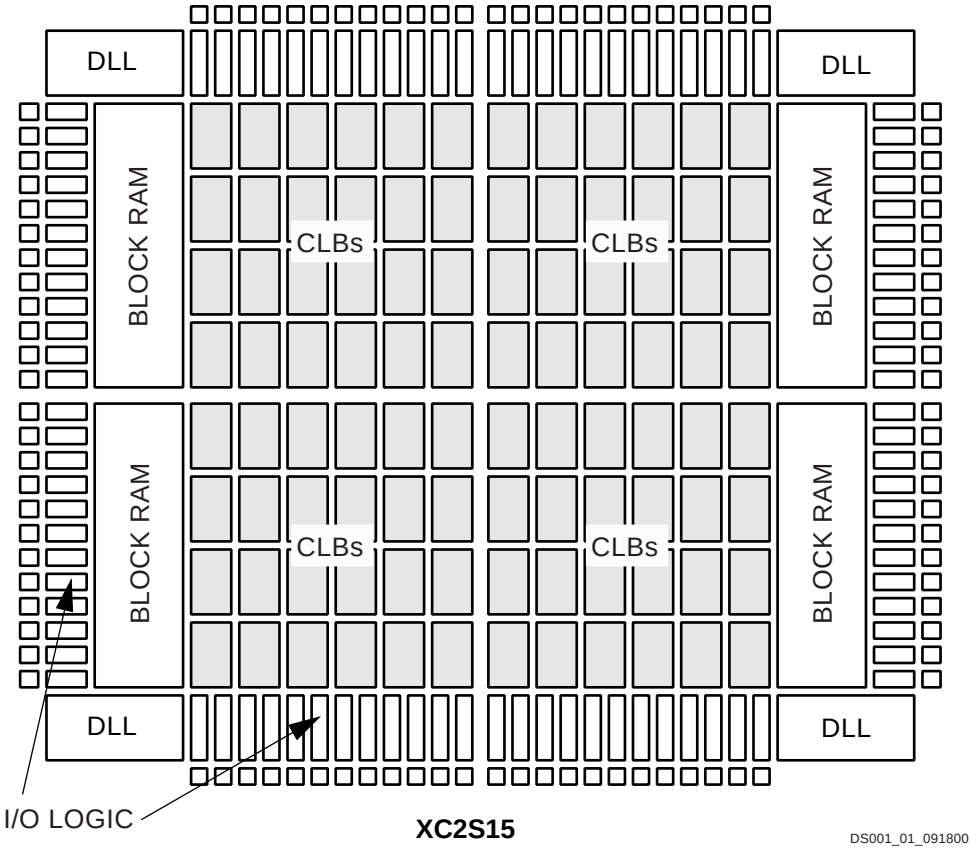



*Figure 1:* **Basic Spartan-II Family FPGA Block Diagram**

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

### *Arithmetic Logic*

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-II FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

### *BUFTs*

Each Spartan-II FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing," page 12. Each Spartan-II FPGA BUFT has an independent 3-state control pin and an independent input pin.

## Block RAM

Spartan-II FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks.

*Table 5:* **Spartan-II Block RAM Amounts**

| Spartan-II Device | # of Blocks | Total Block RAM Bits |
|---|---|---|
| XC2S15 | 4 | 16K |
| XC2S30 | 6 | 24K |
| XC2S50 | 8 | 32K |
| XC2S100 | 10 | 40K |
| XC2S150 | 12 | 48K |
| XC2S200 | 14 | 56K |

Each block RAM cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

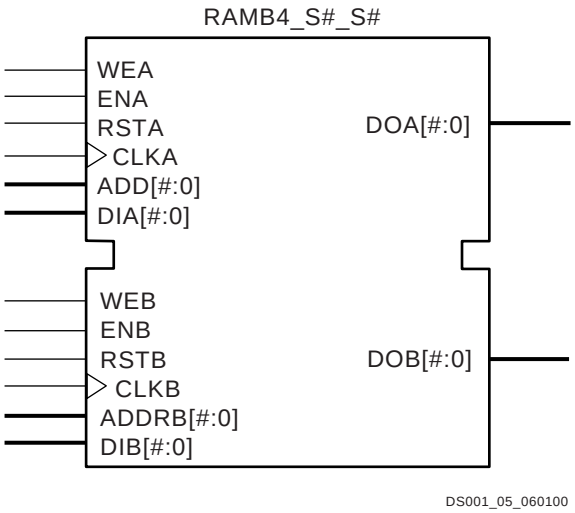



*Figure 5:* **Dual-Port Block RAM**

Table 6 shows the depth and width aspect ratios for the block RAM.

*Table 6:* **Block RAM Port Aspect Ratios**

| Width | Depth | ADDR Bus | Data Bus |
|---|---|---|---|
| 1 | 4096 | ADDR<11:0> | DATA<0> |
| 2 | 2048 | ADDR<10:0> | DATA<1:0> |
| 4 | 1024 | ADDR<9:0> | DATA<3:0> |
| 8 | 512 | ADDR<8:0> | DATA<7:0> |
| 16 | 256 | ADDR<7:0> | DATA<15:0> |

The Spartan-II FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

## Programmable Routing Matrix

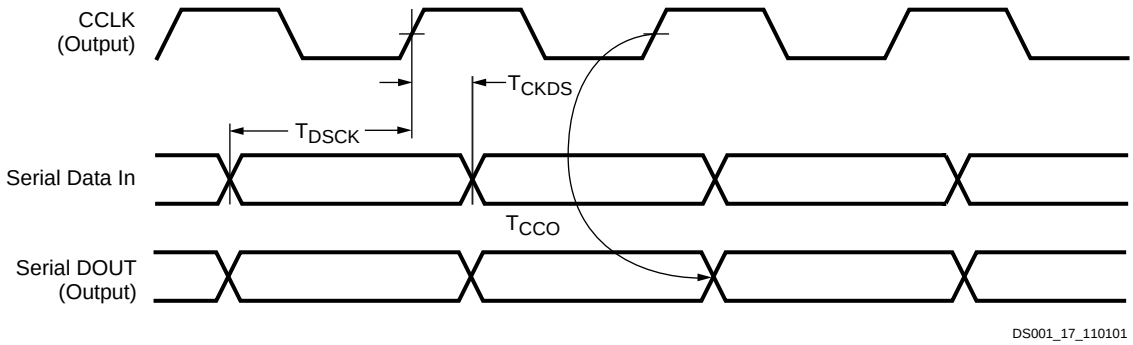
It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

### *Master Serial Mode*

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 15 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by $\overline{\text{INIT}}$, and CE input is driven by DONE. The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx software. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point, the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The frequency of the CCLK signal created by the internal oscillator has a variance of +45%, –30% from the specified value.

Figure 17 shows the timing for Master Serial configuration. The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.




| Symbol | | Description | | Units |
|---|---|---|---|---|
| $T_{DSCK}$ | CCLK | DIN setup | 5.0 | ns, min |
| $T_{CKDS}$ | | DIN hold | 0.0 | ns, min |
| | | Frequency tolerance with respect to nominal | +45%, –30% | - |

*Figure 17:* **Master Serial Mode Timing**

## Slave Parallel Mode

The Slave Parallel mode is the fastest configuration option. Byte-wide data is written into the FPGA. A BUSY flag is provided for controlling the flow of data at a clock frequency $F_{CCNH}$ above 50 MHz.

Figure 18, page 24 shows the connections for two Spartan-II devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

If a configuration file of the format .bit, .rbt, or non-swapped HEX is used for parallel programming, then the most significant bit (i.e. the left-most bit of each configuration byte, as displayed in a text editor) must be routed to the D0 input on the FPGA.

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by de-asserting $\overline{\text{WRITE}}$. See "Readback," page 25.

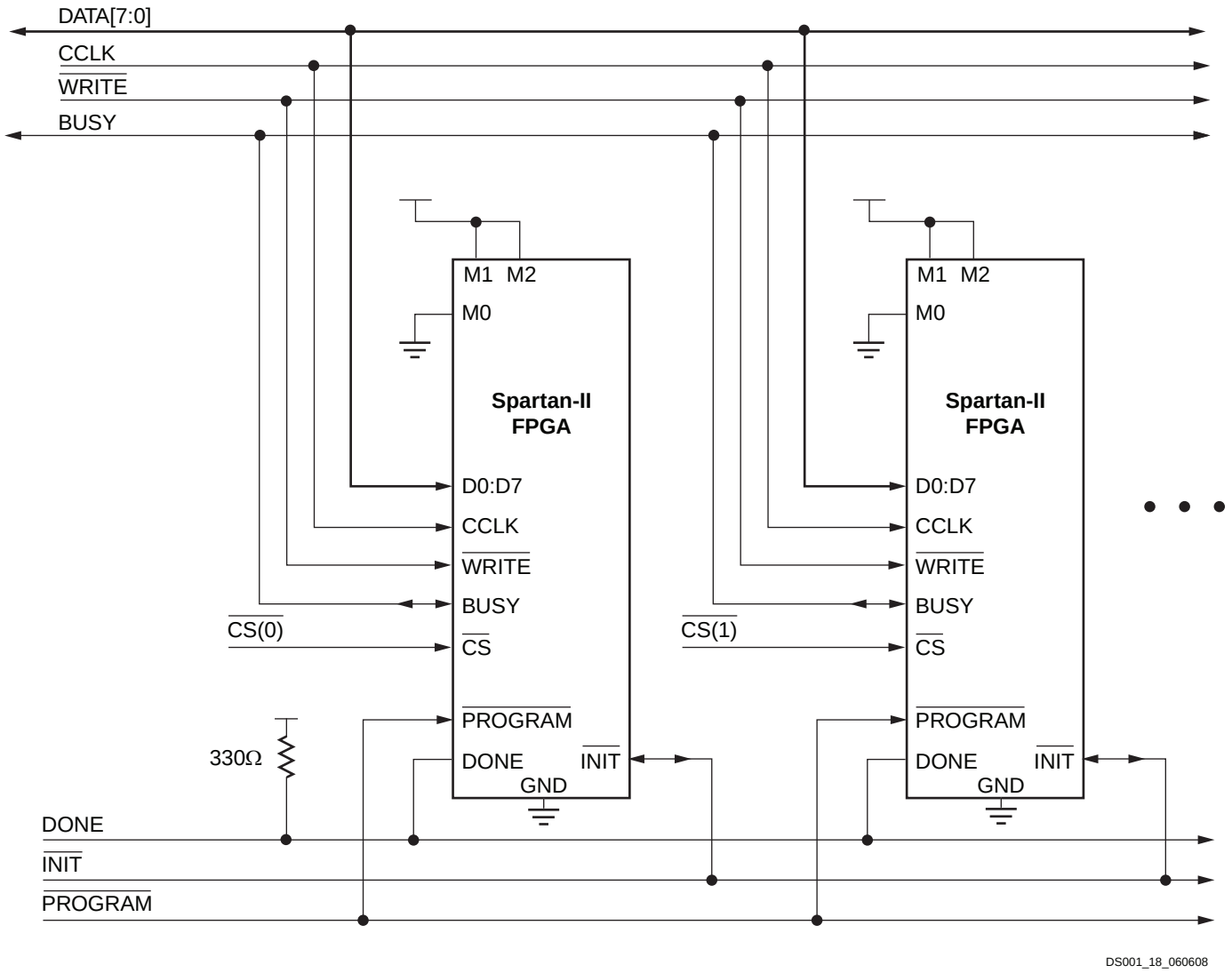



*Figure 18:* **Slave Parallel Configuration Circuit Diagram**

Multiple Spartan-II FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See "Start-up," page 19.

### *Write*

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 19, page 25 shows a flowchart of the write sequence used to load data into the Spartan-II FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 11, page 18. The timing for write operations is shown in Figure 20, page 26.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

If CCLK is slower than $F_{CCNH}$, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

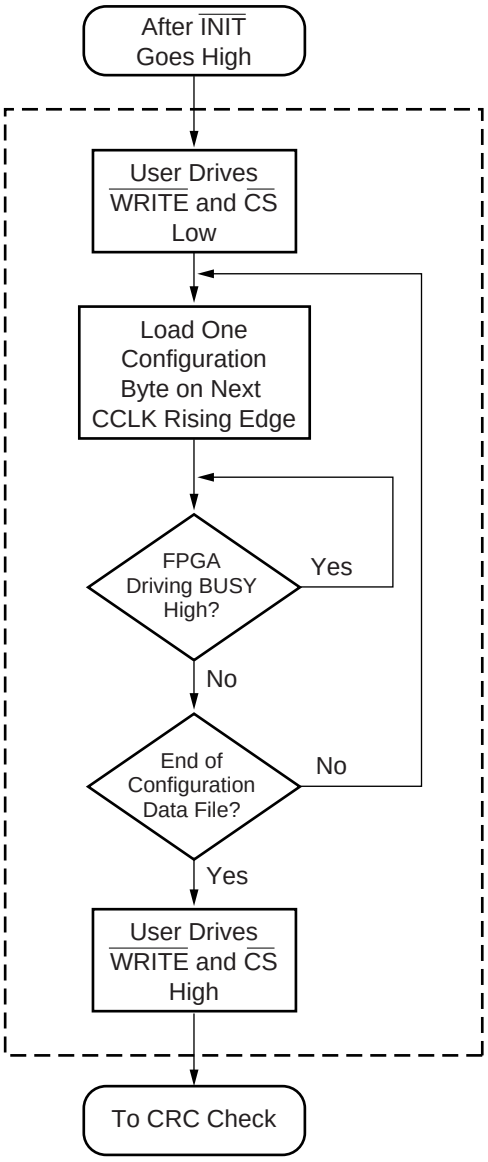



*Figure 19:* **Loading Configuration Data for the Slave Parallel Mode**

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of $\overline{CS}$.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the $\overline{CS}$ signal may be de-asserted until the next byte is valid on D0-D7. While $\overline{CS}$ is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted.

### *Abort*

To abort configuration during a write sequence, de-assert $\overline{WRITE}$ while holding $\overline{CS}$ Low. The abort operation is initiated at the rising edge of CCLK, as shown in Figure 21, page 26. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

## Boundary-Scan Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2).

# Readback

The configuration data stored in the Spartan-II FPGA configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see XAPP176, *Spartan-II FPGA Family Configuration and Readback.*

## BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 25.

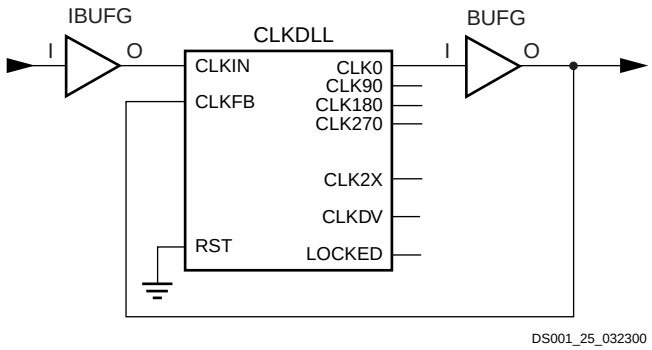



*Figure 25:* **BUFGDLL Block Diagram**

This macro does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This macro also does not provide access to the RST or LOCKED pins of the DLL. For access to these features, a designer must use the DLL primitives described in the following sections.

### *Source Clock Input — I*

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

### *Clock Output — O*

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG primitive, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50/50 duty cycle unless you deactivate the duty cycle correction property.

## CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

### *Source Clock Input — CLKIN*

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

### *Feedback Clock Input — CLKFB*

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. Either a global clock buffer (BUFG) or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feed back to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software to determine which DLL clock output sources the CLKFB pin.

### *Reset Input — RST*

When the reset pin RST activates, the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or be tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer deskew with respect to one another. The DLL must be reset when the input clock frequency changes, if the device is reconfigured in Boundary-Scan mode, if the device undergoes a hot swap, and after the device is configured if the input clock is not stable during the startup sequence.

### *2x Clock Output — CLK2X*

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

### *Clock Divide Output — CLKDV*

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction. The CLKDV output pin has a 50/50 duty cycle for all values of the

### Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the Startup Sequence following device configuration is paused at a user-specified point until the DLL locks. **XAPP176**: *Configuration and Readback of the Spartan-II and Spartan-IIE Families* explains how this can result in delaying the assertion of the DONE pin until the DLL locks.

### DLL Location Constraints

The DLLs are distributed such that there is one DLL in each corner of the device. The location constraint LOC, attached to the DLL primitive with the numeric identifier 0, 1, 2, or 3, controls DLL location. The orientation of the four DLLs and their corresponding clock resources appears in Figure 27.

The LOC property uses the following form.

LOC = DLL2

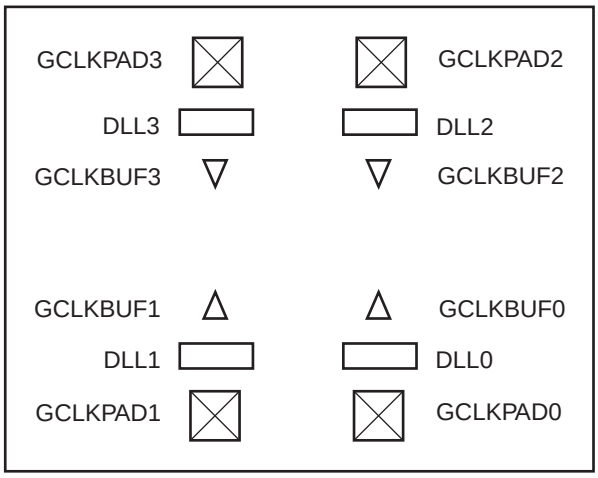



*Figure 27:* **Orientation of DLLs**

## Design Considerations

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

### Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the "DLL Timing Parameters" section of the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

### Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock in a way that has little impact to the DLL. Stopping the clock should be limited to less than approximately 100 µs to keep device cooling to a minimum and maintain the validity of the current tap setting. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED will stay High and remain High when the clock is restored. If these conditions may not be met in the design, apply a manual reset to the DLL after re-starting the input clock, even if the LOCKED signal has not changed.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

### Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). One DLL output can drive more than one OBUF; however, this adds skew.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

# Using Block RAM Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block RAM memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block RAM memory offers new capabilities allowing the FPGA designer to simplify designs.

## Operating Modes

Block RAM memory supports two operating modes.

- Read Through
- Write Back

### *Read Through (One Clock Edge)*

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

### *Write Back (One Clock Edge)*

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

## Block RAM Characteristics

1. All inputs are registered with the port clock and have a setup to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The block RAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

## Library Primitives

Figure 31 and Figure 32 show the two generic library block RAM primitives. Table 11 describes all of the available primitives for synthesis and simulation.

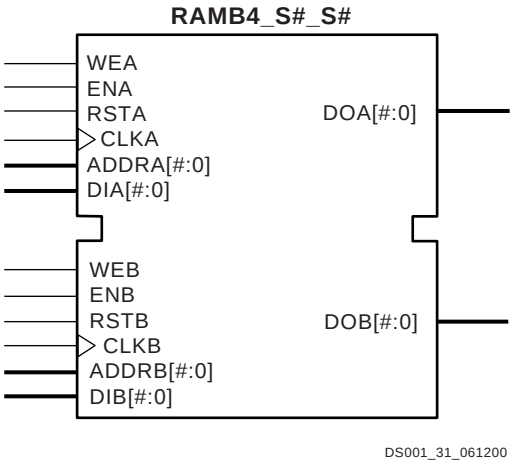



*Figure 31:* **Dual-Port Block RAM Memory**

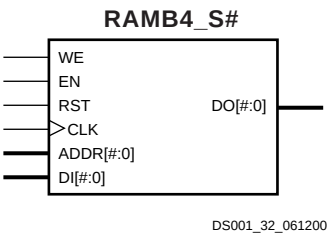



*Figure 32:* **Single-Port Block RAM Memory**

*Table 11:* **Available Library Primitives**

| Primitive | Port A Width | Port B Width |
|---|---|---|
| RAMB4_S1 | 1 | N/A |
| RAMB4_S1_S1 | | 1 |
| RAMB4_S1_S2 | | 2 |
| RAMB4_S1_S4 | | 4 |
| RAMB4_S1_S8 | | 8 |
| RAMB4_S1_S16 | | 16 |
| RAMB4_S2 | 2 | N/A |
| RAMB4_S2_S2 | | 2 |
| RAMB4_S2_S4 | | 4 |
| RAMB4_S2_S8 | | 8 |
| RAMB4_S2_S16 | | 16 |

support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage ($V_{REF}$) and output source voltage ($V_{CCO}$), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features, system-level design and board design can be greatly simplified and improved.

## Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 15, each buffer type can support a variety of voltage requirements.

*Table 15:* **Versatile I/O Supported Standards (Typical Values)**

| I/O Standard | Input Reference Voltage ($V_{REF}$) | Output Source Voltage ($V_{CCO}$) | Board Termination Voltage ($V_{TT}$) |
|---|---|---|---|
| LVTTL (2-24 mA) | N/A | 3.3 | N/A |
| LVCMOS2 | N/A | 2.5 | N/A |
| PCI (3V/5V, 33 MHz/66 MHz) | N/A | 3.3 | N/A |
| GTL | 0.8 | N/A | 1.2 |
| GTL+ | 1.0 | N/A | 1.5 |
| HSTL Class I | 0.75 | 1.5 | 0.75 |
| HSTL Class III | 0.9 | 1.5 | 1.5 |
| HSTL Class IV | 0.9 | 1.5 | 1.5 |
| SSTL3 Class I and II | 1.5 | 3.3 | 1.5 |
| SSTL2 Class I and II | 1.25 | 2.5 | 1.25 |
| CTT | 1.5 | 3.3 | 1.5 |
| AGP-2X | 1.32 | 3.3 | N/A |

## Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance JEDEC website at http://www.jedec.org. For more details on the I/O standards and termination application examples, see XAPP179, "*Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs.*"

### *LVTTL — Low-Voltage TTL*

The Low-Voltage TTL (LVTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a termination voltage ($V_{TT}$).

### *LVCMOS2 — Low-Voltage CMOS for 2.5V*

The Low-Voltage CMOS for 2.5V or lower (LVCMOS2) standard is an extension of the LVCMOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$).

property. This property could have one of the following seven values.

DRIVE=2

DRIVE=4

DRIVE=6

DRIVE=8

DRIVE=12 (Default)

DRIVE=16

DRIVE=24

## Design Considerations

### Reference Voltage ($V_{REF}$) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage ($V_{REF}$). Provide the $V_{REF}$ as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 36, page 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input.

Within each $V_{REF}$ bank, any input buffers that require a $V_{REF}$ signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same $V_{REF}$ bank.

### Output Drive Source Voltage ($V_{CCO}$) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage ($V_{CCO}$). As a result each device can often have to support multiple output drive source voltages.

The $V_{CCO}$ supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined $V_{CCO}$ supply. The TQ144 and the CS144 packages provide four independent $V_{CCO}$ supplies. The FG256 and the FG456 provide eight independent $V_{CCO}$ supplies.

Output buffers within a given $V_{CCO}$ bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the $V_{CCO}$ voltage for Input $V_{CCO}$ voltage.

### Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

### Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques:

None
Series
Parallel (Shunt)
Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None
Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 41.

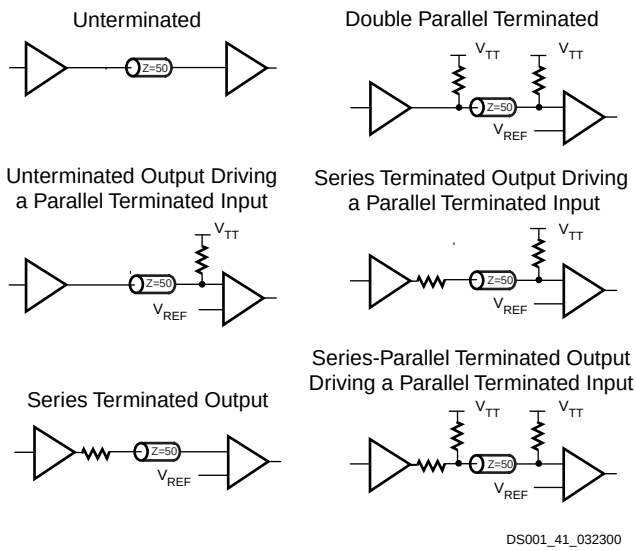



*Figure 41:* **Overview of Standard Input and Output Termination Methods**

### Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

### HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 45. DC voltage specifications appear in Table 23 for the HSTL_III standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

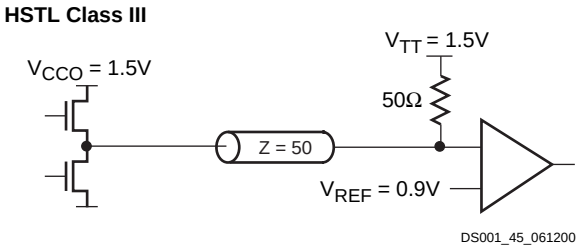



*Figure 45:* **Terminated HSTL Class III**

*Table 23:* **HSTL Class III Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ (1) | - | 0.90 | - |
| $V_{TT}$ | - | $V_{CCO}$ | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 | - | - |

**Notes:**

1. Per EIA/JESD8-6, "The value of $V_{REF}$ is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

### HSTL Class IV

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 46.DC voltage specifications appear in Table 23 for the HSTL_IV standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

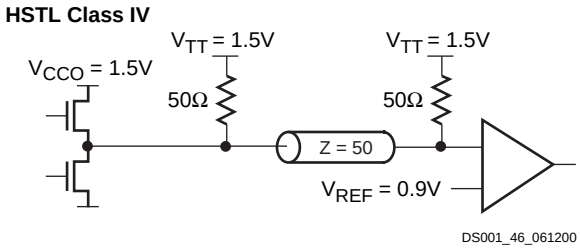



*Figure 46:* **Terminated HSTL Class IV**

*Table 24:* **HSTL Class IV Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ | - | 0.90 | - |
| $V_{TT}$ | - | $V_{CCO}$ | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 48 | - | - |

**Notes:**

1. Per EIA/JESD8-6, "The value of $V_{REF}$ is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

### CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 51. DC voltage specifications appear in Table 29 for the CTT standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics .

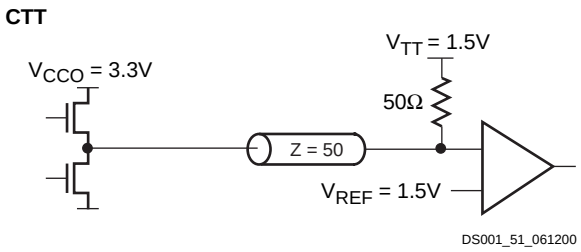



*Figure 51:* **Terminated CTT**

*Table 29:* **CTT Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.05(1) | 3.3 | 3.6 |
| $V_{REF}$ | 1.35 | 1.5 | 1.65 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.55 | 1.7 | - |
| $V_{IL} \leq V_{REF} - 0.2$ | - | 1.3 | 1.45 |
| $V_{OH} \geq V_{REF} + 0.4$ | 1.75 | 1.9 | - |
| $V_{OL} \leq V_{REF} - 0.4$ | - | 1.1 | 1.25 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

**Notes:**
1. Timing delays are calculated based on $V_{CCO}$ min of 3.0V.

### PCI33_3 and PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 30 for the PCI33_3 and PCI66_3 standards. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 30:* **PCI33_3 and PCI66_3 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH} = 0.5 \times V_{CCO}$ | 1.5 | 1.65 | $V_{CCO}$+ 0.5 |
| $V_{IL} = 0.3 \times V_{CCO}$ | –0.5 | 0.99 | 1.08 |
| $V_{OH} = 0.9 \times V_{CCO}$ | 2.7 | - | - |
| $V_{OL} = 0.1 \times V_{CCO}$ | - | - | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 1 | - | - |

**Notes:**
1. Tested according to the relevant specification.

### PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in Table 31 for the PCI33_5 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 31:* **PCI33_5 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.425 | 1.5 | 5.5 |
| $V_{IL}$ | –0.5 | 1.0 | 1.05 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.55 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 1 | - | - |

**Notes:**
1. Tested according to the relevant specification.

## CLB Distributed RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO16}$ | Clock CLK to X/Y outputs (WE active, 16 x 1 mode) | - | 2.2 | - | 2.6 | ns |
| $T_{SHCKO32}$ | Clock CLK to X/Y outputs (WE active, 32 x 1 mode) | - | 2.5 | - | 3.0 | ns |
| **Setup/Hold Times with Respect to Clock CLK**(1) | | | | | | |
| $T_{AS}$ / $T_{AH}$ | F/G address inputs | 0.7 / 0 | - | 0.7 / 0 | - | ns |
| $T_{DS}$ / $T_{DH}$ | BX/BY data inputs (DIN) | 0.8 / 0 | - | 0.9 / 0 | - | ns |
| $T_{WS}$ / $T_{WH}$ | CE input (WS) | 0.9 / 0 | - | 1.0 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{WPH}$ | Minimum pulse width, High | - | 2.9 | - | 2.9 | ns |
| $T_{WPL}$ | Minimum pulse width, Low | - | 2.9 | - | 2.9 | ns |
| $T_{WC}$ | Minimum clock period to meet address write cycle time | - | 5.8 | - | 5.8 | ns |

**Notes:**
1. A zero hold time listing indicates no hold time or a negative hold time.

## CLB Shift Register Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock CLK to X/Y outputs | - | 3.47 | - | 3.88 | ns |
| **Setup Times with Respect to Clock CLK** | | | | | | |
| $T_{SHDICK}$ | BX/BY data inputs (DIN) | 0.8 | - | 0.9 | - | ns |
| $T_{SHCECK}$ | CE input (WS) | 0.9 | - | 1.0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{SRPH}$ | Minimum pulse width, High | - | 2.9 | - | 2.9 | ns |
| $T_{SRPL}$ | Minimum pulse width, Low | - | 2.9 | - | 2.9 | ns |

## Introduction

This section describes how the various pins on a Spartan®-II FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-II FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

## Pin Types

Most pins on a Spartan-II FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-II FPGA packages, as outlined in Table 35.

*Table 35:* **Pin Definitions**

| Pin Name | Dedicated | Direction | Description |
|---|---|---|---|
| GCK0, GCK1, GCK2, GCK3 | No | Input | Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks. |
| M0, M1, M2 | Yes | Input | Mode pins are used to specify the configuration mode. |
| CCLK | Yes | Input or Output | The configuration Clock I/O pin. It is an input for slave-parallel and slave-serial modes, and output in master-serial mode. |
| $\overline{\text{PROGRAM}}$ | Yes | Input | Initiates a configuration sequence when asserted Low. |
| DONE | Yes | Bidirectional | Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain. |
| $\overline{\text{INIT}}$ | No | Bidirectional (Open-drain) | When Low, indicates that the configuration memory is being cleared. This pin becomes a user I/O after configuration. |
| BUSY/DOUT | No | Output | In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.<br>In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration. |
| D0/DIN, D1, D2, D3, D4, D5, D6, D7 | No | Input or Output | In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained.<br>In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration. |
| $\overline{\text{WRITE}}$ | No | Input | In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. |
| $\overline{\text{CS}}$ | No | Input | In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. |
| TDI, TDO, TMS, TCK | Yes | Mixed | Boundary Scan Test Access Port pins (IEEE 1149.1). |
| $V_{CCINT}$ | Yes | Input | Power supply pins for the internal core logic. |
| $V_{CCO}$ | Yes | Input | Power supply pins for output drivers (subject to banking rules) |
| $V_{REF}$ | No | Input | Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules). |
| GND | Yes | Input | Ground. |
| IRDY, TRDY | No | See PCI core documentation | These signals can only be accessed when using Xilinx® PCI cores. If the cores are not used, these pins are available as user I/Os. |

## Package Thermal Characteristics

Table 39 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance ($\theta_{JC}$) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board ($\theta_{JB}$) value similarly reports the difference between the board and junction temperature. The junction-to-ambient ($\theta_{JA}$) value reports the temperature difference between the ambient environment and the junction temperature. The $\theta_{JA}$ value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the $\theta_{JA}$ value in a system without a fan. The thermal resistance drops with increasing air flow.

*Table 39:* **Spartan-II Package Thermal Characteristics**

| Package | Device | Junction-to-Case ($\theta_{JC}$) | Junction-to-Board ($\theta_{JB}$) | Junction-to-Ambient ($\theta_{JA}$) at Different Air Flows | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Still Air (0 LFM) | 250 LFM | 500 LFM | 750 LFM | |
| VQ100 VQG100 | XC2S15 | 11.3 | N/A | 44.1 | 36.7 | 34.2 | 33.3 | °C/Watt |
| | XC2S30 | 10.1 | N/A | 40.7 | 33.9 | 31.5 | 30.8 | °C/Watt |
| TQ144 TQG144 | XC2S15 | 7.3 | N/A | 38.6 | 30.0 | 25.7 | 24.1 | °C/Watt |
| | XC2S30 | 6.7 | N/A | 34.7 | 27.0 | 23.1 | 21.7 | °C/Watt |
| | XC2S50 | 5.8 | N/A | 32.2 | 25.1 | 21.4 | 20.1 | °C/Watt |
| | XC2S100 | 5.3 | N/A | 31.4 | 24.4 | 20.9 | 19.6 | °C/Watt |
| CS144 CSG144 | XC2S30 | 2.8 | N/A | 34.0 | 26.0 | 23.9 | 23.2 | °C/Watt |
| PQ208 PQG208 | XC2S50 | 6.7 | N/A | 25.2 | 18.6 | 16.4 | 15.2 | °C/Watt |
| | XC2S100 | 5.9 | N/A | 24.6 | 18.1 | 16.0 | 14.9 | °C/Watt |
| | XC2S150 | 5.0 | N/A | 23.8 | 17.6 | 15.6 | 14.4 | °C/Watt |
| | XC2S200 | 4.1 | N/A | 23.0 | 17.0 | 15.0 | 13.9 | °C/Watt |
| FG256 FGG256 | XC2S50 | 7.1 | 17.6 | 27.2 | 21.4 | 20.3 | 19.8 | °C/Watt |
| | XC2S100 | 5.8 | 15.1 | 25.1 | 19.5 | 18.3 | 17.8 | °C/Watt |
| | XC2S150 | 4.6 | 12.7 | 23.0 | 17.6 | 16.3 | 15.8 | °C/Watt |
| | XC2S200 | 3.5 | 10.7 | 21.4 | 16.1 | 14.7 | 14.2 | °C/Watt |
| FG456 FGG456 | XC2S150 | 2.0 | N/A | 21.9 | 17.3 | 15.8 | 15.2 | °C/Watt |
| | XC2S200 | 2.0 | N/A | 21.0 | 16.6 | 15.1 | 14.5 | °C/Watt |

# Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan®-II device. They follow the pad locations around the die, and include Boundary Scan register locations.

## XC2S15 Device Pinouts

| XC2S15 Pad Name | | VQ100 | TQ144 | CS144 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| GND | - | P1 | P143 | A1 | - |
| TMS | - | P2 | P142 | B1 | - |
| I/O | 7 | P3 | P141 | C2 | 77 |
| I/O | 7 | - | P140 | C1 | 80 |
| I/O, $V_{REF}$ | 7 | P4 | P139 | D4 | 83 |
| I/O | 7 | P5 | P137 | D2 | 86 |
| I/O | 7 | P6 | P136 | D1 | 89 |
| GND | - | - | P135 | E4 | - |
| I/O | 7 | P7 | P134 | E3 | 92 |
| I/O | 7 | - | P133 | E2 | 95 |
| I/O, $V_{REF}$ | 7 | P8 | P132 | E1 | 98 |
| I/O | 7 | P9 | P131 | F4 | 101 |
| I/O | 7 | - | P130 | F3 | 104 |
| I/O, IRDY(1) | 7 | P10 | P129 | F2 | 107 |
| GND | - | P11 | P128 | F1 | - |
| $V_{CCO}$ | 7 | P12 | P127 | G2 | - |
| $V_{CCO}$ | 6 | P12 | P127 | G2 | - |
| I/O, TRDY(1) | 6 | P13 | P126 | G1 | 110 |
| $V_{CCINT}$ | - | P14 | P125 | G3 | - |
| I/O | 6 | - | P124 | G4 | 113 |
| I/O | 6 | P15 | P123 | H1 | 116 |
| I/O, $V_{REF}$ | 6 | P16 | P122 | H2 | 119 |
| I/O | 6 | - | P121 | H3 | 122 |
| I/O | 6 | P17 | P120 | H4 | 125 |
| GND | - | - | P119 | J1 | - |
| I/O | 6 | P18 | P118 | J2 | 128 |
| I/O | 6 | P19 | P117 | J3 | 131 |
| I/O, $V_{REF}$ | 6 | P20 | P115 | K1 | 134 |
| I/O | 6 | - | P114 | K2 | 137 |
| I/O | 6 | P21 | P113 | K3 | 140 |
| I/O | 6 | P22 | P112 | L1 | 143 |
| M1 | - | P23 | P111 | L2 | 146 |
| GND | - | P24 | P110 | L3 | - |
| M0 | - | P25 | P109 | M1 | 147 |
| $V_{CCO}$ | 6 | P26 | P108 | M2 | - |
| $V_{CCO}$ | 5 | P26 | P107 | N1 | - |

## XC2S15 Device Pinouts *(Continued)*

| XC2S15 Pad Name | | VQ100 | TQ144 | CS144 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| M2 | - | P27 | P106 | N2 | 148 |
| I/O | 5 | - | P103 | K4 | 155 |
| I/O, $V_{REF}$ | 5 | P30 | P102 | L4 | 158 |
| I/O | 5 | P31 | P100 | N4 | 161 |
| I/O | 5 | P32 | P99 | K5 | 164 |
| GND | - | - | P98 | L5 | - |
| $V_{CCINT}$ | - | P33 | P97 | M5 | - |
| I/O | 5 | - | P96 | N5 | 167 |
| I/O | 5 | - | P95 | K6 | 170 |
| I/O, $V_{REF}$ | 5 | P34 | P94 | L6 | 173 |
| I/O | 5 | - | P93 | M6 | 176 |
| $V_{CCINT}$ | - | P35 | P92 | N6 | - |
| I, GCK1 | 5 | P36 | P91 | M7 | 185 |
| $V_{CCO}$ | 5 | P37 | P90 | N7 | - |
| $V_{CCO}$ | 4 | P37 | P90 | N7 | - |
| GND | - | P38 | P89 | L7 | - |
| I, GCK0 | 4 | P39 | P88 | K7 | 186 |
| I/O | 4 | P40 | P87 | N8 | 190 |
| I/O | 4 | - | P86 | M8 | 193 |
| I/O, $V_{REF}$ | 4 | P41 | P85 | L8 | 196 |
| I/O | 4 | - | P84 | K8 | 199 |
| I/O | 4 | - | P83 | N9 | 202 |
| $V_{CCINT}$ | - | P42 | P82 | M9 | - |
| GND | - | - | P81 | L9 | - |
| I/O | 4 | P43 | P80 | K9 | 205 |
| I/O | 4 | P44 | P79 | N10 | 208 |
| I/O, $V_{REF}$ | 4 | P45 | P77 | L10 | 211 |
| I/O | 4 | - | P76 | N11 | 214 |
| I/O | 4 | P46 | P75 | M11 | 217 |
| I/O | 4 | P47 | P74 | L11 | 220 |
| GND | - | P48 | P73 | N12 | - |
| DONE | 3 | P49 | P72 | M12 | 223 |
| $V_{CCO}$ | 4 | P50 | P71 | N13 | - |
| $V_{CCO}$ | 3 | P50 | P70 | M13 | - |
| $\overline{PROGRAM}$ | - | P51 | P69 | L12 | 226 |
| I/O ($\overline{INIT}$) | 3 | P52 | P68 | L13 | 227 |
| I/O (D7) | 3 | P53 | P67 | K10 | 230 |
| I/O | 3 | - | P66 | K11 | 233 |
| I/O, $V_{REF}$ | 3 | P54 | P65 | K12 | 236 |
| I/O | 3 | P55 | P63 | J10 | 239 |
| I/O (D6) | 3 | P56 | P62 | J11 | 242 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| I/O | 4 | - | - | - | P87 | 295 |
| I/O | 4 | - | - | - | P88 | 298 |
| I/O | 4 | - | P84 | K8 | P89 | 301 |
| I/O | 4 | - | P83 | N9 | P90 | 304 |
| $V_{CCINT}$ | - | P42 | P82 | M9 | P91 | - |
| $V_{CCO}$ | 4 | - | - | - | P92 | - |
| GND | - | - | P81 | L9 | P93 | - |
| I/O | 4 | P43 | P80 | K9 | P94 | 307 |
| I/O | 4 | P44 | P79 | N10 | P95 | 310 |
| I/O | 4 | - | P78 | M10 | P96 | 313 |
| I/O, $V_{REF}$ | 4 | P45 | P77 | L10 | P98 | 316 |
| I/O | 4 | - | - | - | P99 | 319 |
| I/O | 4 | - | P76 | N11 | P100 | 322 |
| I/O | 4 | P46 | P75 | M11 | P101 | 325 |
| I/O | 4 | P47 | P74 | L11 | P102 | 328 |
| GND | - | P48 | P73 | N12 | P103 | - |
| DONE | 3 | P49 | P72 | M12 | P104 | 331 |
| $V_{CCO}$ | 4 | P50 | P71 | N13 | P105 | - |
| $V_{CCO}$ | 3 | P50 | P70 | M13 | P105 | - |
| $\overline{PROGRAM}$ | - | P51 | P69 | L12 | P106 | 334 |
| I/O ($\overline{INIT}$) | 3 | P52 | P68 | L13 | P107 | 335 |
| I/O (D7) | 3 | P53 | P67 | K10 | P108 | 338 |
| I/O | 3 | - | P66 | K11 | P109 | 341 |
| I/O | 3 | - | - | - | P110 | 344 |
| I/O, $V_{REF}$ | 3 | P54 | P65 | K12 | P111 | 347 |
| I/O | 3 | - | P64 | K13 | P113 | 350 |
| I/O | 3 | P55 | P63 | J10 | P114 | 353 |
| I/O (D6) | 3 | P56 | P62 | J11 | P115 | 356 |
| GND | - | - | P61 | J12 | P116 | - |
| $V_{CCO}$ | 3 | - | - | - | P117 | - |
| I/O (D5) | 3 | P57 | P60 | J13 | P119 | 359 |
| I/O | 3 | P58 | P59 | H10 | P120 | 362 |
| I/O | 3 | - | - | - | P121 | 365 |
| I/O | 3 | - | - | - | P122 | 368 |
| I/O | 3 | - | - | - | P123 | 371 |
| GND | - | - | - | - | P124 | - |
| I/O, $V_{REF}$ | 3 | P59 | P58 | H11 | P125 | 374 |
| I/O (D4) | 3 | P60 | P57 | H12 | P126 | 377 |
| I/O | 3 | - | P56 | H13 | P127 | 380 |
| $V_{CCINT}$ | - | P61 | P55 | G12 | P128 | - |
| I/O, TRDY(1) | 3 | P62 | P54 | G13 | P129 | 386 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| $V_{CCO}$ | 3 | P63 | P53 | G11 | P130 | - |
| $V_{CCO}$ | 2 | P63 | P53 | G11 | P130 | - |
| GND | - | P64 | P52 | G10 | P131 | - |
| I/O, IRDY(1) | 2 | P65 | P51 | F13 | P132 | 389 |
| I/O | 2 | - | - | - | P133 | 392 |
| I/O | 2 | - | P50 | F12 | P134 | 395 |
| I/O (D3) | 2 | P66 | P49 | F11 | P135 | 398 |
| I/O, $V_{REF}$ | 2 | P67 | P48 | F10 | P136 | 401 |
| GND | - | - | - | - | P137 | - |
| I/O | 2 | - | - | - | P138 | 404 |
| I/O | 2 | - | - | - | P139 | 407 |
| I/O | 2 | - | - | - | P140 | 410 |
| I/O | 2 | P68 | P47 | E13 | P141 | 413 |
| I/O (D2) | 2 | P69 | P46 | E12 | P142 | 416 |
| $V_{CCO}$ | 2 | - | - | - | P144 | - |
| GND | - | - | P45 | E11 | P145 | - |
| I/O (D1) | 2 | P70 | P44 | E10 | P146 | 419 |
| I/O | 2 | P71 | P43 | D13 | P147 | 422 |
| I/O | 2 | - | P42 | D12 | P148 | 425 |
| I/O, $V_{REF}$ | 2 | P72 | P41 | D11 | P150 | 428 |
| I/O | 2 | - | - | - | P151 | 431 |
| I/O | 2 | - | P40 | C13 | P152 | 434 |
| I/O (DIN, D0) | 2 | P73 | P39 | C12 | P153 | 437 |
| I/O (DOUT, BUSY) | 2 | P74 | P38 | C11 | P154 | 440 |
| CCLK | 2 | P75 | P37 | B13 | P155 | 443 |
| $V_{CCO}$ | 2 | P76 | P36 | B12 | P156 | - |
| $V_{CCO}$ | 1 | P76 | P35 | A13 | P156 | - |
| TDO | 2 | P77 | P34 | A12 | P157 | - |
| GND | - | P78 | P33 | B11 | P158 | - |
| TDI | - | P79 | P32 | A11 | P159 | - |
| I/O ($\overline{CS}$) | 1 | P80 | P31 | D10 | P160 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P81 | P30 | C10 | P161 | 3 |
| I/O | 1 | - | P29 | B10 | P162 | 6 |
| I/O | 1 | - | - | - | P163 | 9 |
| I/O, $V_{REF}$ | 1 | P82 | P28 | A10 | P164 | 12 |
| I/O | 1 | - | - | - | P166 | 15 |
| I/O | 1 | P83 | P27 | D9 | P167 | 18 |
| I/O | 1 | P84 | P26 | C9 | P168 | 21 |
| GND | - | - | P25 | B9 | P169 | - |
| $V_{CCO}$ | 1 | - | - | - | P170 | - |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| I/O | 0 | - | - | D8 | 83 |
| I/O | 0 | - | P188 | A6 | 86 |
| I/O, $V_{REF}$ | 0 | P12 | P189 | B7 | 89 |
| GND | - | - | P190 | GND* | - |
| I/O | 0 | - | P191 | C8 | 92 |
| I/O | 0 | - | P192 | D7 | 95 |
| I/O | 0 | - | P193 | E7 | 98 |
| I/O | 0 | P11 | P194 | C7 | 104 |
| I/O | 0 | P10 | P195 | B6 | 107 |
| $V_{CCINT}$ | - | P9 | P196 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 0 | - | P197 | $V_{CCO}$ Bank 0* | - |
| GND | - | P8 | P198 | GND* | - |
| I/O | 0 | P7 | P199 | A5 | 110 |
| I/O | 0 | P6 | P200 | C6 | 113 |
| I/O | 0 | - | P201 | B5 | 116 |
| I/O | 0 | - | - | D6 | 119 |
| I/O | 0 | - | P202 | A4 | 122 |
| I/O, $V_{REF}$ | 0 | P5 | P203 | B4 | 125 |
| GND | - | - | - | GND* | - |
| I/O | 0 | - | P204 | E6 | 128 |
| I/O | 0 | - | - | D5 | 131 |
| I/O | 0 | P4 | P205 | A3 | 134 |
| I/O | 0 | - | - | C5 | 137 |
| I/O | 0 | P3 | P206 | B3 | 140 |
| TCK | - | P2 | P207 | C4 | - |
| $V_{CCO}$ | 0 | P1 | P208 | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P144 | P208 | $V_{CCO}$ Bank 7* | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S50 Package Pins

**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P104 | P105 | - | - | - | - |

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## Additional XC2S100 Package Pins

**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P104 | P105 | - | - | - | - |

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**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

11/02/00

**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

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**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |

## Additional XC2S100 Package Pins *(Continued)*

| | | | | | |
|---|---|---|---|---|---|
| F10 | F7 | F8 | F9 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U10 | U7 | U8 | U9 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A4 | A5 | A6 | A12 | A13 |
| A14 | A15 | A17 | B3 | B6 | B8 |
| B11 | B14 | B16 | B19 | C1 | C2 |
| C8 | C9 | C12 | C18 | C22 | D1 |
| D4 | D5 | D10 | D18 | D19 | D21 |
| E4 | E11 | E13 | E15 | E16 | E17 |
| E19 | E22 | F4 | F11 | F22 | G2 |
| G3 | G4 | G19 | G22 | H1 | H21 |
| J1 | J3 | J4 | J19 | J20 | K2 |
| K18 | K19 | L2 | L5 | L18 | L19 |
| M2 | M6 | M17 | M18 | M21 | N1 |
| N5 | N19 | P1 | P5 | P19 | P22 |
| R1 | R3 | R20 | R22 | T5 | T19 |
| U3 | U11 | U18 | V1 | V2 | V10 |
| V12 | V17 | V3 | V4 | V6 | V8 |
| V20 | V21 | V22 | W4 | W5 | W9 |
| W13 | W14 | W15 | W16 | W19 | Y5 |
| Y14 | Y18 | Y22 | AA1 | AA3 | AA6 |
| AA9 | AA10 | AA11 | AA16 | AA17 | AA18 |
| AA22 | AB3 | AB4 | AB7 | AB8 | AB12 |
| AB14 | AB21 | - | - | - | - |

11/02/00

## XC2S200 Device Pinouts

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| GND | - | P1 | GND* | GND* | - |
| TMS | - | P2 | D3 | D3 | - |
| I/O | 7 | P3 | C2 | B1 | 257 |
| I/O | 7 | - | - | E4 | 263 |
| I/O | 7 | - | - | C1 | 266 |
| I/O | 7 | - | A2 | F5 | 269 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 7 | P4 | B1 | D2 | 272 |
| I/O | 7 | - | - | E3 | 275 |
| I/O | 7 | - | - | F4 | 281 |
| GND | - | - | GND* | GND* | - |
| I/O | 7 | - | E3 | G5 | 284 |
| I/O | 7 | P5 | D2 | F3 | 287 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 7 | - | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| I/O, $V_{REF}$ | 7 | P6 | C1 | E2 | 290 |
| I/O | 7 | P7 | F3 | E1 | 293 |
| I/O | 7 | - | - | G4 | 296 |
| I/O | 7 | - | - | G3 | 299 |
| I/O | 7 | - | E2 | H5 | 302 |
| GND | - | - | GND* | GND* | - |
| I/O | 7 | P8 | E4 | F2 | 305 |
| I/O | 7 | - | - | F1 | 308 |
| I/O, $V_{REF}$ | 7 | P9 | D1 | H4 | 314 |
| I/O | 7 | P10 | E1 | G1 | 317 |
| GND | - | P11 | GND* | GND* | - |
| $V_{CCO}$ | 7 | P12 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| $V_{CCINT}$ | - | P13 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 7 | P14 | F2 | H3 | 320 |
| I/O | 7 | P15 | G3 | H2 | 323 |
| I/O | 7 | - | - | J4 | 326 |
| I/O | 7 | - | - | H1 | 329 |
| I/O | 7 | - | F1 | J5 | 332 |
| GND | - | - | GND* | GND* | - |
| I/O | 7 | P16 | F4 | J2 | 335 |
| I/O | 7 | - | - | J3 | 338 |
| I/O | 7 | - | - | J1 | 341 |
| I/O | 7 | P17 | F5 | K5 | 344 |
| I/O | 7 | P18 | G2 | K1 | 347 |
| GND | - | P19 | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 7 | - | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| I/O, $V_{REF}$ | 7 | P20 | H3 | K3 | 350 |
| I/O | 7 | P21 | G4 | K4 | 353 |
| I/O | 7 | - | - | K2 | 359 |
| I/O | 7 | - | H2 | L6 | 362 |
| I/O | 7 | P22 | G5 | L1 | 365 |
| I/O | 7 | - | - | L5 | 368 |
| I/O | 7 | P23 | H4 | L4 | 374 |
| I/O, IRDY(1) | 7 | P24 | G1 | L3 | 377 |
| GND | - | P25 | GND* | GND* | - |
| $V_{CCO}$ | 7 | P26 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |
| $V_{CCO}$ | 6 | P26 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| I/O, TRDY(1) | 6 | P27 | J2 | M1 | 380 |
| $V_{CCINT}$ | - | P28 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 6 | - | - | M6 | 389 |
| I/O | 6 | P29 | H1 | M3 | 392 |
| I/O | 6 | - | J4 | M4 | 395 |
| I/O | 6 | - | - | N1 | 398 |
| I/O | 6 | P30 | J1 | M5 | 404 |
| I/O, $V_{REF}$ | 6 | P31 | J3 | N2 | 407 |
| $V_{CCO}$ | 6 | - | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | P32 | GND* | GND* | - |
| I/O | 6 | P33 | K5 | N3 | 410 |
| I/O | 6 | P34 | K2 | N4 | 413 |
| I/O | 6 | - | - | P1 | 416 |
| I/O | 6 | - | - | N5 | 419 |
| I/O | 6 | P35 | K1 | P2 | 422 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | K3 | P4 | 425 |
| I/O | 6 | - | - | R1 | 428 |
| I/O | 6 | - | - | P5 | 431 |
| I/O | 6 | P36 | L1 | P3 | 434 |
| I/O | 6 | P37 | L2 | R2 | 437 |
| $V_{CCINT}$ | - | P38 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 6 | P39 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | P40 | GND* | GND* | - |
| I/O | 6 | P41 | K4 | T1 | 440 |
| I/O, $V_{REF}$ | 6 | P42 | M1 | R4 | 443 |