# AMD Xilinx - XC2S100-5PQ208C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 600 |
| Number of Logic Elements/Cells | 2700 |
| Total RAM Bits | 40960 |
| Number of I/O | 140 |
| Number of Gates | 100000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s100-5pq208c |

Email: info@E-XFL.COM
Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 7 lists the boundary-scan instructions supported in Spartan-II FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

*Table 7:* **Boundary-Scan Instructions**

| Boundary-Scan Command | Binary Code[4:0] | Description |
|---|---|---|
| EXTEST | 00000 | Enables boundary-scan EXTEST operation |
| SAMPLE | 00001 | Enables boundary-scan SAMPLE operation |
| USR1 | 00010 | Access user-defined register 1 |
| USR2 | 00011 | Access user-defined register 2 |
| CFG_OUT | 00100 | Access the configuration bus for Readback |
| CFG_IN | 00101 | Access the configuration bus for Configuration |
| INTEST | 00111 | Enables boundary-scan INTEST operation |
| USRCODE | 01000 | Enables shifting out USER code |
| IDCODE | 01001 | Enables shifting out of ID Code |
| HIZ | 01010 | Disables output pins while enabling the Bypass Register |
| JSTART | 01100 | Clock the start-up sequence when StartupClk is TCK |
| BYPASS | 11111 | Enables BYPASS |
| RESERVED | All other codes | Xilinx® reserved instructions |

The public boundary-scan instructions are available prior to configuration. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

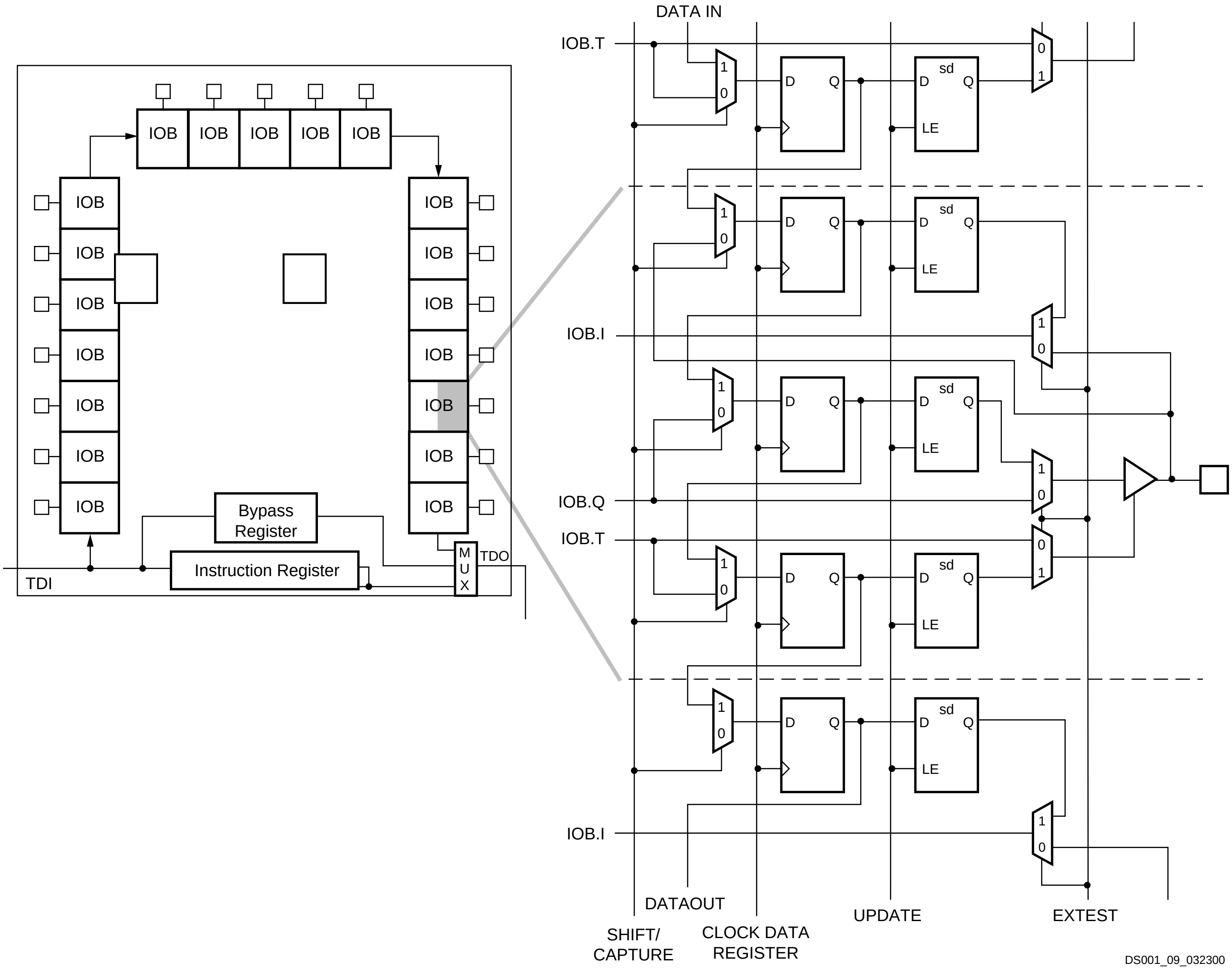

*Figure 9:* **Spartan-II Family Boundary Scan Logic**

### *Bit Sequence*

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the Downloads area.

# Configuration

Configuration is the process by which the bitstream of a design, as generated by the Xilinx software, is loaded into the internal configuration memory of the FPGA. Spartan-II devices support both serial configuration, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

## Configuration File

Spartan-II devices are configured by sequentially loading frames of data that have been concatenated into a configuration file. Table 8 shows how much nonvolatile storage space is needed for Spartan-II devices.

It is important to note that, while a PROM is commonly used to store configuration data before loading them into the FPGA, it is by no means required. Any of a number of different kinds of under populated nonvolatile storage already available either on or off the board (i.e., hard drives, FLASH cards, etc.) can be used. For more information on configuration without a PROM, refer to XAPP098, *The Low-Cost, Efficient Serial Configuration of Spartan FPGAs*.

*Table 8:* **Spartan-II Configuration File Size**

| Device | Configuration File Size (Bits) |
|---|---|
| XC2S15 | 197,696 |
| XC2S30 | 336,768 |
| XC2S50 | 559,200 |
| XC2S100 | 781,216 |
| XC2S150 | 1,040,096 |
| XC2S200 | 1,335,840 |

## Modes

Spartan-II devices support the following four configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to the end of configuration. The selection codes are listed in Table 9.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

*Table 9:* **Configuration Modes**

| Configuration Mode | Preconfiguration Pull-ups | M0 | M1 | M2 | CCLK Direction | Data Width | Serial $D_{OUT}$ |
|---|---|---|---|---|---|---|---|
| Master Serial mode | No | 0 | 0 | 0 | Out | 1 | Yes |
| | Yes | 0 | 0 | 1 | | | |
| Slave Parallel mode | Yes | 0 | 1 | 0 | In | 8 | No |
| | No | 0 | 1 | 1 | | | |
| Boundary-Scan mode | Yes | 1 | 0 | 0 | N/A | 1 | No |
| | No | 1 | 0 | 1 | | | |
| Slave Serial mode | Yes | 1 | 1 | 0 | In | 1 | Yes |
| | No | 1 | 1 | 1 | | | |

**Notes:**

1. During power-on and throughout configuration, the I/O drivers will be in a high-impedance state. After configuration, all unused I/Os (those not assigned signals) will remain in a high-impedance state. Pins used as outputs may pulse High at the end of configuration (see Answer 10504).
2. If the Mode pins are set for preconfiguration pull-ups, those resistors go into effect once the rising edge of INIT samples the Mode pins. They will stay in effect until GTS is released during startup, after which the UnusedPin bitstream generator option will determine whether the unused I/Os have a pull-up, pull-down, or no resistor.

## Creating Larger RAM Structures

The block RAM columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

## Location Constraints

Block RAM instances can have LOC properties attached to them to constrain the placement. The block RAM placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form:

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

## Conflict Resolution

The block RAM memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
  - The write succeeds
  - The data out on the writing port accurately reflects the data written.
  - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

### *Single Port Timing*

Figure 33 shows a timing diagram for a single port of a block RAM memory. The block RAM AC switching characteristics are specified in the data sheet. The block RAM memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the block RAM memory is now disabled. The DO bus retains the last value.

### *Dual Port Timing*

Figure 34 shows a timing diagram for a true dual-port read/write block RAM memory. The clock on port A has a longer period than the clock on Port B. The timing parameter $T_{BCCS}$, (clock-to-clock setup) is shown on this diagram. The parameter, $T_{BCCS}$ is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

$T_{BCCS}$ is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location will be invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory will be correct, but the read port will have invalid data. At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the $T_{BCCS}$ parameter and the DOB reflects the new memory values written by Port A.

At the third rising edge of CLKA, the $T_{BCCS}$ parameter is violated with two writes to memory location 0x0F. The DOA and DOB busses reflect the contents of the DIA and DIB busses, but the stored value at 0x7E is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the $T_{BCCS}$ parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

### Initialization

The block RAM memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 14. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

### Initialization in VHDL

The block RAM structures may be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization.

### Initialization in Verilog

The block RAM structures may be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization.

### Block Memory Generation

The CORE Generator™ software generates memory structures using the block RAM features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

*Table 14:* **RAM Initialization Properties**

| Property | Memory Cells |
|---|---|
| INIT_00 | 255 to 0 |
| INIT_01 | 511 to 256 |
| INIT_02 | 767 to 512 |
| INIT_03 | 1023 to 768 |
| INIT_04 | 1279 to 1024 |
| INIT_05 | 1535 to 1280 |
| INIT_06 | 1791 to 1536 |
| INIT_07 | 2047 to 1792 |
| INIT_08 | 2303 to 2048 |
| INIT_09 | 2559 to 2304 |
| INIT_0a | 2815 to 2560 |
| INIT_0b | 3071 to 2816 |
| INIT_0c | 3327 to 3072 |
| INIT_0d | 3583 to 3328 |
| INIT_0e | 3839 to 3584 |
| INIT_0f | 4095 to 3840 |

For design examples and more information on using the Block RAM, see XAPP173, *Using Block SelectRAM+ Memory in Spartan-II FPGAs*.

## Using Versatile I/O

The Spartan-II FPGA family includes a highly configurable, high-performance I/O resource called Versatile I/O to provide support for a wide variety of I/O standards. The Versatile I/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and Versatile I/O features and the design considerations described in this document can improve and simplify system level design.

### Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high-performance I/O becomes more important. While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. Versatile I/O, the revolutionary input/output resources of Spartan-II devices, has resolved this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. The Spartan-II FPGA Versatile I/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each Versatile I/O block can support up to 16 I/O standards. Supporting such a variety of I/O standards allows the

### GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 42. Table 20 lists DC voltage specifications for the GTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

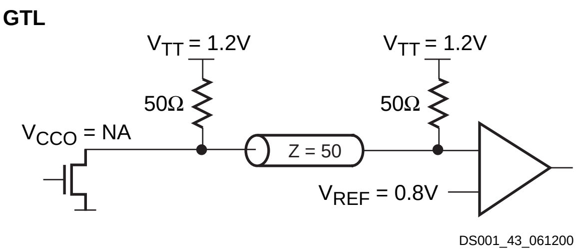

*Figure 42:* **Terminated GTL**

*Table 20:* **GTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | N/A | - |
| $V_{REF} = N \times V_{TT}^{(1)}$ | 0.74 | 0.8 | 0.86 |
| $V_{TT}$ | 1.14 | 1.2 | 1.26 |
| $V_{IH} \geq V_{REF} + 0.05$ | 0.79 | 0.85 | - |
| $V_{IL} \leq V_{REF} - 0.05$ | - | 0.75 | 0.81 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | - | 0.2 | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | - | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) at 0.4V | 32 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) at 0.2V | - | - | 40 |

**Notes:**

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

### GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 43. DC voltage specifications appear in Table 21 for the GTL+ standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

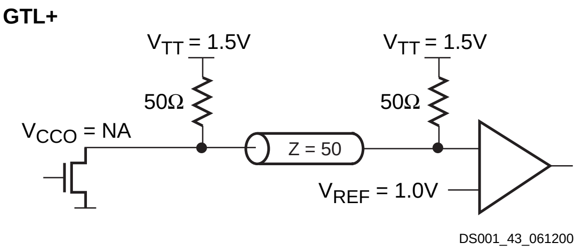

*Figure 43:* **Terminated GTL+**

*Table 21:* **GTL+ Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | - | - |
| $V_{REF} = N \times V_{TT}^{(1)}$ | 0.88 | 1.0 | 1.12 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} \geq V_{REF} + 0.1$ | 0.98 | 1.1 | - |
| $V_{IL} \leq V_{REF} - 0.1$ | - | 0.9 | 1.02 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | 0.3 | 0.45 | 0.6 |
| $I_{OH}$ at $V_{OH}$ (mA) | - | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) at 0.6V | 36 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) at 0.3V | - | - | 48 |

**Notes:**

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

### HSTL Class I

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 44. DC voltage specifications appear in Table 22 for the HSTL_1 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

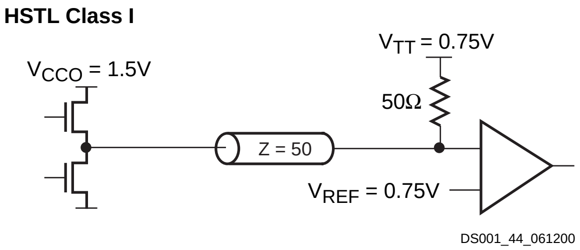

*Figure 44:* **Terminated HSTL Class I**

*Table 22:* **HSTL Class I Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ | 0.68 | 0.75 | 0.90 |
| $V_{TT}$ | - | $V_{CCO} \times 0.5$ | - |
| $V_{IH}$ | $V_{REF} + 0.1$ | - | - |
| $V_{IL}$ | - | - | $V_{REF} - 0.1$ |
| $V_{OH}$ | $V_{CCO} - 0.4$ | - | - |
| $V_{OL}$ | | | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

### CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 51. DC voltage specifications appear in Table 29 for the CTT standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics .

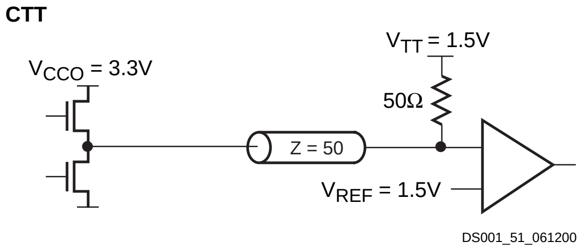

*Figure 51:* **Terminated CTT**

*Table 29:* **CTT Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.05(1) | 3.3 | 3.6 |
| $V_{REF}$ | 1.35 | 1.5 | 1.65 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.55 | 1.7 | - |
| $V_{IL} \leq V_{REF} - 0.2$ | - | 1.3 | 1.45 |
| $V_{OH} \geq V_{REF} + 0.4$ | 1.75 | 1.9 | - |
| $V_{OL} \leq V_{REF} - 0.4$ | - | 1.1 | 1.25 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

**Notes:**

1. Timing delays are calculated based on $V_{CCO}$ min of 3.0V.

### PCI33_3 and PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 30 for the PCI33_3 and PCI66_3 standards. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 30:* **PCI33_3 and PCI66_3 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH} = 0.5 \times V_{CCO}$ | 1.5 | 1.65 | $V_{CCO}$+ 0.5 |
| $V_{IL} = 0.3 \times V_{CCO}$ | –0.5 | 0.99 | 1.08 |
| $V_{OH} = 0.9 \times V_{CCO}$ | 2.7 | - | - |
| $V_{OL} = 0.1 \times V_{CCO}$ | - | - | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 1 | - | - |

**Notes:**

1. Tested according to the relevant specification.

### PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in Table 31 for the PCI33_5 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 31:* **PCI33_5 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.425 | 1.5 | 5.5 |
| $V_{IL}$ | –0.5 | 1.0 | 1.05 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.55 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 1 | - | - |

**Notes:**

1. Tested according to the relevant specification.

## IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Delay Adjustments for Different Standards," page 57.

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -6 | | -5 | | |
| | | | Min | Max | Min | Max | |
| **Propagation Delays** | | | | | | | |
| $T_{IOPI}$ | Pad to I output, no delay | All | - | 0.8 | - | 1.0 | ns |
| $T_{IOPID}$ | Pad to I output, with delay | All | - | 1.5 | - | 1.8 | ns |
| $T_{IOPLI}$ | Pad to output IQ via transparent latch, no delay | All | - | 1.7 | - | 2.0 | ns |
| $T_{IOPLID}$ | Pad to output IQ via transparent latch, with delay | XC2S15 | - | 3.8 | - | 4.5 | ns |
| | | XC2S30 | - | 3.8 | - | 4.5 | ns |
| | | XC2S50 | - | 3.8 | - | 4.5 | ns |
| | | XC2S100 | - | 3.8 | - | 4.5 | ns |
| | | XC2S150 | - | 4.0 | - | 4.7 | ns |
| | | XC2S200 | - | 4.0 | - | 4.7 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{IOCKIQ}$ | Clock CLK to output IQ | All | - | 0.7 | - | 0.8 | ns |
| **Setup/Hold Times with Respect to Clock CLK(2)** | | | | | | | |
| $T_{IOPICK}$ / $T_{IOICKP}$ | Pad, no delay | All | 1.7 / 0 | - | 1.9 / 0 | - | ns |
| $T_{IOPICKD}$ / $T_{IOICKPD}$ | Pad, with delay(1) | XC2S15 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S30 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S50 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S100 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S150 | 3.9 / 0 | - | 4.6 / 0 | - | ns |
| | | XC2S200 | 3.9 / 0 | - | 4.6 / 0 | - | ns |
| $T_{IOICECK}$ / $T_{IOCKICE}$ | ICE input | All | 0.9 / 0.01 | - | 0.9 / 0.01 | - | ns |
| **Set/Reset Delays** | | | | | | | |
| $T_{IOSRCKI}$ | SR input (IFF, synchronous) | All | - | 1.1 | - | 1.2 | ns |
| $T_{IOSRIQ}$ | SR input to IQ (asynchronous) | All | - | 1.5 | - | 1.7 | ns |
| $T_{GSRQ}$ | GSR to output IQ | All | - | 9.9 | - | 11.7 | ns |

**Notes:**

1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.
2. A zero hold time listing indicates no hold time or a negative hold time.

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | 4-input function: F/G inputs to X/Y outputs | - | 0.6 | - | 0.7 | ns |
| $T_{IF5}$ | 5-input function: F/G inputs to F5 output | - | 0.7 | - | 0.9 | ns |
| $T_{IF5X}$ | 5-input function: F/G inputs to X output | - | 0.9 | - | 1.1 | ns |
| $T_{IF6Y}$ | 6-input function: F/G inputs to Y output via F6 MUX | - | 1.0 | - | 1.1 | ns |
| $T_{F5INY}$ | 6-input function: F5IN input to Y output | - | 0.4 | - | 0.4 | ns |
| $T_{IFNCTL}$ | Incremental delay routing through transparent latch to XQ/YQ outputs | - | 0.7 | - | 0.9 | ns |
| $T_{BYYB}$ | BY input to YB output | - | 0.6 | - | 0.7 | ns |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | FF clock CLK to XQ/YQ outputs | - | 1.1 | - | 1.3 | ns |
| $T_{CKLO}$ | Latch clock CLK to XQ/YQ outputs | - | 1.2 | - | 1.5 | ns |
| **Setup/Hold Times with Respect to Clock CLK**(1) | | | | | | |
| $T_{ICK}$ / $T_{CKI}$ | 4-input function: F/G inputs | 1.3 / 0 | - | 1.4 / 0 | - | ns |
| $T_{IF5CK}$ / $T_{CKIF5}$ | 5-input function: F/G inputs | 1.6 / 0 | - | 1.8 / 0 | - | ns |
| $T_{F5INCK}$ / $T_{CKF5IN}$ | 6-input function: F5IN input | 1.0 / 0 | - | 1.1 / 0 | - | ns |
| $T_{IF6CK}$ / $T_{CKIF6}$ | 6-input function: F/G inputs via F6 MUX | 1.6 / 0 | - | 1.8 / 0 | - | ns |
| $T_{DICK}$ / $T_{CKDI}$ | BX/BY inputs | 0.8 / 0 | - | 0.8 / 0 | - | ns |
| $T_{CECK}$ / $T_{CKCE}$ | CE input | 0.9 / 0 | - | 0.9 / 0 | - | ns |
| $T_{RCK}$ / $T_{CKR}$ | SR/BY inputs (synchronous) | 0.8 / 0 | - | 0.8 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{CH}$ | Minimum pulse width, High | - | 1.9 | - | 1.9 | ns |
| $T_{CL}$ | Minimum pulse width, Low | - | 1.9 | - | 1.9 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW}$ | Minimum pulse width, SR/BY inputs | 3.1 | - | 3.1 | - | ns |
| $T_{RQ}$ | Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | - | 1.1 | - | 1.3 | ns |
| $T_{IOGSRQ}$ | Delay from GSR to XQ/YQ outputs | - | 9.9 | - | 11.7 | ns |
| $F_{TOG}$ | Toggle frequency (for export control) | - | 263 | - | 263 | MHz |

**Notes:**

1. A zero hold time listing indicates no hold time or a negative hold time.

# Revision History

| Date | Version No. | Description |
|---|---|---|
| 09/18/00 | 2.0 | Sectioned the Spartan-II Family data sheet into four modules. Updated timing to reflect the latest speed files. Added current supply numbers and XC2S200 -5 timing numbers. Approved -5 timing numbers as preliminary information with exceptions as noted. |
| 11/02/00 | 2.1 | Removed Power Down feature. |
| 01/19/01 | 2.2 | DC and timing numbers updated to Preliminary for the XC2S50 and XC2S100. Industrial power-on current specifications and -6 DLL timing numbers added. Power-on specification clarified. |
| 03/09/01 | 2.3 | Added note on power sequencing. Clarified power-on current requirement. |
| 08/28/01 | 2.4 | Added -6 preliminary timing. Added typical and industrial standby current numbers. Specified min. power-on current by junction temperature instead of by device type (Commercial vs. Industrial). Eliminated minimum $V_{CCINT}$ ramp time requirement. Removed footnote limiting DLL operation to the Commercial temperature range. |
| 07/26/02 | 2.5 | Clarified that I/O leakage current is specified over the Recommended Operating Conditions for $V_{CCINT}$ and $V_{CCO}$. |
| 08/26/02 | 2.6 | Added references for XAPP450 to Power-On Current Specification. |
| 09/03/03 | 2.7 | Added relaxed minimum power-on current ($I_{CCPO}$) requirements to page 53. On page 64, moved $T_{RPW}$ values from maximum to minimum column. |
| 06/13/08 | 2.8 | Updated I/O measurement thresholds. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |

## XC2S30 Device Pinouts

| XC2S30 Pad Name | | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
|---|---|---|---|---|---|---|
| **Function** | **Bank** | | | | | |
| GND | - | P1 | P143 | A1 | P1 | - |
| TMS | - | P2 | P142 | B1 | P2 | - |
| I/O | 7 | P3 | P141 | C2 | P3 | 113 |
| I/O | 7 | - | P140 | C1 | P4 | 116 |
| I/O | 7 | - | - | - | P5 | 119 |
| I/O, $V_{REF}$ | 7 | P4 | P139 | D4 | P6 | 122 |
| I/O | 7 | - | P138 | D3 | P8 | 125 |
| I/O | 7 | P5 | P137 | D2 | P9 | 128 |
| I/O | 7 | P6 | P136 | D1 | P10 | 131 |
| GND | - | - | P135 | E4 | P11 | - |
| $V_{CCO}$ | 7 | - | - | - | P12 | - |
| I/O | 7 | P7 | P134 | E3 | P14 | 134 |
| I/O | 7 | - | P133 | E2 | P15 | 137 |
| I/O | 7 | - | - | - | P16 | 140 |
| I/O | 7 | - | - | - | P17 | 143 |
| I/O | 7 | - | - | - | P18 | 146 |
| GND | - | - | - | - | P19 | - |
| I/O, $V_{REF}$ | 7 | P8 | P132 | E1 | P20 | 149 |
| I/O | 7 | P9 | P131 | F4 | P21 | 152 |
| I/O | 7 | - | P130 | F3 | P22 | 155 |
| I/O | 7 | - | - | - | P23 | 158 |
| I/O, IRDY(1) | 7 | P10 | P129 | F2 | P24 | 161 |
| GND | - | P11 | P128 | F1 | P25 | - |
| $V_{CCO}$ | 7 | P12 | P127 | G2 | P26 | - |
| $V_{CCO}$ | 6 | P12 | P127 | G2 | P26 | - |
| I/O, TRDY(1) | 6 | P13 | P126 | G1 | P27 | 164 |
| $V_{CCINT}$ | - | P14 | P125 | G3 | P28 | - |
| I/O | 6 | - | P124 | G4 | P29 | 170 |
| I/O | 6 | P15 | P123 | H1 | P30 | 173 |
| I/O, $V_{REF}$ | 6 | P16 | P122 | H2 | P31 | 176 |
| GND | - | - | - | - | P32 | - |
| I/O | 6 | - | - | - | P33 | 179 |
| I/O | 6 | - | - | - | P34 | 182 |
| I/O | 6 | - | - | - | P35 | 185 |
| I/O | 6 | - | P121 | H3 | P36 | 188 |
| I/O | 6 | P17 | P120 | H4 | P37 | 191 |
| $V_{CCO}$ | 6 | - | - | - | P39 | - |
| GND | - | - | P119 | J1 | P40 | - |
| I/O | 6 | P18 | P118 | J2 | P41 | 194 |
| I/O | 6 | P19 | P117 | J3 | P42 | 197 |
| I/O | 6 | - | P116 | J4 | P43 | 200 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
|---|---|---|---|---|---|---|
| **Function** | **Bank** | | | | | |
| I/O, $V_{REF}$ | 6 | P20 | P115 | K1 | P45 | 203 |
| I/O | 6 | - | - | - | P46 | 206 |
| I/O | 6 | - | P114 | K2 | P47 | 209 |
| I/O | 6 | P21 | P113 | K3 | P48 | 212 |
| I/O | 6 | P22 | P112 | L1 | P49 | 215 |
| M1 | - | P23 | P111 | L2 | P50 | 218 |
| GND | - | P24 | P110 | L3 | P51 | - |
| M0 | - | P25 | P109 | M1 | P52 | 219 |
| $V_{CCO}$ | 6 | P26 | P108 | M2 | P53 | - |
| $V_{CCO}$ | 5 | P26 | P107 | N1 | P53 | - |
| M2 | - | P27 | P106 | N2 | P54 | 220 |
| I/O | 5 | - | P103 | K4 | P57 | 227 |
| I/O | 5 | - | - | - | P58 | 230 |
| I/O, $V_{REF}$ | 5 | P30 | P102 | L4 | P59 | 233 |
| I/O | 5 | - | P101 | M4 | P61 | 236 |
| I/O | 5 | P31 | P100 | N4 | P62 | 239 |
| I/O | 5 | P32 | P99 | K5 | P63 | 242 |
| GND | - | - | P98 | L5 | P64 | - |
| $V_{CCO}$ | 5 | - | - | - | P65 | - |
| $V_{CCINT}$ | - | P33 | P97 | M5 | P66 | - |
| I/O | 5 | - | P96 | N5 | P67 | 245 |
| I/O | 5 | - | P95 | K6 | P68 | 248 |
| I/O | 5 | - | - | - | P69 | 251 |
| I/O | 5 | - | - | - | P70 | 254 |
| I/O | 5 | - | - | - | P71 | 257 |
| GND | - | - | - | - | P72 | - |
| I/O, $V_{REF}$ | 5 | P34 | P94 | L6 | P73 | 260 |
| I/O | 5 | - | - | - | P74 | 263 |
| I/O | 5 | - | P93 | M6 | P75 | 266 |
| $V_{CCINT}$ | - | P35 | P92 | N6 | P76 | - |
| I, GCK1 | 5 | P36 | P91 | M7 | P77 | 275 |
| $V_{CCO}$ | 5 | P37 | P90 | N7 | P78 | - |
| $V_{CCO}$ | 4 | P37 | P90 | N7 | P78 | - |
| GND | - | P38 | P89 | L7 | P79 | - |
| I, GCK0 | 4 | P39 | P88 | K7 | P80 | 276 |
| I/O | 4 | P40 | P87 | N8 | P81 | 280 |
| I/O | 4 | - | P86 | M8 | P82 | 283 |
| I/O | 4 | - | - | - | P83 | 286 |
| I/O, $V_{REF}$ | 4 | P41 | P85 | L8 | P84 | 289 |
| GND | - | - | - | - | P85 | - |
| I/O | 4 | - | - | - | P86 | 292 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| $V_{CCINT}$ | - | P85 | P24 | A9 | P171 | - |
| I/O | 1 | - | P23 | D8 | P172 | 24 |
| I/O | 1 | - | P22 | C8 | P173 | 27 |
| I/O | 1 | - | - | - | P174 | 30 |
| I/O | 1 | - | - | - | P175 | 33 |
| I/O | 1 | - | - | - | P176 | 36 |
| GND | - | - | - | - | P177 | - |
| I/O, $V_{REF}$ | 1 | P86 | P21 | B8 | P178 | 39 |
| I/O | 1 | - | - | - | P179 | 42 |
| I/O | 1 | - | P20 | A8 | P180 | 45 |
| I/O | 1 | P87 | P19 | B7 | P181 | 48 |
| I, GCK2 | 1 | P88 | P18 | A7 | P182 | 54 |
| GND | - | P89 | P17 | C7 | P183 | - |
| $V_{CCO}$ | 1 | P90 | P16 | D7 | P184 | - |
| $V_{CCO}$ | 0 | P90 | P16 | D7 | P184 | - |
| I, GCK3 | 0 | P91 | P15 | A6 | P185 | 55 |
| $V_{CCINT}$ | - | P92 | P14 | B6 | P186 | - |
| I/O | 0 | - | P13 | C6 | P187 | 62 |
| I/O | 0 | - | - | - | P188 | 65 |
| I/O, $V_{REF}$ | 0 | P93 | P12 | D6 | P189 | 68 |
| GND | - | - | - | - | P190 | - |
| I/O | 0 | - | - | - | P191 | 71 |
| I/O | 0 | - | - | - | P192 | 74 |
| I/O | 0 | - | - | - | P193 | 77 |
| I/O | 0 | - | P11 | A5 | P194 | 80 |
| I/O | 0 | - | P10 | B5 | P195 | 83 |
| $V_{CCINT}$ | - | P94 | P9 | C5 | P196 | - |
| $V_{CCO}$ | 0 | - | - | - | P197 | - |
| GND | - | - | P8 | D5 | P198 | - |
| I/O | 0 | P95 | P7 | A4 | P199 | 86 |
| I/O | 0 | P96 | P6 | B4 | P200 | 89 |
| I/O | 0 | - | - | - | P201 | 92 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| I/O, $V_{REF}$ | 0 | P97 | P5 | C4 | P203 | 95 |
| I/O | 0 | - | - | - | P204 | 98 |
| I/O | 0 | - | P4 | A3 | P205 | 101 |
| I/O | 0 | P98 | P3 | B3 | P206 | 104 |
| TCK | - | P99 | P2 | C3 | P207 | - |
| $V_{CCO}$ | 0 | P100 | P1 | A2 | P208 | - |
| $V_{CCO}$ | 7 | P100 | P144 | B2 | P208 | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S30 Package Pins

**VQ100**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P28 | P29 | - | - | - | - |

11/02/00

**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P104 | P105 | - | - | - | - |

11/02/00

**CS144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| M3 | N3 | - | - | - | - |

11/02/00

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P7 | P13 | P38 | P44 | P55 | P56 |
| P60 | P97 | P112 | P118 | P143 | P149 |
| P165 | P202 | - | - | - | - |

11/02/00

**Notes:**

1. For the PQ208 package, P13, P38, P118, and P143, which are Not Connected Pins on the XC2S30, are assigned to $V_{CCINT}$ on larger devices.

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | TQ144 | PQ208 | FG256 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 5 | P99 | P63 | P6 | 326 |
| GND | - | P98 | P64 | GND* | - |
| $V_{CCO}$ | 5 | - | P65 | $V_{CCO}$<br>Bank 5* | - |
| $V_{CCINT}$ | - | P97 | P66 | $V_{CCINT}$* | - |
| I/O | 5 | P96 | P67 | R6 | 329 |
| I/O | 5 | P95 | P68 | M7 | 332 |
| I/O | 5 | - | P69 | N7 | 338 |
| I/O | 5 | - | P70 | T6 | 341 |
| I/O | 5 | - | P71 | P7 | 344 |
| GND | - | - | P72 | GND* | - |
| I/O, $V_{REF}$ | 5 | P94 | P73 | P8 | 347 |
| I/O | 5 | - | P74 | R7 | 350 |
| I/O | 5 | - | - | T7 | 353 |
| I/O | 5 | P93 | P75 | T8 | 356 |
| $V_{CCINT}$ | - | P92 | P76 | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P91 | P77 | R8 | 365 |
| $V_{CCO}$ | 5 | P90 | P78 | $V_{CCO}$<br>Bank 5* | - |
| $V_{CCO}$ | 4 | P90 | P78 | $V_{CCO}$<br>Bank 4* | - |
| GND | - | P89 | P79 | GND* | - |
| I, GCK0 | 4 | P88 | P80 | N8 | 366 |
| I/O | 4 | P87 | P81 | N9 | 370 |
| I/O | 4 | P86 | P82 | R9 | 373 |
| I/O | 4 | - | - | N10 | 376 |
| I/O | 4 | - | P83 | T9 | 379 |
| I/O, $V_{REF}$ | 4 | P85 | P84 | P9 | 382 |
| GND | - | - | P85 | GND* | - |
| I/O | 4 | - | P86 | M10 | 385 |
| I/O | 4 | - | P87 | R10 | 388 |
| I/O | 4 | - | P88 | P10 | 391 |
| I/O | 4 | P84 | P89 | T10 | 397 |
| I/O | 4 | P83 | P90 | R11 | 400 |
| $V_{CCINT}$ | - | P82 | P91 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | - | P92 | $V_{CCO}$<br>Bank 4* | - |
| GND | - | P81 | P93 | GND* | - |
| I/O | 4 | P80 | P94 | M11 | 403 |
| I/O | 4 | P79 | P95 | T11 | 406 |
| I/O | 4 | P78 | P96 | N11 | 409 |
| I/O | 4 | - | - | R12 | 412 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | TQ144 | PQ208 | FG256 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 4 | - | P97 | P11 | 415 |
| I/O, $V_{REF}$ | 4 | P77 | P98 | T12 | 418 |
| GND | - | - | - | GND* | - |
| I/O | 4 | - | P99 | T13 | 421 |
| I/O | 4 | - | - | N12 | 424 |
| I/O | 4 | P76 | P100 | R13 | 427 |
| I/O | 4 | - | - | P12 | 430 |
| I/O | 4 | P75 | P101 | P13 | 433 |
| I/O | 4 | P74 | P102 | T14 | 436 |
| GND | - | P73 | P103 | GND* | - |
| DONE | 3 | P72 | P104 | R14 | 439 |
| $V_{CCO}$ | 4 | P71 | P105 | $V_{CCO}$<br>Bank 4* | - |
| $V_{CCO}$ | 3 | P70 | P105 | $V_{CCO}$<br>Bank 3* | - |
| $\overline{\text{PROGRAM}}$ | - | P69 | P106 | P15 | 442 |
| I/O ($\overline{\text{INIT}}$) | 3 | P68 | P107 | N15 | 443 |
| I/O (D7) | 3 | P67 | P108 | N14 | 446 |
| I/O | 3 | - | - | T15 | 449 |
| I/O | 3 | P66 | P109 | M13 | 452 |
| I/O | 3 | - | - | R16 | 455 |
| I/O | 3 | - | P110 | M14 | 458 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 3 | P65 | P111 | L14 | 461 |
| I/O | 3 | - | P112 | M15 | 464 |
| I/O | 3 | - | - | L12 | 467 |
| I/O | 3 | P64 | P113 | P16 | 470 |
| I/O | 3 | P63 | P114 | L13 | 473 |
| I/O (D6) | 3 | P62 | P115 | N16 | 476 |
| GND | - | P61 | P116 | GND* | - |
| $V_{CCO}$ | 3 | - | P117 | $V_{CCO}$<br>Bank 3* | - |
| $V_{CCINT}$ | - | - | P118 | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P60 | P119 | M16 | 479 |
| I/O | 3 | P59 | P120 | K14 | 482 |
| I/O | 3 | - | - | L16 | 485 |
| I/O | 3 | - | P121 | K13 | 488 |
| I/O | 3 | - | P122 | L15 | 491 |
| I/O | 3 | - | P123 | K12 | 494 |
| GND | - | - | P124 | GND* | - |
| I/O, $V_{REF}$ | 3 | P58 | P125 | K16 | 497 |
| I/O (D4) | 3 | P57 | P126 | J16 | 500 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| **Function** | **Bank** | **TQ144** | **PQ208** | **FG256** | **Bndry Scan** |
| I/O | 3 | - | - | J14 | 503 |
| I/O | 3 | P56 | P127 | K15 | 506 |
| $V_{CCINT}$ | - | P55 | P128 | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P54 | P129 | J15 | 512 |
| $V_{CCO}$ | 3 | P53 | P130 | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P53 | P130 | $V_{CCO}$ Bank 2* | - |
| GND | - | P52 | P131 | GND* | - |
| I/O, IRDY(1) | 2 | P51 | P132 | H16 | 515 |
| I/O | 2 | - | P133 | H14 | 518 |
| I/O | 2 | P50 | P134 | H15 | 521 |
| I/O | 2 | - | - | J13 | 524 |
| I/O (D3) | 2 | P49 | P135 | G16 | 527 |
| I/O, $V_{REF}$ | 2 | P48 | P136 | H13 | 530 |
| GND | - | - | P137 | GND* | - |
| I/O | 2 | - | P138 | G14 | 533 |
| I/O | 2 | - | P139 | G15 | 536 |
| I/O | 2 | - | P140 | G12 | 539 |
| I/O | 2 | - | - | F16 | 542 |
| I/O | 2 | P47 | P141 | G13 | 545 |
| I/O (D2) | 2 | P46 | P142 | F15 | 548 |
| $V_{CCINT}$ | - | - | P143 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | - | P144 | $V_{CCO}$ Bank 2* | - |
| GND | - | P45 | P145 | GND* | - |
| I/O (D1) | 2 | P44 | P146 | E16 | 551 |
| I/O | 2 | P43 | P147 | F14 | 554 |
| I/O | 2 | P42 | P148 | D16 | 557 |
| I/O | 2 | - | - | F12 | 560 |
| I/O | 2 | - | P149 | E15 | 563 |
| I/O, $V_{REF}$ | 2 | P41 | P150 | F13 | 566 |
| GND | - | - | - | GND* | - |
| I/O | 2 | - | P151 | E14 | 569 |
| I/O | 2 | - | - | C16 | 572 |
| I/O | 2 | P40 | P152 | E13 | 575 |
| I/O | 2 | - | - | B16 | 578 |
| I/O (DIN, D0) | 2 | P39 | P153 | D14 | 581 |
| I/O (DOUT, BUSY) | 2 | P38 | P154 | C15 | 584 |
| CCLK | 2 | P37 | P155 | D15 | 587 |
| $V_{CCO}$ | 2 | P36 | P156 | $V_{CCO}$ Bank 2* | - |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| **Function** | **Bank** | **TQ144** | **PQ208** | **FG256** | **Bndry Scan** |
| $V_{CCO}$ | 1 | P35 | P156 | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P34 | P157 | B14 | - |
| GND | - | P33 | P158 | GND* | - |
| TDI | - | P32 | P159 | A15 | - |
| I/O ($\overline{CS}$) | 1 | P31 | P160 | B13 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P30 | P161 | C13 | 3 |
| I/O | 1 | - | - | C12 | 6 |
| I/O | 1 | P29 | P162 | A14 | 9 |
| I/O | 1 | - | - | D12 | 12 |
| I/O | 1 | - | P163 | B12 | 15 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 1 | P28 | P164 | C11 | 18 |
| I/O | 1 | - | P165 | A13 | 21 |
| I/O | 1 | - | - | D11 | 24 |
| I/O | 1 | - | P166 | A12 | 27 |
| I/O | 1 | P27 | P167 | E11 | 30 |
| I/O | 1 | P26 | P168 | B11 | 33 |
| GND | - | P25 | P169 | GND* | - |
| $V_{CCO}$ | 1 | - | P170 | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P24 | P171 | $V_{CCINT}$* | - |
| I/O | 1 | P23 | P172 | A11 | 36 |
| I/O | 1 | P22 | P173 | C10 | 39 |
| I/O | 1 | - | P174 | B10 | 45 |
| I/O | 1 | - | P175 | D10 | 48 |
| I/O | 1 | - | P176 | A10 | 51 |
| GND | - | - | P177 | GND* | - |
| I/O, $V_{REF}$ | 1 | P21 | P178 | B9 | 54 |
| I/O | 1 | - | P179 | E10 | 57 |
| I/O | 1 | - | - | A9 | 60 |
| I/O | 1 | P20 | P180 | D9 | 63 |
| I/O | 1 | P19 | P181 | A8 | 66 |
| I, GCK2 | 1 | P18 | P182 | C9 | 72 |
| GND | - | P17 | P183 | GND* | - |
| $V_{CCO}$ | 1 | P16 | P184 | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P16 | P184 | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P15 | P185 | B8 | 73 |
| $V_{CCINT}$ | - | P14 | P186 | $V_{CCINT}$* | - |
| I/O | 0 | P13 | P187 | A7 | 80 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| I/O, $V_{REF}$ | 4 | P79 | P95 | T11 | AB16 | 502 |
| I/O | 4 | - | - | - | AB17 | 505 |
| I/O | 4 | P78 | P96 | N11 | V15 | 508 |
| I/O | 4 | - | - | R12 | Y16 | 511 |
| I/O | 4 | - | P97 | P11 | AB18 | 517 |
| I/O, $V_{REF}$ | 4 | P77 | P98 | T12 | AB19 | 520 |
| $V_{CCO}$ | 4 | - | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 4 | - | P99 | T13 | Y17 | 523 |
| I/O | 4 | - | - | N12 | V16 | 526 |
| I/O | 4 | - | - | - | W17 | 529 |
| I/O | 4 | P76 | P100 | R13 | AB20 | 532 |
| I/O | 4 | - | - | P12 | AA19 | 535 |
| I/O | 4 | P75 | P101 | P13 | AA20 | 541 |
| I/O | 4 | P74 | P102 | T14 | W18 | 544 |
| GND | - | P73 | P103 | GND* | GND* | - |
| DONE | 3 | P72 | P104 | R14 | Y19 | 547 |
| $V_{CCO}$ | 4 | P71 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P70 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{\text{PROGRAM}}$ | - | P69 | P106 | P15 | W20 | 550 |
| I/O ($\overline{\text{INIT}}$) | 3 | P68 | P107 | N15 | V19 | 551 |
| I/O (D7) | 3 | P67 | P108 | N14 | Y21 | 554 |
| I/O | 3 | - | - | T15 | W21 | 560 |
| I/O | 3 | P66 | P109 | M13 | U20 | 563 |
| I/O | 3 | - | - | - | U19 | 566 |
| I/O | 3 | - | - | R16 | T18 | 569 |
| I/O | 3 | - | P110 | M14 | W22 | 572 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P65 | P111 | L14 | U21 | 575 |
| I/O | 3 | - | P112 | M15 | T20 | 578 |
| I/O | 3 | - | - | L12 | T21 | 584 |
| I/O | 3 | P64 | P113 | P16 | R18 | 587 |
| I/O | 3 | - | - | - | U22 | 590 |
| I/O, $V_{REF}$ | 3 | P63 | P114 | L13 | R19 | 593 |
| I/O (D6) | 3 | P62 | P115 | N16 | T22 | 596 |
| GND | - | P61 | P116 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| $V_{CCO}$ | 3 | - | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P60 | P119 | M16 | R21 | 599 |
| I/O | 3 | P59 | P120 | K14 | P18 | 602 |
| I/O | 3 | - | - | L16 | P20 | 605 |
| I/O | 3 | - | P121 | K13 | P21 | 608 |
| I/O | 3 | - | P122 | L15 | N18 | 614 |
| I/O | 3 | - | P123 | K12 | N20 | 617 |
| GND | - | - | P124 | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P58 | P125 | K16 | N21 | 620 |
| I/O (D4) | 3 | P57 | P126 | J16 | N22 | 623 |
| I/O | 3 | - | - | J14 | M19 | 626 |
| I/O | 3 | P56 | P127 | K15 | M20 | 629 |
| $V_{CCINT}$ | - | P55 | P128 | E5 | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P54 | P129 | J15 | M22 | 638 |
| $V_{CCO}$ | 3 | P53 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P53 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P52 | P131 | GND* | GND* | - |
| I/O, IRDY(1) | 2 | P51 | P132 | H16 | L20 | 641 |
| I/O | 2 | - | P133 | H14 | L17 | 644 |
| I/O | 2 | P50 | P134 | H15 | L21 | 650 |
| I/O | 2 | - | - | J13 | L22 | 653 |
| I/O (D3) | 2 | P49 | P135 | G16 | K20 | 656 |
| I/O, $V_{REF}$ | 2 | P48 | P136 | H13 | K21 | 659 |
| GND | - | - | P137 | GND* | GND* | - |
| I/O | 2 | - | P138 | G14 | K22 | 662 |
| I/O | 2 | - | P139 | G15 | J21 | 665 |
| I/O | 2 | - | P140 | G12 | J18 | 671 |
| I/O | 2 | - | - | F16 | J22 | 674 |
| I/O | 2 | P47 | P141 | G13 | H19 | 677 |
| I/O (D2) | 2 | P46 | P142 | F15 | H20 | 680 |
| $V_{CCINT}$ | - | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | - | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P45 | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P44 | P146 | E16 | H22 | 683 |
| I/O, $V_{REF}$ | 2 | P43 | P147 | F14 | H18 | 686 |
| I/O | 2 | - | - | - | G21 | 689 |
| I/O | 2 | P42 | P148 | D16 | G18 | 692 |

## Additional XC2S150 Package Pins

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

11/02/00

**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

11/02/00

## Additional XC2S150 Package Pins *(Continued)*

**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| F7 | F8 | F9 | F10 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U7 | U8 | U9 | U10 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A6 | A12 | A13 | A14 | B11 |
| B16 | C2 | C8 | C9 | D1 | D4 |
| D18 | D19 | E13 | E17 | E19 | F11 |
| G2 | G22 | H21 | J1 | J4 | K2 |
| K18 | K19 | L2 | L19 | M2 | M17 |
| M21 | N1 | P1 | P5 | P22 | R3 |
| R20 | R22 | U3 | U18 | V6 | W4 |
| W13 | W15 | W19 | Y5 | Y22 | AA1 |
| AA3 | AA9 | AA10 | AA11 | AA16 | AB7 |
| AB8 | AB12 | AB14 | AB21 | - | - |

11/02/00

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 6 | - | - | T2 | 449 |
| I/O | 6 | P43 | L4 | U1 | 452 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | M2 | R5 | 455 |
| I/O | 6 | - | - | V1 | 458 |
| I/O | 6 | - | - | T5 | 461 |
| I/O | 6 | P44 | L3 | U2 | 464 |
| I/O, $V_{REF}$ | 6 | P45 | N1 | T3 | 467 |
| $V_{CCO}$ | 6 | - | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | P46 | P1 | T4 | 470 |
| I/O | 6 | - | L5 | W1 | 473 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | - | V2 | 476 |
| I/O | 6 | - | - | U4 | 482 |
| I/O, $V_{REF}$ | 6 | P47 | N2 | Y1 | 485 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | M4 | W2 | 488 |
| I/O | 6 | - | - | V3 | 491 |
| I/O | 6 | - | - | V4 | 494 |
| I/O | 6 | P48 | R1 | Y2 | 500 |
| I/O | 6 | P49 | M3 | W3 | 503 |
| M1 | - | P50 | P2 | U5 | 506 |
| GND | - | P51 | GND* | GND* | - |
| M0 | - | P52 | N3 | AB2 | 507 |
| $V_{CCO}$ | 6 | P53 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| $V_{CCO}$ | 5 | P53 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| M2 | - | P54 | R3 | Y4 | 508 |
| I/O | 5 | - | - | W5 | 518 |
| I/O | 5 | - | - | AB3 | 521 |
| I/O | 5 | - | N5 | V7 | 524 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 5 | P57 | T2 | Y6 | 527 |
| I/O | 5 | - | - | AA4 | 530 |
| I/O | 5 | - | - | AB4 | 536 |
| I/O | 5 | - | P5 | W6 | 539 |
| I/O | 5 | P58 | T3 | Y7 | 542 |
| GND | - | - | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P59 | T4 | AA5 | 545 |
| I/O | 5 | P60 | M6 | AB5 | 548 |
| I/O | 5 | - | - | V8 | 551 |
| I/O | 5 | - | - | AA6 | 554 |
| I/O | 5 | - | T5 | AB6 | 557 |
| GND | - | - | GND* | GND* | - |
| I/O | 5 | P61 | N6 | AA7 | 560 |
| I/O | 5 | - | - | W7 | 563 |
| I/O, $V_{REF}$ | 5 | P62 | R5 | W8 | 569 |
| I/O | 5 | P63 | P6 | Y8 | 572 |
| GND | - | P64 | GND* | GND* | - |
| $V_{CCO}$ | 5 | P65 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCINT}$ | - | P66 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 5 | P67 | R6 | AA8 | 575 |
| I/O | 5 | P68 | M7 | V9 | 578 |
| I/O | 5 | - | - | AB8 | 581 |
| I/O | 5 | - | - | W9 | 584 |
| I/O | 5 | - | - | AB9 | 587 |
| GND | - | - | GND* | GND* | - |
| I/O | 5 | P69 | N7 | Y9 | 590 |
| I/O | 5 | - | - | V10 | 593 |
| I/O | 5 | - | - | AA9 | 596 |
| I/O | 5 | P70 | T6 | W10 | 599 |
| I/O | 5 | P71 | P7 | AB10 | 602 |
| GND | - | P72 | GND* | GND* | - |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P73 | P8 | Y10 | 605 |
| I/O | 5 | P74 | R7 | V11 | 608 |
| I/O | 5 | - | - | AA10 | 614 |
| I/O | 5 | - | T7 | W11 | 617 |
| I/O | 5 | P75 | T8 | AB11 | 620 |
| I/O | 5 | - | - | U11 | 623 |
| $V_{CCINT}$ | - | P76 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P77 | R8 | Y11 | 635 |
| $V_{CCO}$ | 5 | P78 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCO}$ | 4 | P78 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P79 | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| **Function** | **Bank** | | | | |
| I, GCK0 | 4 | P80 | N8 | W12 | 636 |
| I/O | 4 | P81 | N9 | U12 | 640 |
| I/O | 4 | - | - | V12 | 646 |
| I/O | 4 | P82 | R9 | Y12 | 649 |
| I/O | 4 | - | N10 | AA12 | 652 |
| I/O | 4 | - | - | W13 | 655 |
| I/O | 4 | P83 | T9 | AB13 | 661 |
| I/O, $V_{REF}$ | 4 | P84 | P9 | AA13 | 664 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P85 | GND* | GND* | - |
| I/O | 4 | P86 | M10 | Y13 | 667 |
| I/O | 4 | P87 | R10 | V13 | 670 |
| I/O | 4 | - | - | AB14 | 673 |
| I/O | 4 | - | - | W14 | 676 |
| I/O | 4 | P88 | P10 | AA14 | 679 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | - | V14 | 682 |
| I/O | 4 | - | - | Y14 | 685 |
| I/O | 4 | - | - | W15 | 688 |
| I/O | 4 | P89 | T10 | AB15 | 691 |
| I/O | 4 | P90 | R11 | AA15 | 694 |
| $V_{CCINT}$ | - | P91 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | P92 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P93 | GND* | GND* | - |
| I/O | 4 | P94 | M11 | Y15 | 697 |
| I/O, $V_{REF}$ | 4 | P95 | T11 | AB16 | 700 |
| I/O | 4 | - | - | AB17 | 706 |
| I/O | 4 | P96 | N11 | V15 | 709 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | R12 | Y16 | 712 |
| I/O | 4 | - | - | AA17 | 715 |
| I/O | 4 | - | - | W16 | 718 |
| I/O | 4 | P97 | P11 | AB18 | 721 |
| I/O, $V_{REF}$ | 4 | P98 | T12 | AB19 | 724 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | P99 | T13 | Y17 | 727 |
| I/O | 4 | - | N12 | V16 | 730 |
| I/O | 4 | - | - | AA18 | 733 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| **Function** | **Bank** | | | | |
| I/O | 4 | - | - | W17 | 739 |
| I/O, $V_{REF}$ | 4 | P100 | R13 | AB20 | 742 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | P12 | AA19 | 745 |
| I/O | 4 | - | - | V17 | 748 |
| I/O | 4 | - | - | Y18 | 751 |
| I/O | 4 | P101 | P13 | AA20 | 757 |
| I/O | 4 | P102 | T14 | W18 | 760 |
| GND | - | P103 | GND* | GND* | - |
| DONE | 3 | P104 | R14 | Y19 | 763 |
| $V_{CCO}$ | 4 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{\text{PROGRAM}}$ | - | P106 | P15 | W20 | 766 |
| I/O ($\overline{\text{INIT}}$) | 3 | P107 | N15 | V19 | 767 |
| I/O (D7) | 3 | P108 | N14 | Y21 | 770 |
| I/O | 3 | - | - | V20 | 776 |
| I/O | 3 | - | - | AA22 | 779 |
| I/O | 3 | - | T15 | W21 | 782 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P109 | M13 | U20 | 785 |
| I/O | 3 | - | - | U19 | 788 |
| I/O | 3 | - | - | V21 | 794 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | - | R16 | T18 | 797 |
| I/O | 3 | P110 | M14 | W22 | 800 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P111 | L14 | U21 | 803 |
| I/O | 3 | P112 | M15 | T20 | 806 |
| I/O | 3 | - | - | T19 | 809 |
| I/O | 3 | - | - | V22 | 812 |
| I/O | 3 | - | L12 | T21 | 815 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P113 | P16 | R18 | 818 |
| I/O | 3 | - | - | U22 | 821 |
| I/O, $V_{REF}$ | 3 | P114 | L13 | R19 | 827 |
| I/O (D6) | 3 | P115 | N16 | T22 | 830 |
| GND | - | P116 | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| **Function** | **Bank** | **PQ208** | **FG256** | **FG456** | **Bndry Scan** |
| GND | - | P198 | GND* | GND* | - |
| I/O | 0 | P199 | A5 | B7 | 188 |
| I/O, $V_{REF}$ | 0 | P200 | C6 | E8 | 191 |
| I/O | 0 | - | - | D8 | 197 |
| I/O | 0 | P201 | B5 | C7 | 200 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | D6 | D7 | 203 |
| I/O | 0 | - | - | B6 | 206 |
| I/O | 0 | - | - | A5 | 209 |
| I/O | 0 | P202 | A4 | D6 | 212 |
| I/O, $V_{REF}$ | 0 | P203 | B4 | C6 | 215 |
| $V_{CCO}$ | 0 | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | P204 | E6 | B5 | 218 |
| I/O | 0 | - | D5 | E7 | 221 |
| I/O | 0 | - | - | A4 | 224 |
| I/O | 0 | - | - | E6 | 230 |
| I/O, $V_{REF}$ | 0 | P205 | A3 | B4 | 233 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | C5 | A3 | 236 |
| I/O | 0 | - | - | B3 | 239 |
| I/O | 0 | - | - | D5 | 242 |
| I/O | 0 | P206 | B3 | C5 | 248 |
| TCK | - | P207 | C4 | C4 | - |
| $V_{CCO}$ | 0 | P208 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P208 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S200 Package Pins

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

11/02/00

**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

## Additional XC2S200 Package Pins *(Continued)*

11/02/00

**FG456**

| **$V_{CCINT}$ Pins** | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| F7 | F8 | F9 | F10 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U7 | U8 | U9 | U10 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |

## Additional XC2S200 Package Pins *(Continued)*

| G6 | H6 | J6 | K6 | K7 | L7 |
|---|---|---|---|---|---|
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A6 | A12 | B11 | B16 | C2 |
| D1 | D4 | D18 | D19 | E17 | E19 |
| G2 | G22 | L2 | L19 | M2 | M21 |
| R3 | R20 | U3 | U18 | V6 | W4 |
| W19 | Y5 | Y22 | AA1 | AA3 | AA11 |
| AA16 | AB7 | AB12 | AB21 | - | - |

11/02/00

## Revision History

| Version No. | Date | Description |
|---|---|---|
| 2.0 | 09/18/00 | Sectioned the Spartan-II Family data sheet into four modules. Corrected all known errors in the pinout tables. |
| 2.1 | 10/04/00 | Added notes requiring $\overline{PWDN}$ to be tied to $V_{CCINT}$ when unused. |
| 2.2 | 11/02/00 | Removed the Power Down feature. |
| 2.3 | 03/05/01 | Added notes on pinout tables for IRDY and TRDY. |
| 2.4 | 04/30/01 | Reinstated XC2S50 $V_{CCO}$ Bank 7, GND, and "not connected" pins missing in version 2.3. |
| 2.5 | 09/03/03 | Added caution about Not Connected Pins to XC2S30 pinout tables on page 76. |
| 2.8 | 06/13/08 | Added "Package Overview" section. Added notes to clarify shared $V_{CCO}$ banks. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |