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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	600
Number of Logic Elements/Cells	2700
Total RAM Bits	40960
Number of I/O	140
Number of Gates	100000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s100-5pq208i

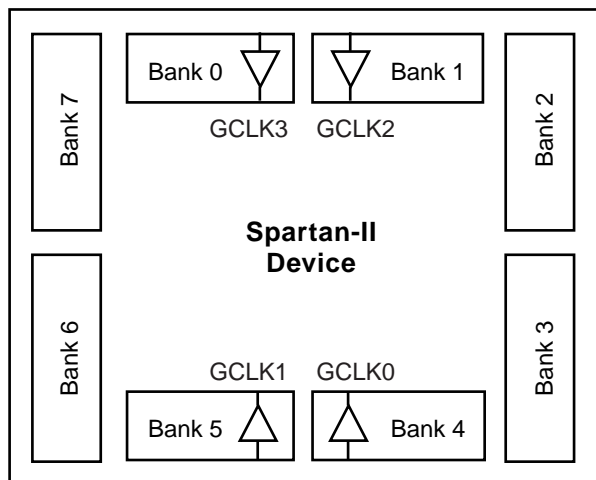
drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage is determined by the output standards in use.



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Figure 3: Spartan-II I/O Banks

Within a bank, output standards may be mixed only if they use the same V_{CCO} . Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO} .

Table 4: Compatible Output Standards

V_{CCO}	Compatible Standards
3.3V	PCI, LVTTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF} . In this case, certain user-I/O pins are

automatically configured as inputs for the V_{REF} voltage. About one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

In a bank, inputs requiring V_{REF} can be mixed with those that do not but only one V_{REF} voltage may be used within a bank. Input buffers that use V_{REF} are not 5V tolerant. LVTTTL, LVCMOS2, and PCI are 5V tolerant. The V_{CCO} and V_{REF} pins for each bank appear in the device pinout tables.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device. All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

Independent Banks Available

Package	VQ100 PQ208	CS144 TQ144	FG256 FG456
Independent Banks	1	4	8

Configurable Logic Block

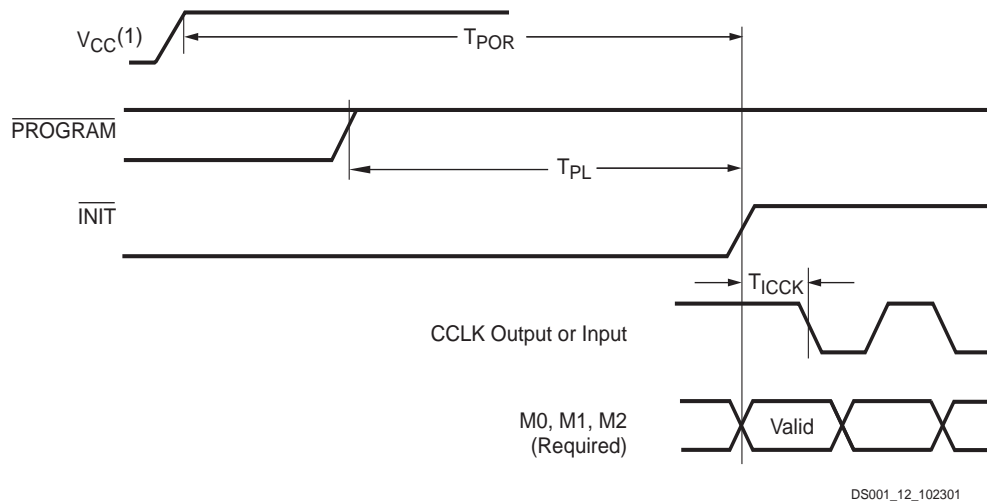
The basic building block of the Spartan-II FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. Output from the function generator in each LC drives the CLB output and the D input of the flip-flop. Each Spartan-II FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 4.

In addition to the four basic LCs, the Spartan-II FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

Look-Up Tables

Spartan-II FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-II FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.



Symbol	Description	Min	Max
T_{POR}	Power-on reset	-	2 ms
T_{PL}	Program latency	-	100 μ s
T_{ICCK}	CCLK output delay (Master Serial mode only)	0.5 μ s	4 μ s
$T_{PROGRAM}$	Program pulse width	300 ns	-

Notes: (referring to waveform above:)

1. Before configuration can begin, V_{CCINT} must be greater than 1.6V and V_{CCO} Bank 2 must be greater than 1.0V.

Figure 12: Configuration Timing on Power-Up

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving \overline{INIT} Low. At this time, the user can delay configuration by holding either $\overline{PROGRAM}$ or \overline{INIT} Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional \overline{INIT} line is driving a Low logic level during memory clearing. To avoid contention, use an open-drain driver to keep \overline{INIT} Low.

With no delay in force, the device indicates that the memory is completely clear by driving \overline{INIT} High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data

Once \overline{INIT} is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 14. Loading data using the Slave Parallel mode is shown in Figure 19, page 25.

CRC Error Checking

During the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values

do not match, the FPGA drives \overline{INIT} Low to indicate that a frame error has occurred and configuration is aborted.

To reconfigure the device, the $\overline{PROGRAM}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See "Clearing Configuration Memory".

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State net. This activates I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-down resistors present.
3. Negates Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

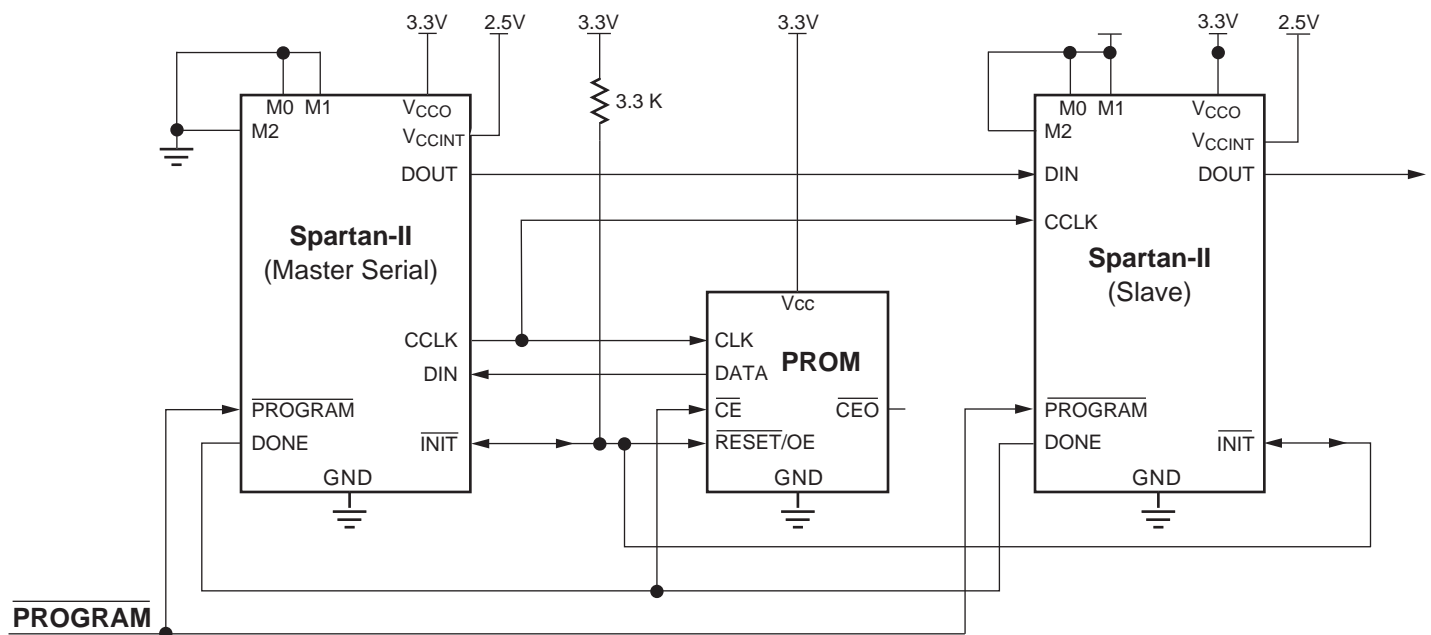
Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is $2^{20}-1$ (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until INIT pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.



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Notes:

1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 15: Master/Slave Serial Configuration Circuit Diagram

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 25.

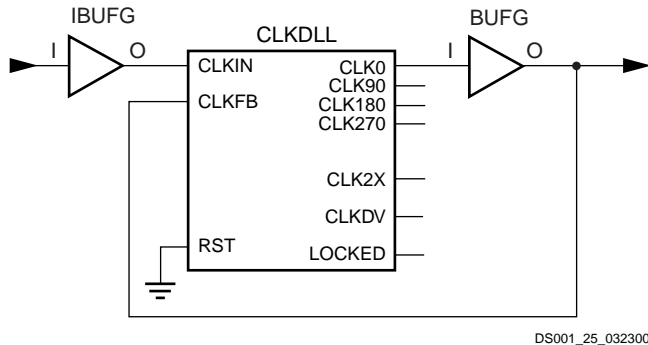


Figure 25: BUFGDLL Block Diagram

This macro does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This macro also does not provide access to the RST or LOCKED pins of the DLL. For access to these features, a designer must use the DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG primitive, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50/50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL

or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. Either a global clock buffer (BUFG) or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feed back to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software to determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates, the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or be tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer deskew with respect to one another. The DLL must be reset when the input clock frequency changes, if the device is reconfigured in Boundary-Scan mode, if the device undergoes a hot swap, and after the device is configured if the input clock is not stable during the startup sequence.

2x Clock Output — CLK2X

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

Clock Divide Output — CLKDV

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction. The CLKDV output pin has a 50/50 duty cycle for all values of the

Table 11: Available Library Primitives

Primitive	Port A Width	Port B Width
RAMB4_S4	4	N/A
RAMB4_S4_S4		4
RAMB4_S4_S8		8
RAMB4_S4_S16		16
RAMB4_S8	8	N/A
RAMB4_S8_S8		8
RAMB4_S8_S16		16
RAMB4_S16	16	N/A
RAMB4_S16_S16		16

Port Signals

Each block RAM port operates independently of the others while accessing the same set of 4096 memory cells.

Table 12 describes the depth and width aspect ratios for the block RAM memory.

Table 12: Block RAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A/B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A/B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A/B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A/B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A/B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 12.

Data In Bus—DI[A/B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 12.

Data Output Bus—DO[A/B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 12.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$\text{Start} = ([\text{ADDR}_{\text{port}} + 1] * \text{Width}_{\text{port}}) - 1$$

$$\text{End} = \text{ADDR}_{\text{port}} * \text{Width}_{\text{port}}$$

Table 13 shows low order address mapping for each port width.

Table 13: Port Address Mapping

Port Width	Port Addresses																
1	4095...	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features, system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 15, each buffer type can support a variety of voltage requirements.

Table 15: Versatile I/O Supported Standards (Typical Values)

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTTL (2-24 mA)	N/A	3.3	N/A
LVC MOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	1.5
HSTL Class IV	0.9	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance JEDEC website at <http://www.jedec.org>. For more details on the I/O standards and termination application examples, see XAPP179, "Using SelectIO Interfaces in Spartan-II and Spartan-IIe FPGAs."

LVTTTL — Low-Voltage TTL

The Low-Voltage TTL (LVTTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVC MOS2 — Low-Voltage CMOS for 2.5V

The Low-Voltage CMOS for 2.5V or lower (LVC MOS2) standard is an extension of the LVC MOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

the LOC property is described below. Table 16 summarizes the input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

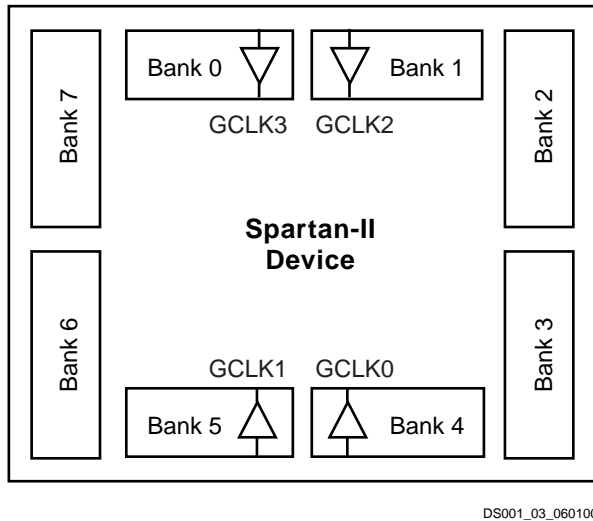


Figure 36: I/O Banks

Table 16: Xilinx Input Standards Compatibility Requirements

Rule 1	All differential amplifier input signals within a bank are required to be of the same standard.
Rule 2	There are no placement restrictions for inputs with standards that require a single-ended input buffer.

IBUFG

Signals used as high fanout clock inputs to the Spartan-II device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG primitive can

only drive a CLKDLL, CLKDLLHF, or a BUFG primitive. The generic IBUFG primitive appears in Figure 37.

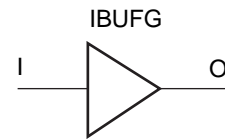


Figure 37: Global Clock Input Buffer (IBUFG) Primitive

With no extension or property specified for the generic IBUFG primitive, the assumed standard is LVTTTL.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP primitive represents a combination of the LVTTTL IBUFG and BUFG primitives, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

The Spartan-II FPGA BUFGP primitive can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) primitive appears in Figure 38.

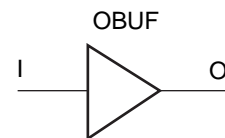


Figure 38: Output Buffer (OBUF) Primitive

With no extension or property specified for the generic OBUF primitive, the assumed standard is slew rate limited LVTTTL with 12 mA drive strength.

The LVTTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

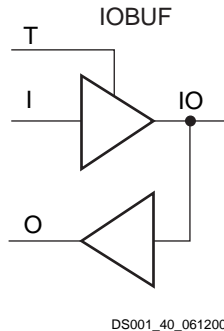


Figure 40: Input/Output Buffer Primitive (IOBUF)

When the IOBUF primitive supports an I/O standard such as LVTTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard ($V_{CCO} < 2V$), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36, page 39 for a representation of the Spartan-II FPGA I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

IOB Flip-Flop/Latch Property

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified:

```
map -pr b <filename>
```

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each Versatile I/O primitive with the location constraint LOC attached to the Versatile I/O primitive. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

```
LOC=A42
```

```
LOC=P37
```

Output Slew Rate Property

In the case of the LVTTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

```
SLEW=SLOW
```

```
SLEW=FAST
```

Output Drive Strength Property

For the LVTTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE=

property. This property could have one of the following seven values.

DRIVE=2
 DRIVE=4
 DRIVE=6
 DRIVE=8
 DRIVE=12 (Default)
 DRIVE=16
 DRIVE=24

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See [Figure 36, page 39](#) for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The V_{CCO} supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined V_{CCO} supply. The TQ144 and the CS144 packages provide four independent V_{CCO} supplies. The FG256 and the FG456 provide eight independent V_{CCO} supplies.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

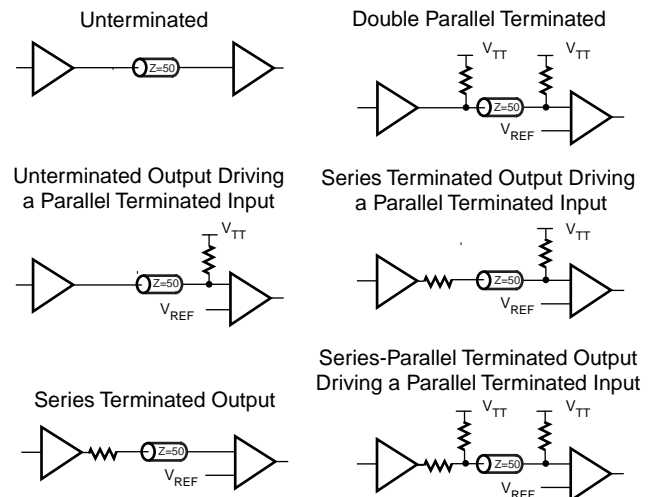
The following lists output termination techniques:

None
 Series
 Parallel (Shunt)
 Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None
 Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in [Figure 41](#).



DS001_41_032300

Figure 41: Overview of Standard Input and Output Termination Methods

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 42. Table 20 lists DC voltage specifications for the GTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

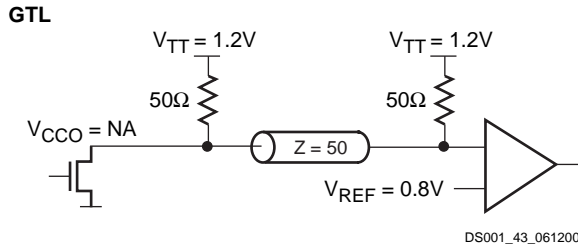


Figure 42: Terminated GTL

Table 20: GTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}^{(1)}$	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} \geq V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} \leq V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.4V	32	-	-
I_{OL} at V_{OL} (mA) at 0.2V	-	-	40

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 43. DC voltage specifications appear in Table 21 for the GTL+ standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

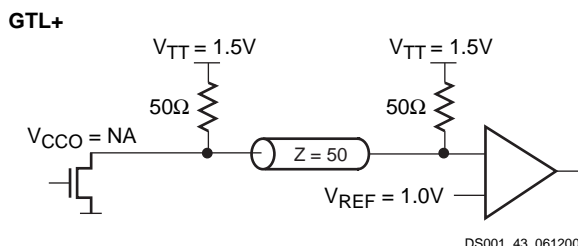


Figure 43: Terminated GTL+

Table 21: GTL+ Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}^{(1)}$	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} \geq V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} \leq V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.6V	36	-	-
I_{OL} at V_{OL} (mA) at 0.3V	-	-	48

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

HSTL Class I

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 44. DC voltage specifications appear in Table 22 for the HSTL_1 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

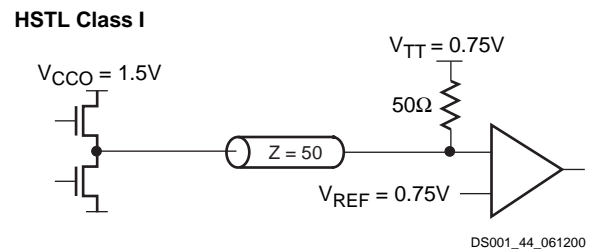


Figure 44: Terminated HSTL Class I

Table 22: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

SSTL3 Class I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 47. DC voltage specifications appear in Table 25 for the SSTL3_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

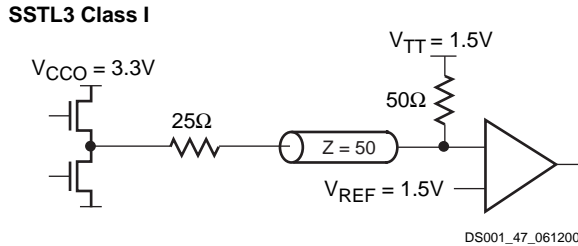


Figure 47: Terminated SSTL3 Class I

Table 25: SSTL3_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} \leq V_{REF} - 0.2$	-0.3 ⁽²⁾	1.3	1.5
$V_{OH} \geq V_{REF} + 0.6$	1.9	-	-
$V_{OL} \leq V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:

- V_{IH} maximum is $V_{CCO} + 0.3$.
- V_{IL} minimum does not conform to the formula.

SSTL3 Class II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 48. DC voltage specifications appear in Table 26 for the SSTL3_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

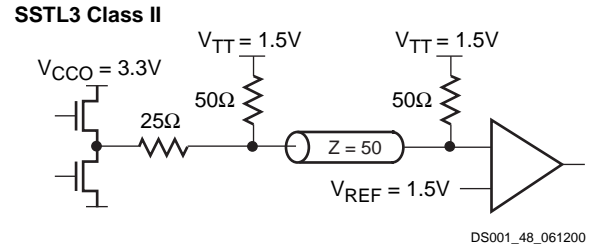


Figure 48: Terminated SSTL3 Class II

Table 26: SSTL3_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} \leq V_{REF} - 0.2$	-0.3 ⁽²⁾	1.3	1.5
$V_{OH} \geq V_{REF} + 0.8$	2.1	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	-16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:

- V_{IH} maximum is $V_{CCO} + 0.3$.
- V_{IL} minimum does not conform to the formula.

IOB Input Delay Adjustments for Different Standards⁽¹⁾

Input delays associated with the pad are specified for LVTTTL. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Data Input Delay Adjustments					
T _{ILVTTL}	Standard-specific data input delay adjustments	LVTTTL	0	0	ns
T _{ILVCMOS2}		LVCMSO2	−0.04	−0.05	ns
T _{IPCI33_3}		PCI, 33 MHz, 3.3V	−0.11	−0.13	ns
T _{IPCI33_5}		PCI, 33 MHz, 5.0V	0.26	0.30	ns
T _{IPCI66_3}		PCI, 66 MHz, 3.3V	−0.11	−0.13	ns
T _{IGTL}		GTL	0.20	0.24	ns
T _{IGTLP}		GTL+	0.11	0.13	ns
T _{IHSTL}		HSTL	0.03	0.04	ns
T _{ISSTL2}		SSTL2	−0.08	−0.09	ns
T _{ISSTL3}		SSTL3	−0.04	−0.05	ns
T _{ICTT}		CTT	0.02	0.02	ns
T _{IAGP}		AGP	−0.06	−0.07	ns

Notes:

- Input timing for LVTTTL is measured at 1.4V. For other I/O standards, see the table ["Delay Measurement Methodology," page 60](#).

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O Input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard as listed in the table "Constants for Calculating T_{IOOP} ", below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, T_{IOOP1} .

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

Adj is selected from "IOB Output Delay Adjustments for Different Standards", page 59, according to the I/O standard used

C_{LOAD} is the capacitive load for the design

F_L is the capacitance scaling factor

Delay Measurement Methodology

Standard	$V_L^{(1)}$	$V_H^{(1)}$	Meas. Point	V_{REF} Typ ⁽²⁾
LVTTL	0	3	1.4	-
LVC MOS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.80
GTL+	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.0
HSTL Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL Class III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL Class IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL3 I and II	$V_{REF} - 1.0$	$V_{REF} + 1.0$	V_{REF}	1.5
SSTL2 I and II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
CTT	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.5
AGP	$V_{REF} - (0.2 \times V_{CCO})$	$V_{REF} + (0.2 \times V_{CCO})$	V_{REF}	Per AGP Spec

Notes:

- Input waveform switches between V_L and V_H .
- Measurements are made at V_{REF} Typ, Maximum, and Minimum. Worst-case values are reported.
- I/O parameter measurements are made with the capacitance values shown in the table, "Constants for Calculating T_{IOOP} ". See Xilinx application note [XAPP179](#) for the appropriate terminations.
- I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Constants for Calculating T_{IOOP}

Standard	$C_{SL}^{(1)}$ (pF)	F_L (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVC MOS2	35	0.041
PCI 33 MHz 5V	50	0.050
PCI 33 MHz 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

- I/O parameter measurements are made with the capacitance values shown above. See Xilinx application note [XAPP179](#) for the appropriate terminations.
- I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Introduction

This section describes how the various pins on a Spartan®-II FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-II FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all

information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-II FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-II FPGA packages, as outlined in [Table 35](#).

Table 35: Pin Definitions

Pin Name	Dedicated	Direction	Description
GCK0, GCK1, GCK2, GCK3	No	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin. It is an input for slave-parallel and slave-serial modes, and output in master-serial mode.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. This pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
CS	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V _{CCINT}	Yes	Input	Power supply pins for the internal core logic.
V _{CCO}	Yes	Input	Power supply pins for output drivers (subject to banking rules)
V _{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx® PCI cores. If the cores are not used, these pins are available as user I/Os.

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
I/O, V _{REF}	4	P79	P95	T11	AB16	502
I/O	4	-	-	-	AB17	505
I/O	4	P78	P96	N11	V15	508
I/O	4	-	-	R12	Y16	511
I/O	4	-	P97	P11	AB18	517
I/O, V _{REF}	4	P77	P98	T12	AB19	520
V _{CCO}	4	-	-	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	-	-	GND*	GND*	-
I/O	4	-	P99	T13	Y17	523
I/O	4	-	-	N12	V16	526
I/O	4	-	-	-	W17	529
I/O	4	P76	P100	R13	AB20	532
I/O	4	-	-	P12	AA19	535
I/O	4	P75	P101	P13	AA20	541
I/O	4	P74	P102	T14	W18	544
GND	-	P73	P103	GND*	GND*	-
DONE	3	P72	P104	R14	Y19	547
V _{CCO}	4	P71	P105	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
V _{CCO}	3	P70	P105	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
PROGRAM	-	P69	P106	P15	W20	550
I/O (INIT)	3	P68	P107	N15	V19	551
I/O (D7)	3	P67	P108	N14	Y21	554
I/O	3	-	-	T15	W21	560
I/O	3	P66	P109	M13	U20	563
I/O	3	-	-	-	U19	566
I/O	3	-	-	R16	T18	569
I/O	3	-	P110	M14	W22	572
GND	-	-	-	GND*	GND*	-
V _{CCO}	3	-	-	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
I/O, V _{REF}	3	P65	P111	L14	U21	575
I/O	3	-	P112	M15	T20	578
I/O	3	-	-	L12	T21	584
I/O	3	P64	P113	P16	R18	587
I/O	3	-	-	-	U22	590
I/O, V _{REF}	3	P63	P114	L13	R19	593
I/O (D6)	3	P62	P115	N16	T22	596
GND	-	P61	P116	GND*	GND*	-

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
V _{CCO}	3	-	P117	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{CCINT}	-	-	P118	V _{CCINT} *	V _{CCINT} *	-
I/O (D5)	3	P60	P119	M16	R21	599
I/O	3	P59	P120	K14	P18	602
I/O	3	-	-	L16	P20	605
I/O	3	-	P121	K13	P21	608
I/O	3	-	P122	L15	N18	614
I/O	3	-	P123	K12	N20	617
GND	-	-	P124	GND*	GND*	-
I/O, V _{REF}	3	P58	P125	K16	N21	620
I/O (D4)	3	P57	P126	J16	N22	623
I/O	3	-	-	J14	M19	626
I/O	3	P56	P127	K15	M20	629
V _{CCINT}	-	P55	P128	E5	V _{CCINT} *	-
I/O, TRDY ⁽¹⁾	3	P54	P129	J15	M22	638
V _{CCO}	3	P53	P130	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{CCO}	2	P53	P130	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P52	P131	GND*	GND*	-
I/O, IRDY ⁽¹⁾	2	P51	P132	H16	L20	641
I/O	2	-	P133	H14	L17	644
I/O	2	P50	P134	H15	L21	650
I/O	2	-	-	J13	L22	653
I/O (D3)	2	P49	P135	G16	K20	656
I/O, V _{REF}	2	P48	P136	H13	K21	659
GND	-	-	P137	GND*	GND*	-
I/O	2	-	P138	G14	K22	662
I/O	2	-	P139	G15	J21	665
I/O	2	-	P140	G12	J18	671
I/O	2	-	-	F16	J22	674
I/O	2	P47	P141	G13	H19	677
I/O (D2)	2	P46	P142	F15	H20	680
V _{CCINT}	-	-	P143	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	2	-	P144	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P45	P145	GND*	GND*	-
I/O (D1)	2	P44	P146	E16	H22	683
I/O, V _{REF}	2	P43	P147	F14	H18	686
I/O	2	-	-	-	G21	689
I/O	2	P42	P148	D16	G18	692

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	6	P46	P1	T4	404
I/O	6	-	L5	W1	407
I/O	6	-	-	V2	410
I/O	6	-	-	U4	413
I/O	6	P47	N2	Y1	416
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	419
I/O	6	-	-	V3	422
I/O	6	-	-	V4	425
I/O	6	P48	R1	Y2	428
I/O	6	P49	M3	W3	431
M1	-	P50	P2	U5	434
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	435
V _{CCO}	6	P53	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
V _{CCO}	5	P53	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
M2	-	P54	R3	Y4	436
I/O	5	-	-	W5	443
I/O	5	-	-	AB3	446
I/O	5	-	N5	V7	449
GND	-	-	GND*	GND*	-
I/O	5	P57	T2	Y6	452
I/O	5	-	-	AA4	455
I/O	5	-	-	AB4	458
I/O	5	-	P5	W6	461
I/O	5	P58	T3	Y7	464
GND	-	-	GND*	GND*	-
V _{CCO}	5	-	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
I/O, V _{REF}	5	P59	T4	AA5	467
I/O	5	P60	M6	AB5	470
I/O	5	-	-	V8	473
I/O	5	-	-	AA6	476
I/O	5	-	T5	AB6	479
I/O	5	P61	N6	AA7	482
I/O	5	-	-	W7	485
I/O, V _{REF}	5	P62	R5	W8	488
I/O	5	P63	P6	Y8	491
GND	-	P64	GND*	GND*	-

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V _{CCO}	5	P65	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCINT}	-	P66	V _{CCINT} *	V _{CCINT} *	-
I/O	5	P67	R6	AA8	494
I/O	5	P68	M7	V9	497
I/O	5	-	-	W9	503
I/O	5	-	-	AB9	506
I/O	5	P69	N7	Y9	509
I/O	5	-	-	V10	512
I/O	5	P70	T6	W10	518
I/O	5	P71	P7	AB10	521
GND	-	P72	GND*	GND*	-
V _{CCO}	5	-	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
I/O, V _{REF}	5	P73	P8	Y10	524
I/O	5	P74	R7	V11	527
I/O	5	-	T7	W11	530
I/O	5	P75	T8	AB11	533
I/O	5	-	-	U11	536
V _{CCINT}	-	P76	V _{CCINT} *	V _{CCINT} *	-
I, GCK1	5	P77	R8	Y11	545
V _{CCO}	5	P78	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCO}	4	P78	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-
I, GCK0	4	P80	N8	W12	546
I/O	4	P81	N9	U12	550
I/O	4	-	-	V12	553
I/O	4	P82	R9	Y12	556
I/O	4	-	N10	AA12	559
I/O	4	P83	T9	AB13	562
I/O, V _{REF}	4	P84	P9	AA13	565
V _{CCO}	4	-	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P85	GND*	GND*	-
I/O	4	P86	M10	Y13	568
I/O	4	P87	R10	V13	571
I/O	4	-	-	W14	577
I/O	4	P88	P10	AA14	580
I/O	4	-	-	V14	583
I/O	4	-	-	Y14	586
I/O	4	P89	T10	AB15	592

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O, IRDY ⁽¹⁾	2	P132	H16	L20	767
I/O	2	P133	H14	L17	770
I/O	2	-	-	L18	773
I/O	2	P134	H15	L21	776
I/O	2	-	J13	L22	779
I/O (D3)	2	P135	G16	K20	782
I/O, V _{REF}	2	P136	H13	K21	785
V _{CCO}	2	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P137	GND*	GND*	-
I/O	2	P138	G14	K22	788
I/O	2	P139	G15	J21	791
I/O	2	-	-	J20	797
I/O	2	P140	G12	J18	800
I/O	2	-	F16	J22	803
I/O	2	-	-	J19	806
I/O	2	P141	G13	H19	812
I/O (D2)	2	P142	F15	H20	815
V _{CCINT}	-	P143	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	2	P144	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P145	GND*	GND*	-
I/O (D1)	2	P146	E16	H22	818
I/O, V _{REF}	2	P147	F14	H18	821
I/O	2	-	-	G21	824
I/O	2	P148	D16	G18	827
I/O	2	-	F12	G20	830
I/O	2	-	-	G19	833
I/O	2	-	-	F22	836
I/O	2	P149	E15	F19	839
I/O, V _{REF}	2	P150	F13	F21	842
V _{CCO}	2	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	-	GND*	GND*	-
I/O	2	P151	E14	F20	845
I/O	2	-	C16	F18	848
I/O	2	-	-	E22	851
I/O	2	-	-	E21	854
I/O	2	P152	E13	D22	857
GND	-	-	GND*	GND*	-
I/O	2	-	B16	E20	860
I/O	2	-	-	D21	863

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	2	-	-	C22	866
I/O (DIN, D0)	2	P153	D14	D20	869
I/O (DOUT, BUSY)	2	P154	C15	C21	872
CCLK	2	P155	D15	B22	875
V _{CCO}	2	P156	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
V _{CCO}	1	P156	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
TDO	2	P157	B14	A21	-
GND	-	P158	GND*	GND*	-
TDI	-	P159	A15	B20	-
I/O ($\overline{\text{CS}}$)	1	P160	B13	C19	0
I/O ($\overline{\text{WRITE}}$)	1	P161	C13	A20	3
I/O	1	-	-	B19	6
I/O	1	-	-	C18	9
I/O	1	-	C12	D17	12
GND	-	-	GND*	GND*	-
I/O	1	P162	A14	A19	15
I/O	1	-	-	B18	18
I/O	1	-	-	E16	21
I/O	1	-	D12	C17	24
I/O	1	P163	B12	D16	27
GND	-	-	GND*	GND*	-
V _{CCO}	1	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P164	C11	A18	30
I/O	1	P165	A13	B17	33
I/O	1	-	-	E15	36
I/O	1	-	-	A17	39
I/O	1	-	D11	D15	42
I/O	1	P166	A12	C16	45
I/O	1	-	-	D14	48
I/O, V _{REF}	1	P167	E11	E14	51
I/O	1	P168	B11	A16	54
GND	-	P169	GND*	GND*	-
V _{CCO}	1	P170	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCINT}	-	P171	V _{CCINT} *	V _{CCINT} *	-
I/O	1	P172	A11	C15	57
I/O	1	P173	C10	B15	60
I/O	1	-	-	A15	66
I/O	1	-	-	F12	69

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	1	P174	B10	C14	72
I/O	1	-	-	B14	75
I/O	1	P175	D10	D13	81
I/O	1	P176	A10	C13	84
GND	-	P177	GND*	GND*	-
V _{CCO}	1	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P178	B9	B13	87
I/O	1	P179	E10	E12	90
I/O	1	-	A9	B12	93
I/O	1	P180	D9	D12	96
I/O	1	-	-	C12	99
I/O	1	P181	A8	D11	102
I, GCK2	1	P182	C9	A11	108
GND	-	P183	GND*	GND*	-
V _{CCO}	1	P184	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCO}	0	P184	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
I, GCK3	0	P185	B8	C11	109
V _{CCINT}	-	P186	V _{CCINT} *	V _{CCINT} *	-
I/O	0	-	-	E11	116
I/O	0	P187	A7	A10	119
I/O	0	-	D8	B10	122
I/O	0	P188	A6	C10	125
I/O, V _{REF}	0	P189	B7	A9	128
V _{CCO}	0	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	P190	GND*	GND*	-
I/O	0	P191	C8	B9	131
I/O	0	P192	D7	E10	134
I/O	0	-	-	D10	140
I/O	0	P193	E7	A8	143
I/O	0	-	-	D9	146
I/O	0	-	-	B8	149
I/O	0	P194	C7	E9	155
I/O	0	P195	B6	A7	158

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V _{CCINT}	-	P196	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	0	P197	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	P198	GND*	GND*	-
I/O	0	P199	A5	B7	161
I/O, V _{REF}	0	P200	C6	E8	164
I/O	0	-	-	D8	167
I/O	0	P201	B5	C7	170
I/O	0	-	D6	D7	173
I/O	0	-	-	B6	176
I/O	0	-	-	A5	179
I/O	0	P202	A4	D6	182
I/O, V _{REF}	0	P203	B4	C6	185
V _{CCO}	0	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	-	GND*	GND*	-
I/O	0	P204	E6	B5	188
I/O	0	-	D5	E7	191
I/O	0	-	-	A4	194
I/O	0	-	-	E6	197
I/O	0	P205	A3	B4	200
GND	-	-	GND*	GND*	-
I/O	0	-	C5	A3	203
I/O	0	-	-	B3	206
I/O	0	-	-	D5	209
I/O	0	P206	B3	C5	212
TCK	-	P207	C4	C4	-
V _{CCO}	0	P208	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
V _{CCO}	7	P208	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-

04/18/01

Notes:

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on V_{CCO} banking.

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	6	-	-	T2	449
I/O	6	P43	L4	U1	452
GND	-	-	GND*	GND*	-
I/O	6	-	M2	R5	455
I/O	6	-	-	V1	458
I/O	6	-	-	T5	461
I/O	6	P44	L3	U2	464
I/O, V _{REF}	6	P45	N1	T3	467
V _{CCO}	6	-	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-
I/O	6	P46	P1	T4	470
I/O	6	-	L5	W1	473
GND	-	-	GND*	GND*	-
I/O	6	-	-	V2	476
I/O	6	-	-	U4	482
I/O, V _{REF}	6	P47	N2	Y1	485
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	488
I/O	6	-	-	V3	491
I/O	6	-	-	V4	494
I/O	6	P48	R1	Y2	500
I/O	6	P49	M3	W3	503
M1	-	P50	P2	U5	506
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	507
V _{CCO}	6	P53	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
V _{CCO}	5	P53	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
M2	-	P54	R3	Y4	508
I/O	5	-	-	W5	518
I/O	5	-	-	AB3	521
I/O	5	-	N5	V7	524
GND	-	-	GND*	GND*	-
I/O, V _{REF}	5	P57	T2	Y6	527
I/O	5	-	-	AA4	530
I/O	5	-	-	AB4	536
I/O	5	-	P5	W6	539
I/O	5	P58	T3	Y7	542
GND	-	-	GND*	GND*	-

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V _{CCO}	5	-	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
I/O, V _{REF}	5	P59	T4	AA5	545
I/O	5	P60	M6	AB5	548
I/O	5	-	-	V8	551
I/O	5	-	-	AA6	554
I/O	5	-	T5	AB6	557
GND	-	-	GND*	GND*	-
I/O	5	P61	N6	AA7	560
I/O	5	-	-	W7	563
I/O, V _{REF}	5	P62	R5	W8	569
I/O	5	P63	P6	Y8	572
GND	-	P64	GND*	GND*	-
V _{CCO}	5	P65	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCINT}	-	P66	V _{CCINT} *	V _{CCINT} *	-
I/O	5	P67	R6	AA8	575
I/O	5	P68	M7	V9	578
I/O	5	-	-	AB8	581
I/O	5	-	-	W9	584
I/O	5	-	-	AB9	587
GND	-	-	GND*	GND*	-
I/O	5	P69	N7	Y9	590
I/O	5	-	-	V10	593
I/O	5	-	-	AA9	596
I/O	5	P70	T6	W10	599
I/O	5	P71	P7	AB10	602
GND	-	P72	GND*	GND*	-
V _{CCO}	5	-	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
I/O, V _{REF}	5	P73	P8	Y10	605
I/O	5	P74	R7	V11	608
I/O	5	-	-	AA10	614
I/O	5	-	T7	W11	617
I/O	5	P75	T8	AB11	620
I/O	5	-	-	U11	623
V _{CCINT}	-	P76	V _{CCINT} *	V _{CCINT} *	-
I, GCK1	5	P77	R8	Y11	635
V _{CCO}	5	P78	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCO}	4	P78	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V _{CCO}	1	P156	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
TDO	2	P157	B14	A21	-
GND	-	P158	GND*	GND*	-
TDI	-	P159	A15	B20	-
I/O (\overline{CS})	1	P160	B13	C19	0
I/O (\overline{WRITE})	1	P161	C13	A20	3
I/O	1	-	-	B19	9
I/O	1	-	-	C18	12
I/O	1	-	C12	D17	15
GND	-	-	GND*	GND*	-
I/O, V _{REF}	1	P162	A14	A19	18
I/O	1	-	-	B18	21
I/O	1	-	-	E16	27
I/O	1	-	D12	C17	30
I/O	1	P163	B12	D16	33
GND	-	-	GND*	GND*	-
V _{CCO}	1	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P164	C11	A18	36
I/O	1	P165	A13	B17	39
I/O	1	-	-	E15	42
I/O	1	-	-	A17	45
I/O	1	-	D11	D15	48
GND	-	-	GND*	GND*	-
I/O	1	P166	A12	C16	51
I/O	1	-	-	D14	54
I/O, V _{REF}	1	P167	E11	E14	60
I/O	1	P168	B11	A16	63
GND	-	P169	GND*	GND*	-
V _{CCO}	1	P170	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCINT}	-	P171	V _{CCINT} *	V _{CCINT} *	-
I/O	1	P172	A11	C15	66
I/O	1	P173	C10	B15	69
I/O	1	-	-	E13	72
I/O	1	-	-	A15	75
I/O	1	-	-	F12	78
GND	-	-	GND*	GND*	-
I/O	1	P174	B10	C14	81
I/O	1	-	-	B14	84
I/O	1	-	-	A14	87

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	1	P175	D10	D13	90
I/O	1	P176	A10	C13	93
GND	-	P177	GND*	GND*	-
V _{CCO}	1	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P178	B9	B13	96
I/O	1	P179	E10	E12	99
I/O	1	-	-	A13	105
I/O	1	-	A9	B12	108
I/O	1	P180	D9	D12	111
I/O	1	-	-	C12	114
I/O	1	P181	A8	D11	120
I, GCK2	1	P182	C9	A11	126
GND	-	P183	GND*	GND*	-
V _{CCO}	1	P184	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCO}	0	P184	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
I, GCK3	0	P185	B8	C11	127
V _{CCINT}	-	P186	V _{CCINT} *	V _{CCINT} *	-
I/O	0	-	-	E11	137
I/O	0	P187	A7	A10	140
I/O	0	-	D8	B10	143
I/O	0	-	-	F11	146
I/O	0	P188	A6	C10	152
I/O, V _{REF}	0	P189	B7	A9	155
V _{CCO}	0	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	P190	GND*	GND*	-
I/O	0	P191	C8	B9	158
I/O	0	P192	D7	E10	161
I/O	0	-	-	C9	164
I/O	0	-	-	D10	167
I/O	0	P193	E7	A8	170
GND	-	-	GND*	GND*	-
I/O	0	-	-	D9	173
I/O	0	-	-	B8	176
I/O	0	-	-	C8	179
I/O	0	P194	C7	E9	182
I/O	0	P195	B6	A7	185
V _{CCINT}	-	P196	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	0	P197	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-