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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 600 |
| Number of Logic Elements/Cells | 2700 |
| Total RAM Bits | 40960 |
| Number of I/O | 92 |
| Number of Gates | 100000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s100-5tq144i |

## General Overview

The Spartan-II family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-II FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes.

Spartan-II FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-II FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-II FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-II devices provide system clock rates up to 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-II FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

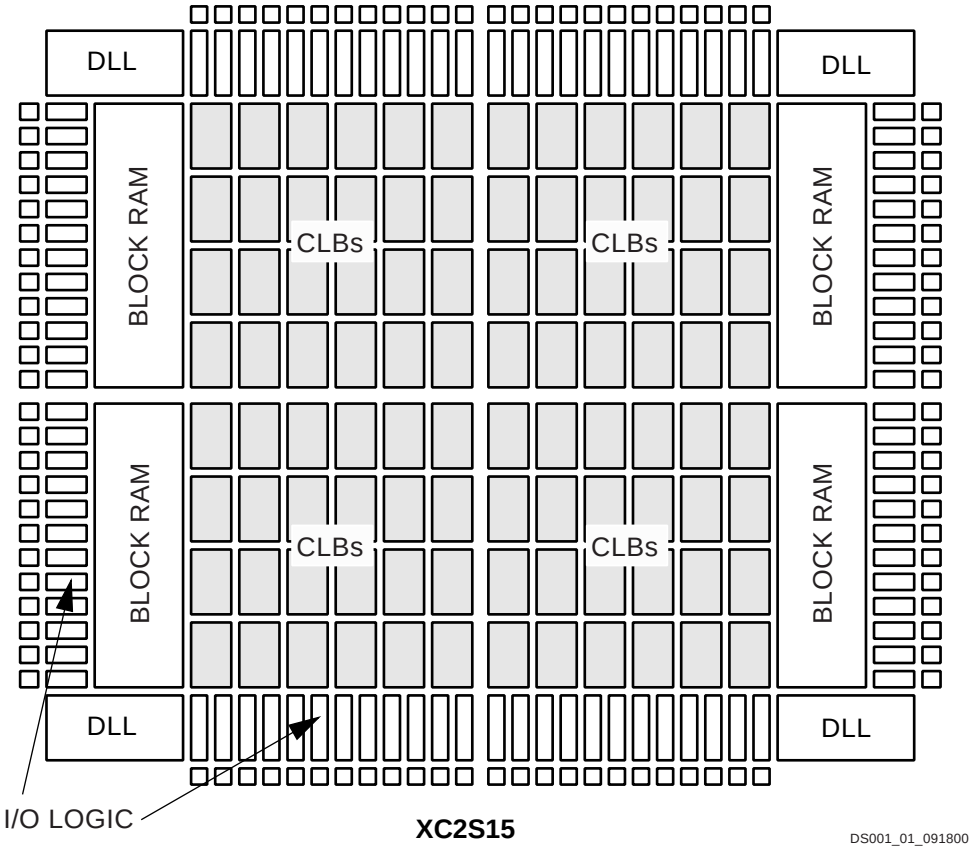



*Figure 1:* **Basic Spartan-II Family FPGA Block Diagram**

## Spartan-II Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination. The four global clock pins are usable as additional user I/Os when not used as a global clock pin. These pins are not included in user I/O counts.

*Table 2:* **Spartan-II FPGA User I/O Chart(1)**

| Device | Maximum User I/O | Available User I/O According to Package Type | | | | | |
|---|---|---|---|---|---|---|---|
| | | VQ100 VQG100 | TQ144 TQG144 | CS144 CSG144 | PQ208 PQG208 | FG256 FGG256 | FG456 FGG456 |
| XC2S15 | 86 | 60 | 86 | (Note 2) | - | - | - |
| XC2S30 | 92 | 60 | 92 | 92 | (Note 2) | - | - |
| XC2S50 | 176 | - | 92 | - | 140 | 176 | - |
| XC2S100 | 176 | - | 92 | - | 140 | 176 | (Note 2) |
| XC2S150 | 260 | - | - | - | 140 | 176 | 260 |
| XC2S200 | 284 | - | - | - | 140 | 176 | 284 |

**Notes:**
1. All user I/O counts do not include the four global clock/user input pins.
2. Discontinued by PDN2004-01.

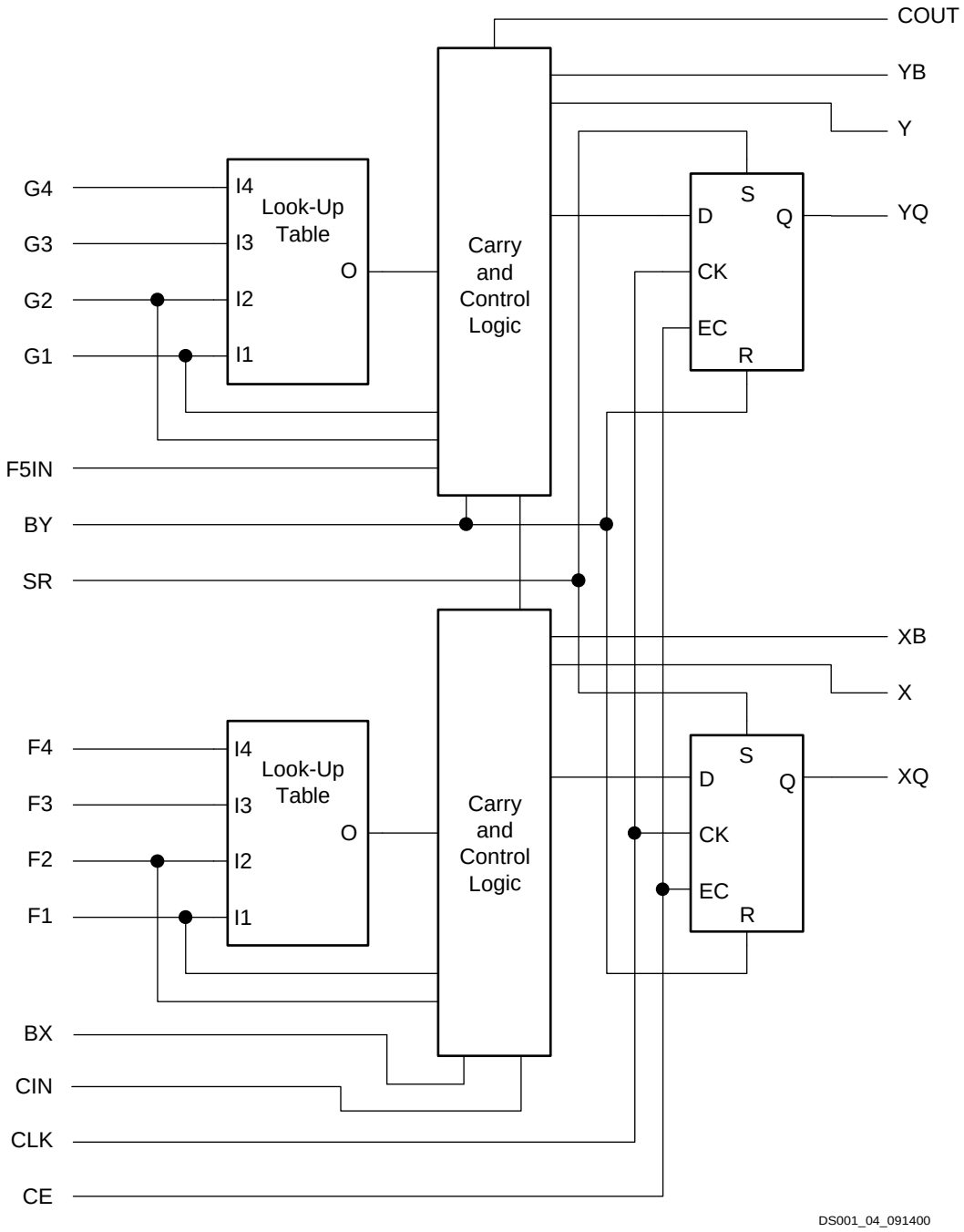



*Figure 4:* **Spartan-II CLB Slice** (two identical slices in each CLB)

### *Storage Elements*

Storage elements in the Spartan-II FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

### *Additional Logic*

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

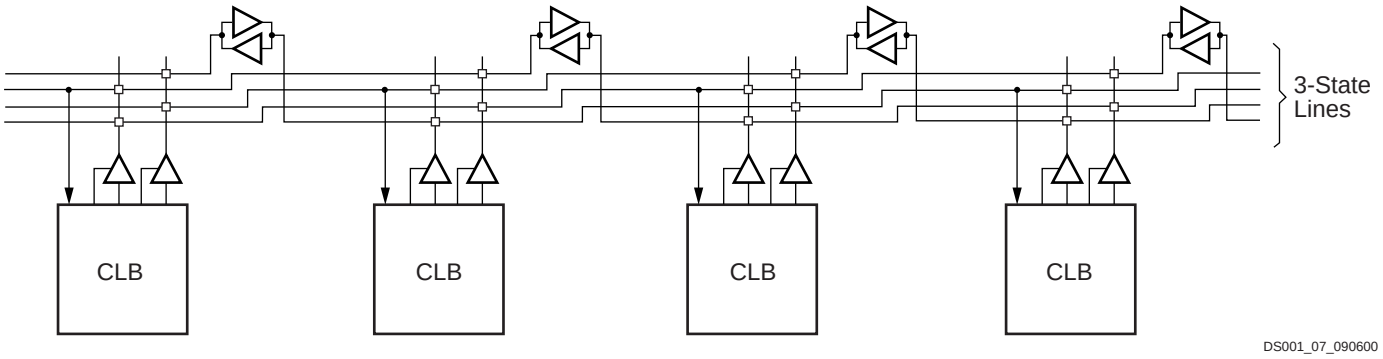



*Figure 7:* **BUFT Connections to Dedicated Horizontal Bus Lines**

## Clock Distribution

The Spartan-II family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 8.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing. Global clock pins do not have the option for internal, weak pull-up resistors.

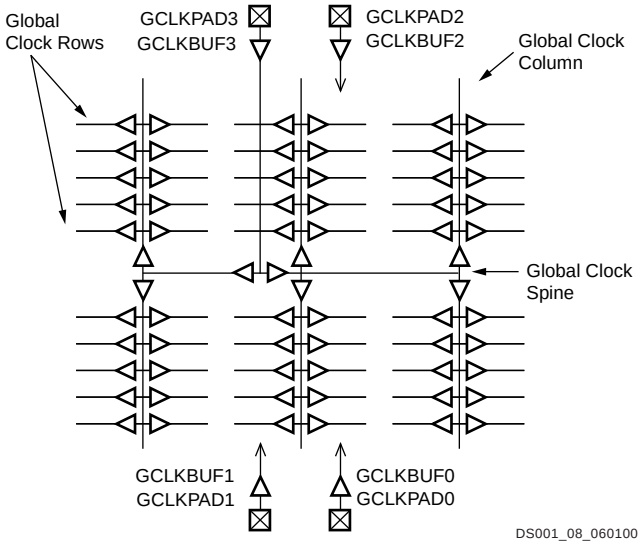



*Figure 8:* **Global Clock Distribution Network**

### *Delay-Locked Loop (DLL)*

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-II devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

## Boundary Scan

Spartan-II devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the $V_{CCO}$ for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and $V_{CCO}$. TDI, TMS, and TCK have a default internal weak pull-up resistor, and TDO has no default resistor. Bitstream options allow setting any of the four TAP pins to have an internal pull-up, pull-down, or neither.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The default timing for start-up is shown in the top half of Figure 13. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx software. Heavy lines show default settings.

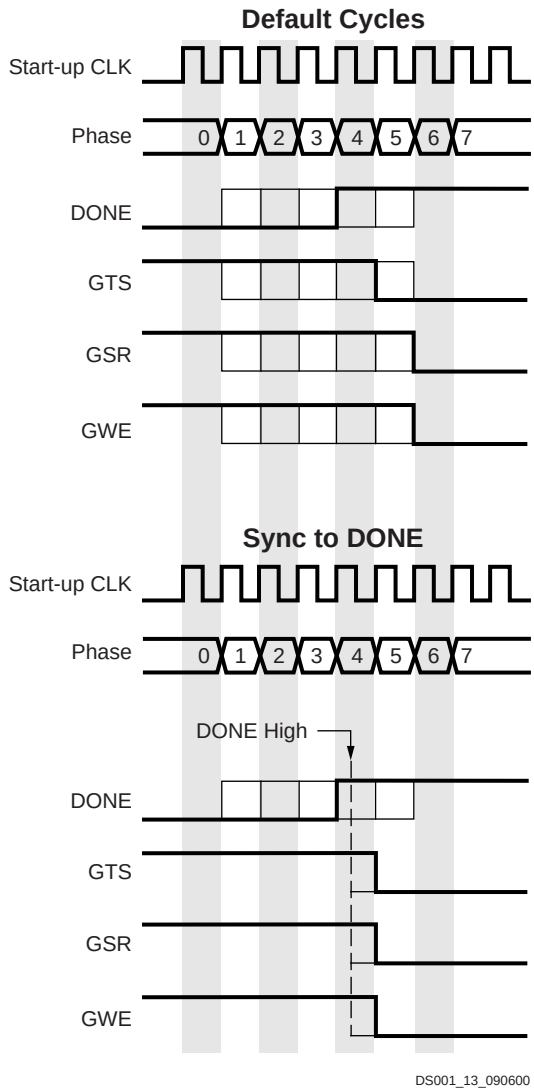



*Figure 13:* **Start-Up Waveforms**

The bottom half of Figure 13 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

## Serial Modes

There are two serial configuration modes: In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 14 for the sequence for loading data into the Spartan-II FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 11. Note that $\overline{CS}$ and $\overline{WRITE}$ normally are not used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{WRITE}$ with $\overline{CS}$ Low during serial configuration.

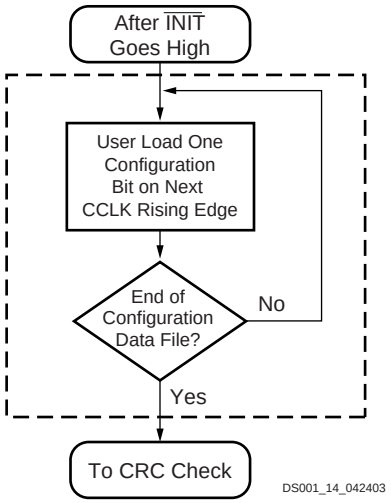



*Figure 14:* **Loading Serial Mode Configuration Data**

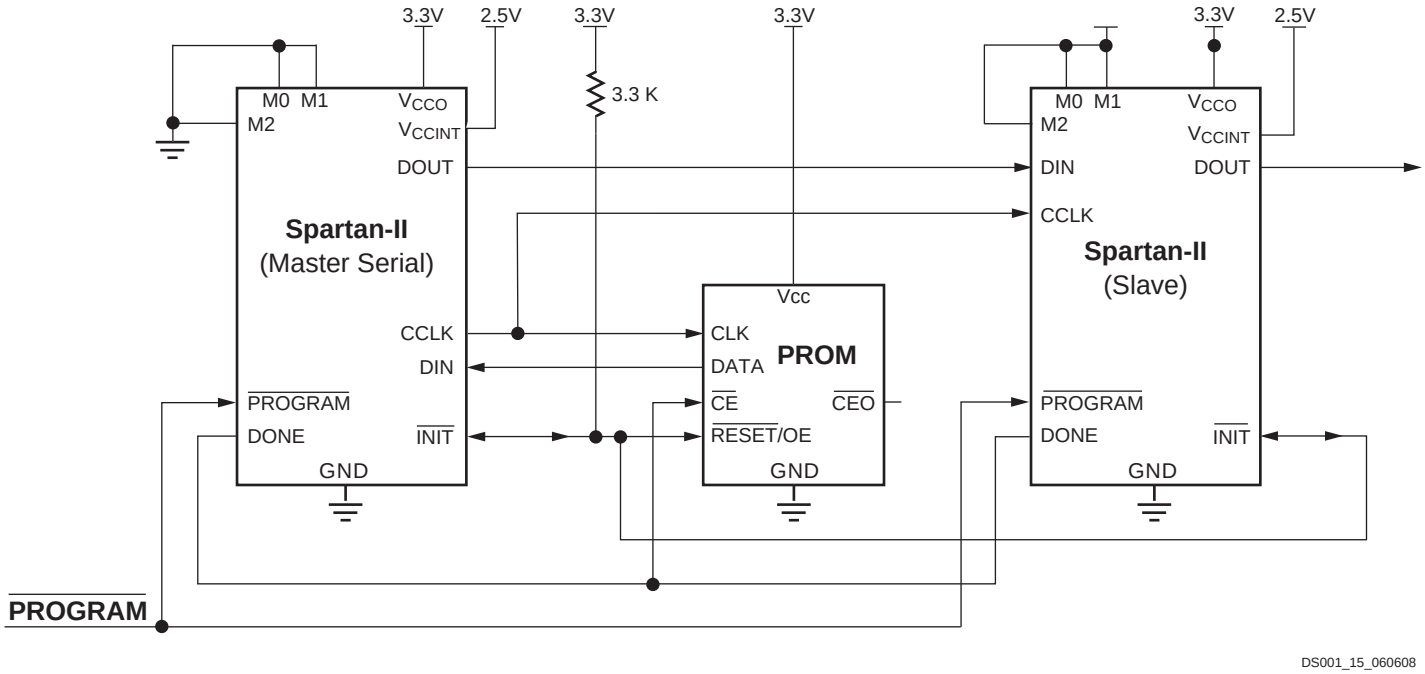
### *Slave Serial Mode*

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is $2^{20}$-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.




**Notes:**
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

*Figure 15:* **Master/Slave Serial Configuration Circuit Diagram**

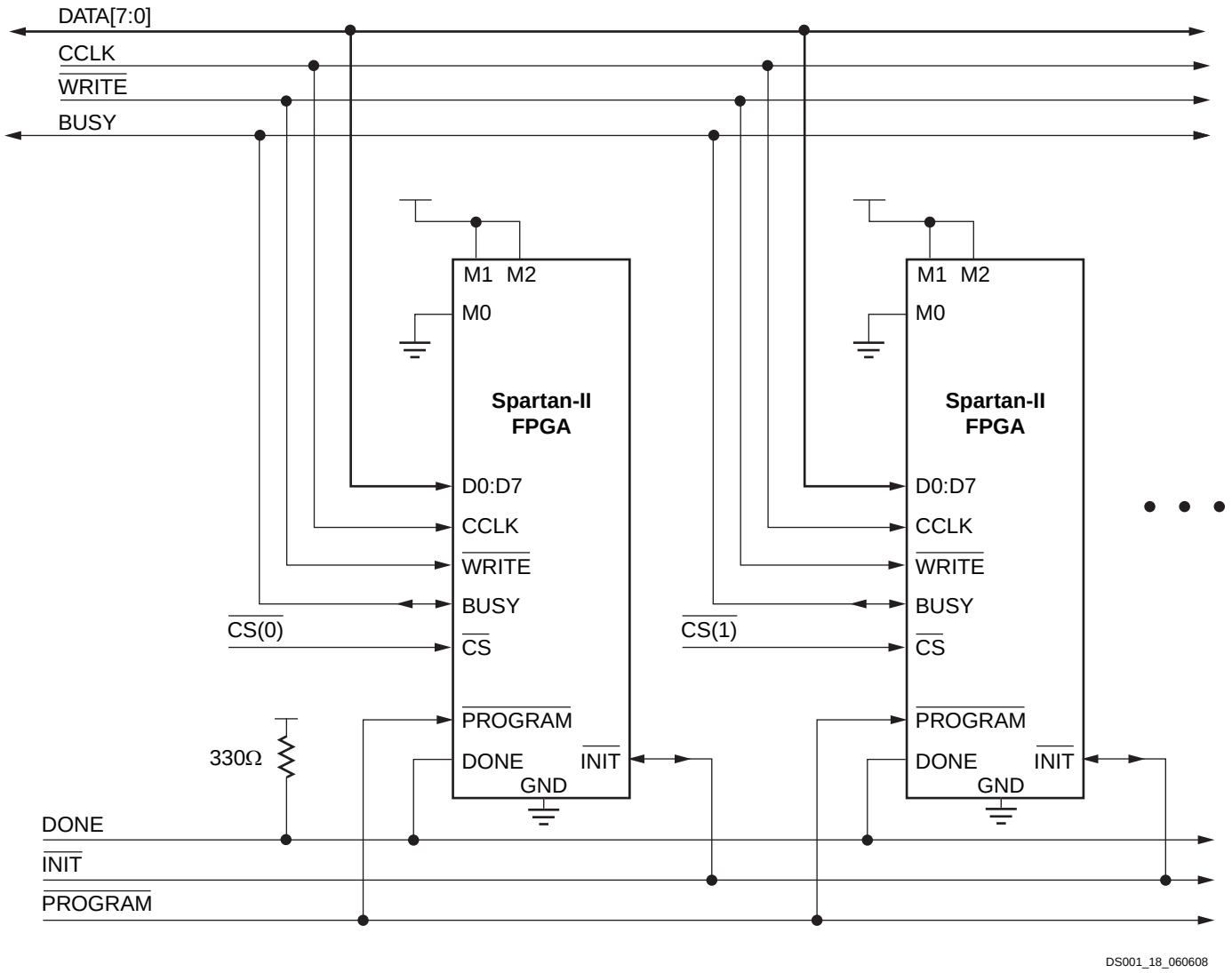



*Figure 18:* **Slave Parallel Configuration Circuit Diagram**

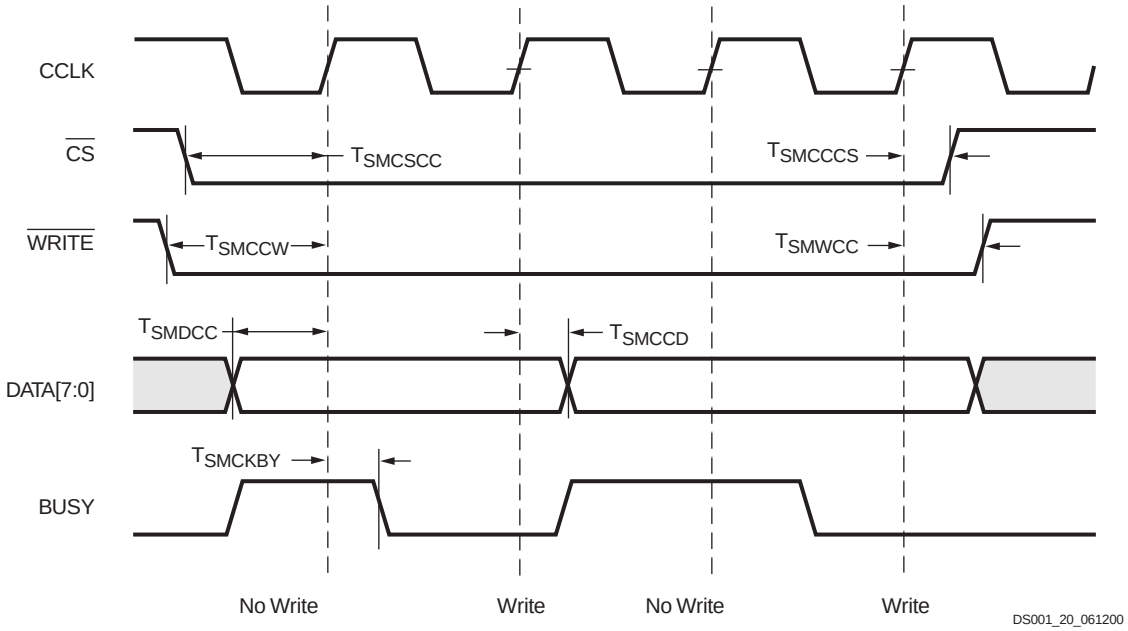
Multiple Spartan-II FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See "Start-up," page 19.

### *Write*

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 19, page 25 shows a flowchart of the write sequence used to load data into the Spartan-II FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 11, page 18. The timing for write operations is shown in Figure 20, page 26.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.




| Symbol | | Description | | Units |
|---|---|---|---|---|
| $T_{SMDCC}$ | CCLK | D0-D7 setup/hold | 5 | ns, min |
| $T_{SMCCD}$ | | D0-D7 hold | 0 | ns, min |
| $T_{SMCSCC}$ | | $\overline{CS}$ setup | 7 | ns, min |
| $T_{SMCCCS}$ | | $\overline{CS}$ hold | 0 | ns, min |
| $T_{SMCCW}$ | | $\overline{WRITE}$ setup | 7 | ns, min |
| $T_{SMWCC}$ | | $\overline{WRITE}$ hold | 0 | ns, min |
| $T_{SMCKBY}$ | | BUSY propagation delay | 12 | ns, max |
| $F_{CC}$ | | Maximum frequency | 66 | MHz, max |
| $F_{CCNH}$ | | Maximum frequency with no handshake | 50 | MHz, max |

*Figure 20:* **Slave Parallel Write Timing**

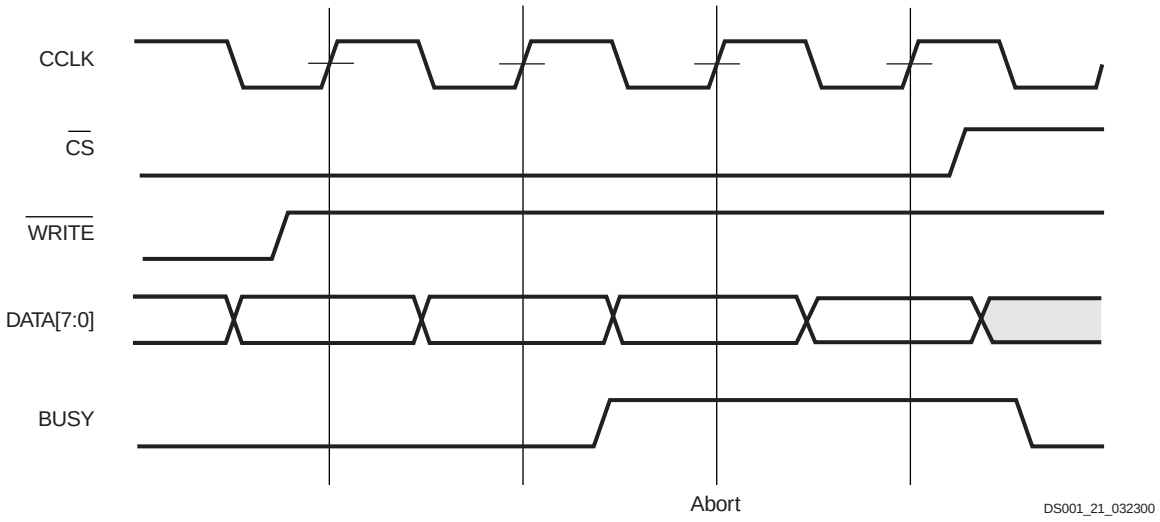



*Figure 21:* **Slave Parallel Write Abort Waveforms**

### LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 32 for the LVTTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 32:* **LVTTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 2.0 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.8 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –24 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 | - | - |

**Notes:**
1. $V_{OL}$ and $V_{OH}$ for lower drive currents sample tested.

### LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 33 for the LVCMOS2 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 33:* **LVCMOS2 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.7 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.7 |
| $V_{OH}$ | 1.9 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –12 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 12 | - | - |

### AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 34 for the AGP-2X standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 34:* **AGP-2X Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = N \times V_{CCO}$ (1) | 1.17 | 1.32 | 1.48 |
| $V_{TT}$ | - | - | - |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.37 | 1.52 | - |
| $V_{IL} \leq V_{REF} - 0.2$ | - | 1.12 | 1.28 |
| $V_{OH} \geq 0.9 \times V_{CCO}$ | 2.7 | 3.0 | - |
| $V_{OL} \leq 0.1 \times V_{CCO}$ | - | 0.33 | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 2 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 2 | - | - |

**Notes:**
1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

For design examples and more information on using the I/O, see XAPP179, *Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs*.

## Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All limits are representative of worst-case supply voltage and junction temperature conditions. Typical numbers are based on measurements taken at a nominal $V_{CCINT}$ level of 2.5V and a junction temperature of 25°C. The parameters included are common to popular designs and typical applications. **All specifications are subject to change without notice.**

## DC Specifications

### Absolute Maximum Ratings(1)

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage relative to GND(2) | | –0.5 | 3.0 | V |
| $V_{CCO}$ | Supply voltage relative to GND(2) | | –0.5 | 4.0 | V |
| $V_{REF}$ | Input reference voltage | | –0.5 | 3.6 | V |
| $V_{IN}$ | Input voltage relative to GND(3) | 5V tolerant I/O(4) | –0.5 | 5.5 | V |
| | | No 5V tolerance(5) | –0.5 | $V_{CCO}$ + 0.5 | V |
| $V_{TS}$ | Voltage applied to 3-state output | 5V tolerant I/O(4) | –0.5 | 5.5 | V |
| | | No 5V tolerance(5) | –0.5 | $V_{CCO}$ + 0.5 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 | +150 | °C |
| $T_J$ | Junction temperature | | - | +125 | °C |

**Notes:**
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Power supplies may turn on in any order.
3. $V_{IN}$ should not exceed $V_{CCO}$ by more than 3.6V over extended periods of time (e.g., longer than a day).
4. Spartan®-II device I/Os are 5V Tolerant whenever the LVTTL, LVCMOS2, or PCI33_5 signal standard has been selected. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA, and undershoot must be limited to either –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to +7.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
5. Without 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either $V_{CCO}$ + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to $V_{CCO}$ + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the Packaging Information on the Xilinx® web site.

## Power-On Requirements

Spartan-II FPGAs require that a minimum supply current $I_{CCPO}$ be provided to the $V_{CCINT}$ lines for a successful power-on. If more current is available, the FPGA can consume more than $I_{CCPO}$ minimum, though this cannot adversely affect reliability.

A maximum limit for $I_{CCPO}$ is not specified. Therefore the use of foldback/crowbar supplies and fuses deserves special attention. In these cases, limit the $I_{CCPO}$ current to a level below the trip point for over-current protection in order to avoid inadvertently shutting down the supply.

| Symbol | Description | Conditions | | New Requirements(1) For Devices with Date Code 0321 or Later | | Old Requirements(1) For Devices with Date Code before 0321 | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Junction Temperature(2) | Device Temperature Grade | Min | Max | Min | Max | |
| $I_{CCPO}$(3) | Total $V_{CCINT}$ supply current required during power-on | –40°C ≤ $T_J$ <–20°C | Industrial | 1.50 | - | 2.00 | - | A |
| | | –20°C ≤ $T_J$ < 0°C | Industrial | 1.00 | - | 2.00 | - | A |
| | | 0°C ≤ $T_J$ ≤ 85°C | Commercial | 0.25 | - | 0.50 | - | A |
| | | 85°C < $T_J$ ≤ 100°C | Industrial | 0.50 | - | 0.50 | - | A |
| $T_{CCPO}$(4,5) | $V_{CCINT}$ ramp time | –40°C≤ $T_J$≤ 100°C | All | - | 50 | - | 50 | ms |

**Notes:**

1. The date code is printed on the top of the device's package. See the "Device Part Marking" section in Module 1.
2. The expected $T_J$ range for the design determines the $I_{CCPO}$ minimum requirement. Use the applicable ranges in the junction temperature column to find the associated current values in the appropriate new or old requirements column according to the date code. Then choose the highest of these current values to serve as the minimum $I_{CCPO}$ requirement that must be met. For example, if the junction temperature for a given design is -25°C ≤ $T_J$ ≤ 75°C, then the new minimum $I_{CCPO}$ requirement is 1.5A. If 5°C ≤ $T_J$ ≤ 90°C, then the new minimum $I_{CCPO}$ requirement is 0.5A.
3. The $I_{CCPO}$ requirement applies for a brief time (commonly only a few milliseconds) when $V_{CCINT}$ ramps from 0 to 2.5V.
4. The ramp time is measured from GND to $V_{CCINT}$ max on a fully loaded board.
5. During power-on, the $V_{CCINT}$ ramp must increase steadily in voltage with no dips.
6. For more information on designing to meet the power-on specifications, refer to the application note **XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families"**

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $V_{OL}$ and $V_{OH}$ are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum $V_{CCO}$ with the respective $I_{OL}$ and $I_{OH}$ currents shown. Other standards are sample tested.

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| LVTTL(1) | –0.5 | 0.8 | 2.0 | 5.5 | 0.4 | 2.4 | 24 | –24 |
| LVCMOS2 | –0.5 | 0.7 | 1.7 | 5.5 | 0.4 | 1.9 | 12 | –12 |
| PCI, 3.3V | –0.5 | 44% $V_{CCINT}$ | 60% $V_{CCINT}$ | $V_{CCO}$ + 0.5 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note (2) | Note (2) |
| PCI, 5.0V | –0.5 | 0.8 | 2.0 | 5.5 | 0.55 | 2.4 | Note (2) | Note (2) |
| GTL | –0.5 | $V_{REF}$ – 0.05 | $V_{REF}$ + 0.05 | 3.6 | 0.4 | N/A | 40 | N/A |
| GTL+ | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.6 | N/A | 36 | N/A |
| HSTL I | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 8 | –8 |
| HSTL III | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 24 | –8 |
| HSTL IV | –0.5 | $V_{REF}$ – 0.1 | $V_{REF}$ + 0.1 | 3.6 | 0.4 | $V_{CCO}$ – 0.4 | 48 | –8 |
| SSTL3 I | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.6 | $V_{REF}$ + 0.6 | 8 | –8 |
| SSTL3 II | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | 16 | –16 |
| SSTL2 I | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.6 | $V_{REF}$ + 0.6 | 7.6 | –7.6 |
| SSTL2 II | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | 15.2 | –15.2 |

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| CTT | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.4 | $V_{REF}$ + 0.4 | 8 | –8 |
| AGP | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note (2) | Note (2) |

**Notes:**
1. $V_{OL}$ and $V_{OH}$ for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

## Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

### Global Clock Input to Output Delay for LVTTL, *with* DLL (Pin-to-Pin)(1)

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | All | -6 | -5 | |
| | | | Min | Max | Max | |
| $T_{ICKOFDLL}$ | Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *with* DLL. | All | | 2.9 | 3.3 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

### Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)(1)

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | All | -6 | -5 | |
| | | | Min | Max | Max | |
| $T_{ICKOF}$ | Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *without* DLL. | XC2S15 | | 4.5 | 5.4 | ns |
| | | XC2S30 | | 4.5 | 5.4 | ns |
| | | XC2S50 | | 4.5 | 5.4 | ns |
| | | XC2S100 | | 4.6 | 5.5 | ns |
| | | XC2S150 | | 4.6 | 5.5 | ns |
| | | XC2S200 | | 4.7 | 5.6 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

## IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Delay Adjustments for Different Standards," page 57.

| Symbol | Description | Device | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | -6 | | -5 | | |
| | | | Min | Max | Min | Max | |
| **Propagation Delays** | | | | | | | |
| $T_{IOPI}$ | Pad to I output, no delay | All | - | 0.8 | - | 1.0 | ns |
| $T_{IOPID}$ | Pad to I output, with delay | All | - | 1.5 | - | 1.8 | ns |
| $T_{IOPLI}$ | Pad to output IQ via transparent latch, no delay | All | - | 1.7 | - | 2.0 | ns |
| $T_{IOPLID}$ | Pad to output IQ via transparent latch, with delay | XC2S15 | - | 3.8 | - | 4.5 | ns |
| | | XC2S30 | - | 3.8 | - | 4.5 | ns |
| | | XC2S50 | - | 3.8 | - | 4.5 | ns |
| | | XC2S100 | - | 3.8 | - | 4.5 | ns |
| | | XC2S150 | - | 4.0 | - | 4.7 | ns |
| | | XC2S200 | - | 4.0 | - | 4.7 | ns |
| **Sequential Delays** | | | | | | | |
| $T_{IOCKIQ}$ | Clock CLK to output IQ | All | - | 0.7 | - | 0.8 | ns |
| **Setup/Hold Times with Respect to Clock CLK(2)** | | | | | | | |
| $T_{IOPICK}$ / $T_{IOICKP}$ | Pad, no delay | All | 1.7 / 0 | - | 1.9 / 0 | - | ns |
| $T_{IOPICKD}$ / $T_{IOICKPD}$ | Pad, with delay(1) | XC2S15 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S30 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S50 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S100 | 3.8 / 0 | - | 4.4 / 0 | - | ns |
| | | XC2S150 | 3.9 / 0 | - | 4.6 / 0 | - | ns |
| | | XC2S200 | 3.9 / 0 | - | 4.6 / 0 | - | ns |
| $T_{IOICECK}$ / $T_{IOCKICE}$ | ICE input | All | 0.9 / 0.01 | - | 0.9 / 0.01 | - | ns |
| **Set/Reset Delays** | | | | | | | |
| $T_{IOSRCKI}$ | SR input (IFF, synchronous) | All | - | 1.1 | - | 1.2 | ns |
| $T_{IOSRIQ}$ | SR input to IQ (asynchronous) | All | - | 1.5 | - | 1.7 | ns |
| $T_{GSRQ}$ | GSR to output IQ | All | - | 9.9 | - | 11.7 | ns |

**Notes:**
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.
2. A zero hold time listing indicates no hold time or a negative hold time.

## DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| $F_{CLKINHF}$ | Input clock frequency (CLKDLLHF) | 60 | 200 | 60 | 180 | MHz |
| $F_{CLKINLF}$ | Input clock frequency (CLKDLL) | 25 | 100 | 25 | 90 | MHz |
| $T_{DLLPWHF}$ | Input clock pulse width (CLKDLLHF) | 2.0 | - | 2.4 | - | ns |
| $T_{DLLPWLF}$ | Input clock pulse width (CLKDLL) | 2.5 | - | 3.0 | - | ns |

## DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Figure 52, page 63, provides definitions for various parameters in the table below.

| Symbol | Description | $F_{CLKIN}$ | CLKDLLHF | | CLKDLL | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $T_{IPTOL}$ | Input clock period tolerance | | - | 1.0 | - | 1.0 | ns |
| $T_{IJITCC}$ | Input clock jitter tolerance (cycle-to-cycle) | | - | ±150 | - | ±300 | ps |
| $T_{LOCK}$ | Time required for DLL to acquire lock | > 60 MHz | - | 20 | - | 20 | µs |
| | | 50-60 MHz | - | - | - | 25 | µs |
| | | 40-50 MHz | - | - | - | 50 | µs |
| | | 30-40 MHz | - | - | - | 90 | µs |
| | | 25-30 MHz | - | - | - | 120 | µs |
| $T_{OJITCC}$ | Output jitter (cycle-to-cycle) for any DLL clock output(1) | | - | ±60 | - | ±60 | ps |
| $T_{PHIO}$ | Phase offset between CLKIN and CLKO(2) | | - | ±100 | - | ±100 | ps |
| $T_{PHOO}$ | Phase offset between clock outputs on the DLL(3) | | - | ±140 | - | ±140 | ps |
| $T_{PHIOM}$ | Maximum phase difference between CLKIN and CLKO(4) | | - | ±160 | - | ±160 | ps |
| $T_{PHOOM}$ | Maximum phase difference between clock outputs on the DLL(5) | | - | ±200 | - | ±200 | ps |

**Notes:**

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

## Package Thermal Characteristics

Table 39 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance ($\theta_{JC}$) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board ($\theta_{JB}$) value similarly reports the difference between the board and junction temperature. The junction-to-ambient ($\theta_{JA}$) value reports the temperature difference between the ambient environment and the junction temperature. The $\theta_{JA}$ value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the $\theta_{JA}$ value in a system without a fan. The thermal resistance drops with increasing air flow.

*Table 39:* **Spartan-II Package Thermal Characteristics**

| Package | Device | Junction-to-Case ($\theta_{JC}$) | Junction-to-Board ($\theta_{JB}$) | Junction-to-Ambient ($\theta_{JA}$) at Different Air Flows | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Still Air (0 LFM) | 250 LFM | 500 LFM | 750 LFM | |
| VQ100 VQG100 | XC2S15 | 11.3 | N/A | 44.1 | 36.7 | 34.2 | 33.3 | °C/Watt |
| | XC2S30 | 10.1 | N/A | 40.7 | 33.9 | 31.5 | 30.8 | °C/Watt |
| TQ144 TQG144 | XC2S15 | 7.3 | N/A | 38.6 | 30.0 | 25.7 | 24.1 | °C/Watt |
| | XC2S30 | 6.7 | N/A | 34.7 | 27.0 | 23.1 | 21.7 | °C/Watt |
| | XC2S50 | 5.8 | N/A | 32.2 | 25.1 | 21.4 | 20.1 | °C/Watt |
| | XC2S100 | 5.3 | N/A | 31.4 | 24.4 | 20.9 | 19.6 | °C/Watt |
| CS144 CSG144 | XC2S30 | 2.8 | N/A | 34.0 | 26.0 | 23.9 | 23.2 | °C/Watt |
| PQ208 PQG208 | XC2S50 | 6.7 | N/A | 25.2 | 18.6 | 16.4 | 15.2 | °C/Watt |
| | XC2S100 | 5.9 | N/A | 24.6 | 18.1 | 16.0 | 14.9 | °C/Watt |
| | XC2S150 | 5.0 | N/A | 23.8 | 17.6 | 15.6 | 14.4 | °C/Watt |
| | XC2S200 | 4.1 | N/A | 23.0 | 17.0 | 15.0 | 13.9 | °C/Watt |
| FG256 FGG256 | XC2S50 | 7.1 | 17.6 | 27.2 | 21.4 | 20.3 | 19.8 | °C/Watt |
| | XC2S100 | 5.8 | 15.1 | 25.1 | 19.5 | 18.3 | 17.8 | °C/Watt |
| | XC2S150 | 4.6 | 12.7 | 23.0 | 17.6 | 16.3 | 15.8 | °C/Watt |
| | XC2S200 | 3.5 | 10.7 | 21.4 | 16.1 | 14.7 | 14.2 | °C/Watt |
| FG456 FGG456 | XC2S150 | 2.0 | N/A | 21.9 | 17.3 | 15.8 | 15.2 | °C/Watt |
| | XC2S200 | 2.0 | N/A | 21.0 | 16.6 | 15.1 | 14.5 | °C/Watt |

# Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan®-II device. They follow the pad locations around the die, and include Boundary Scan register locations.

## XC2S15 Device Pinouts

| XC2S15 Pad Name | | VQ100 | TQ144 | CS144 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| GND | - | P1 | P143 | A1 | - |
| TMS | - | P2 | P142 | B1 | - |
| I/O | 7 | P3 | P141 | C2 | 77 |
| I/O | 7 | - | P140 | C1 | 80 |
| I/O, $V_{REF}$ | 7 | P4 | P139 | D4 | 83 |
| I/O | 7 | P5 | P137 | D2 | 86 |
| I/O | 7 | P6 | P136 | D1 | 89 |
| GND | - | - | P135 | E4 | - |
| I/O | 7 | P7 | P134 | E3 | 92 |
| I/O | 7 | - | P133 | E2 | 95 |
| I/O, $V_{REF}$ | 7 | P8 | P132 | E1 | 98 |
| I/O | 7 | P9 | P131 | F4 | 101 |
| I/O | 7 | - | P130 | F3 | 104 |
| I/O, IRDY(1) | 7 | P10 | P129 | F2 | 107 |
| GND | - | P11 | P128 | F1 | - |
| $V_{CCO}$ | 7 | P12 | P127 | G2 | - |
| $V_{CCO}$ | 6 | P12 | P127 | G2 | - |
| I/O, TRDY(1) | 6 | P13 | P126 | G1 | 110 |
| $V_{CCINT}$ | - | P14 | P125 | G3 | - |
| I/O | 6 | - | P124 | G4 | 113 |
| I/O | 6 | P15 | P123 | H1 | 116 |
| I/O, $V_{REF}$ | 6 | P16 | P122 | H2 | 119 |
| I/O | 6 | - | P121 | H3 | 122 |
| I/O | 6 | P17 | P120 | H4 | 125 |
| GND | - | - | P119 | J1 | - |
| I/O | 6 | P18 | P118 | J2 | 128 |
| I/O | 6 | P19 | P117 | J3 | 131 |
| I/O, $V_{REF}$ | 6 | P20 | P115 | K1 | 134 |
| I/O | 6 | - | P114 | K2 | 137 |
| I/O | 6 | P21 | P113 | K3 | 140 |
| I/O | 6 | P22 | P112 | L1 | 143 |
| M1 | - | P23 | P111 | L2 | 146 |
| GND | - | P24 | P110 | L3 | - |
| M0 | - | P25 | P109 | M1 | 147 |
| $V_{CCO}$ | 6 | P26 | P108 | M2 | - |
| $V_{CCO}$ | 5 | P26 | P107 | N1 | - |

## XC2S15 Device Pinouts *(Continued)*

| XC2S15 Pad Name | | VQ100 | TQ144 | CS144 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| M2 | - | P27 | P106 | N2 | 148 |
| I/O | 5 | - | P103 | K4 | 155 |
| I/O, $V_{REF}$ | 5 | P30 | P102 | L4 | 158 |
| I/O | 5 | P31 | P100 | N4 | 161 |
| I/O | 5 | P32 | P99 | K5 | 164 |
| GND | - | - | P98 | L5 | - |
| $V_{CCINT}$ | - | P33 | P97 | M5 | - |
| I/O | 5 | - | P96 | N5 | 167 |
| I/O | 5 | - | P95 | K6 | 170 |
| I/O, $V_{REF}$ | 5 | P34 | P94 | L6 | 173 |
| I/O | 5 | - | P93 | M6 | 176 |
| $V_{CCINT}$ | - | P35 | P92 | N6 | - |
| I, GCK1 | 5 | P36 | P91 | M7 | 185 |
| $V_{CCO}$ | 5 | P37 | P90 | N7 | - |
| $V_{CCO}$ | 4 | P37 | P90 | N7 | - |
| GND | - | P38 | P89 | L7 | - |
| I, GCK0 | 4 | P39 | P88 | K7 | 186 |
| I/O | 4 | P40 | P87 | N8 | 190 |
| I/O | 4 | - | P86 | M8 | 193 |
| I/O, $V_{REF}$ | 4 | P41 | P85 | L8 | 196 |
| I/O | 4 | - | P84 | K8 | 199 |
| I/O | 4 | - | P83 | N9 | 202 |
| $V_{CCINT}$ | - | P42 | P82 | M9 | - |
| GND | - | - | P81 | L9 | - |
| I/O | 4 | P43 | P80 | K9 | 205 |
| I/O | 4 | P44 | P79 | N10 | 208 |
| I/O, $V_{REF}$ | 4 | P45 | P77 | L10 | 211 |
| I/O | 4 | - | P76 | N11 | 214 |
| I/O | 4 | P46 | P75 | M11 | 217 |
| I/O | 4 | P47 | P74 | L11 | 220 |
| GND | - | P48 | P73 | N12 | - |
| DONE | 3 | P49 | P72 | M12 | 223 |
| $V_{CCO}$ | 4 | P50 | P71 | N13 | - |
| $V_{CCO}$ | 3 | P50 | P70 | M13 | - |
| $\overline{PROGRAM}$ | - | P51 | P69 | L12 | 226 |
| I/O ($\overline{INIT}$) | 3 | P52 | P68 | L13 | 227 |
| I/O (D7) | 3 | P53 | P67 | K10 | 230 |
| I/O | 3 | - | P66 | K11 | 233 |
| I/O, $V_{REF}$ | 3 | P54 | P65 | K12 | 236 |
| I/O | 3 | P55 | P63 | J10 | 239 |
| I/O (D6) | 3 | P56 | P62 | J11 | 242 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| I/O | 4 | - | - | - | P87 | 295 |
| I/O | 4 | - | - | - | P88 | 298 |
| I/O | 4 | - | P84 | K8 | P89 | 301 |
| I/O | 4 | - | P83 | N9 | P90 | 304 |
| $V_{CCINT}$ | - | P42 | P82 | M9 | P91 | - |
| $V_{CCO}$ | 4 | - | - | - | P92 | - |
| GND | - | - | P81 | L9 | P93 | - |
| I/O | 4 | P43 | P80 | K9 | P94 | 307 |
| I/O | 4 | P44 | P79 | N10 | P95 | 310 |
| I/O | 4 | - | P78 | M10 | P96 | 313 |
| I/O, $V_{REF}$ | 4 | P45 | P77 | L10 | P98 | 316 |
| I/O | 4 | - | - | - | P99 | 319 |
| I/O | 4 | - | P76 | N11 | P100 | 322 |
| I/O | 4 | P46 | P75 | M11 | P101 | 325 |
| I/O | 4 | P47 | P74 | L11 | P102 | 328 |
| GND | - | P48 | P73 | N12 | P103 | - |
| DONE | 3 | P49 | P72 | M12 | P104 | 331 |
| $V_{CCO}$ | 4 | P50 | P71 | N13 | P105 | - |
| $V_{CCO}$ | 3 | P50 | P70 | M13 | P105 | - |
| $\overline{PROGRAM}$ | - | P51 | P69 | L12 | P106 | 334 |
| I/O ($\overline{INIT}$) | 3 | P52 | P68 | L13 | P107 | 335 |
| I/O (D7) | 3 | P53 | P67 | K10 | P108 | 338 |
| I/O | 3 | - | P66 | K11 | P109 | 341 |
| I/O | 3 | - | - | - | P110 | 344 |
| I/O, $V_{REF}$ | 3 | P54 | P65 | K12 | P111 | 347 |
| I/O | 3 | - | P64 | K13 | P113 | 350 |
| I/O | 3 | P55 | P63 | J10 | P114 | 353 |
| I/O (D6) | 3 | P56 | P62 | J11 | P115 | 356 |
| GND | - | - | P61 | J12 | P116 | - |
| $V_{CCO}$ | 3 | - | - | - | P117 | - |
| I/O (D5) | 3 | P57 | P60 | J13 | P119 | 359 |
| I/O | 3 | P58 | P59 | H10 | P120 | 362 |
| I/O | 3 | - | - | - | P121 | 365 |
| I/O | 3 | - | - | - | P122 | 368 |
| I/O | 3 | - | - | - | P123 | 371 |
| GND | - | - | - | - | P124 | - |
| I/O, $V_{REF}$ | 3 | P59 | P58 | H11 | P125 | 374 |
| I/O (D4) | 3 | P60 | P57 | H12 | P126 | 377 |
| I/O | 3 | - | P56 | H13 | P127 | 380 |
| $V_{CCINT}$ | - | P61 | P55 | G12 | P128 | - |
| I/O, TRDY(1) | 3 | P62 | P54 | G13 | P129 | 386 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| $V_{CCO}$ | 3 | P63 | P53 | G11 | P130 | - |
| $V_{CCO}$ | 2 | P63 | P53 | G11 | P130 | - |
| GND | - | P64 | P52 | G10 | P131 | - |
| I/O, IRDY(1) | 2 | P65 | P51 | F13 | P132 | 389 |
| I/O | 2 | - | - | - | P133 | 392 |
| I/O | 2 | - | P50 | F12 | P134 | 395 |
| I/O (D3) | 2 | P66 | P49 | F11 | P135 | 398 |
| I/O, $V_{REF}$ | 2 | P67 | P48 | F10 | P136 | 401 |
| GND | - | - | - | - | P137 | - |
| I/O | 2 | - | - | - | P138 | 404 |
| I/O | 2 | - | - | - | P139 | 407 |
| I/O | 2 | - | - | - | P140 | 410 |
| I/O | 2 | P68 | P47 | E13 | P141 | 413 |
| I/O (D2) | 2 | P69 | P46 | E12 | P142 | 416 |
| $V_{CCO}$ | 2 | - | - | - | P144 | - |
| GND | - | - | P45 | E11 | P145 | - |
| I/O (D1) | 2 | P70 | P44 | E10 | P146 | 419 |
| I/O | 2 | P71 | P43 | D13 | P147 | 422 |
| I/O | 2 | - | P42 | D12 | P148 | 425 |
| I/O, $V_{REF}$ | 2 | P72 | P41 | D11 | P150 | 428 |
| I/O | 2 | - | - | - | P151 | 431 |
| I/O | 2 | - | P40 | C13 | P152 | 434 |
| I/O (DIN, D0) | 2 | P73 | P39 | C12 | P153 | 437 |
| I/O (DOUT, BUSY) | 2 | P74 | P38 | C11 | P154 | 440 |
| CCLK | 2 | P75 | P37 | B13 | P155 | 443 |
| $V_{CCO}$ | 2 | P76 | P36 | B12 | P156 | - |
| $V_{CCO}$ | 1 | P76 | P35 | A13 | P156 | - |
| TDO | 2 | P77 | P34 | A12 | P157 | - |
| GND | - | P78 | P33 | B11 | P158 | - |
| TDI | - | P79 | P32 | A11 | P159 | - |
| I/O ($\overline{CS}$) | 1 | P80 | P31 | D10 | P160 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P81 | P30 | C10 | P161 | 3 |
| I/O | 1 | - | P29 | B10 | P162 | 6 |
| I/O | 1 | - | - | - | P163 | 9 |
| I/O, $V_{REF}$ | 1 | P82 | P28 | A10 | P164 | 12 |
| I/O | 1 | - | - | - | P166 | 15 |
| I/O | 1 | P83 | P27 | D9 | P167 | 18 |
| I/O | 1 | P84 | P26 | C9 | P168 | 21 |
| GND | - | - | P25 | B9 | P169 | - |
| $V_{CCO}$ | 1 | - | - | - | P170 | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| I/O | 2 | - | - | F12 | G20 | 695 |
| I/O | 2 | - | P149 | E15 | F19 | 701 |
| I/O, $V_{REF}$ | 2 | P41 | P150 | F13 | F21 | 704 |
| $V_{CCO}$ | 2 | - | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 2 | - | P151 | E14 | F20 | 707 |
| I/O | 2 | - | - | C16 | F18 | 710 |
| I/O | 2 | - | - | - | E21 | 713 |
| I/O | 2 | P40 | P152 | E13 | D22 | 716 |
| I/O | 2 | - | - | B16 | E20 | 719 |
| I/O (DIN, D0) | 2 | P39 | P153 | D14 | D20 | 725 |
| I/O (DOUT, BUSY) | 2 | P38 | P154 | C15 | C21 | 728 |
| CCLK | 2 | P37 | P155 | D15 | B22 | 731 |
| $V_{CCO}$ | 2 | P36 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| $V_{CCO}$ | 1 | P35 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P34 | P157 | B14 | A21 | - |
| GND | - | P33 | P158 | GND* | GND* | - |
| TDI | - | P32 | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P31 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P30 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | C12 | D17 | 9 |
| I/O | 1 | P29 | P162 | A14 | A19 | 12 |
| I/O | 1 | - | - | - | B18 | 15 |
| I/O | 1 | - | - | D12 | C17 | 18 |
| I/O | 1 | - | P163 | B12 | D16 | 21 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P28 | P164 | C11 | A18 | 24 |
| I/O | 1 | - | P165 | A13 | B17 | 27 |
| I/O | 1 | - | - | D11 | D15 | 33 |
| I/O | 1 | - | P166 | A12 | C16 | 36 |
| I/O | 1 | - | - | - | D14 | 39 |
| I/O, $V_{REF}$ | 1 | P27 | P167 | E11 | E14 | 42 |
| I/O | 1 | P26 | P168 | B11 | A16 | 45 |
| GND | - | P25 | P169 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| $V_{CCO}$ | 1 | - | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P24 | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P23 | P172 | A11 | C15 | 48 |
| I/O | 1 | P22 | P173 | C10 | B15 | 51 |
| I/O | 1 | - | - | - | F12 | 54 |
| I/O | 1 | - | P174 | B10 | C14 | 57 |
| I/O | 1 | - | P175 | D10 | D13 | 63 |
| I/O | 1 | - | P176 | A10 | C13 | 66 |
| GND | - | - | P177 | GND* | GND* | - |
| I/O, $V_{REF}$ | 1 | P21 | P178 | B9 | B13 | 69 |
| I/O | 1 | - | P179 | E10 | E12 | 72 |
| I/O | 1 | - | - | A9 | B12 | 75 |
| I/O | 1 | P20 | P180 | D9 | D12 | 78 |
| I/O | 1 | P19 | P181 | A8 | D11 | 84 |
| I, GCK2 | 1 | P18 | P182 | C9 | A11 | 90 |
| GND | - | P17 | P183 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P16 | P184 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P16 | P184 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P15 | P185 | B8 | C11 | 91 |
| $V_{CCINT}$ | - | P14 | P186 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 0 | P13 | P187 | A7 | A10 | 101 |
| I/O | 0 | - | - | D8 | B10 | 104 |

## Additional XC2S100 Package Pins

**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P104 | P105 | - | - | - | - |

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**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

11/02/00

**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

11/02/00

**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |

## Additional XC2S100 Package Pins *(Continued)*

| | | | | | |
|---|---|---|---|---|---|
| F10 | F7 | F8 | F9 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U10 | U7 | U8 | U9 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A4 | A5 | A6 | A12 | A13 |
| A14 | A15 | A17 | B3 | B6 | B8 |
| B11 | B14 | B16 | B19 | C1 | C2 |
| C8 | C9 | C12 | C18 | C22 | D1 |
| D4 | D5 | D10 | D18 | D19 | D21 |
| E4 | E11 | E13 | E15 | E16 | E17 |
| E19 | E22 | F4 | F11 | F22 | G2 |
| G3 | G4 | G19 | G22 | H1 | H21 |
| J1 | J3 | J4 | J19 | J20 | K2 |
| K18 | K19 | L2 | L5 | L18 | L19 |
| M2 | M6 | M17 | M18 | M21 | N1 |
| N5 | N19 | P1 | P5 | P19 | P22 |
| R1 | R3 | R20 | R22 | T5 | T19 |
| U3 | U11 | U18 | V1 | V2 | V10 |
| V12 | V17 | V3 | V4 | V6 | V8 |
| V20 | V21 | V22 | W4 | W5 | W9 |
| W13 | W14 | W15 | W16 | W19 | Y5 |
| Y14 | Y18 | Y22 | AA1 | AA3 | AA6 |
| AA9 | AA10 | AA11 | AA16 | AA17 | AA18 |
| AA22 | AB3 | AB4 | AB7 | AB8 | AB12 |
| AB14 | AB21 | - | - | - | - |

11/02/00

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 4 | P90 | R11 | AA15 | 595 |
| $V_{CCINT}$ | - | P91 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | P92 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P93 | GND* | GND* | - |
| I/O | 4 | P94 | M11 | Y15 | 598 |
| I/O, $V_{REF}$ | 4 | P95 | T11 | AB16 | 601 |
| I/O | 4 | - | - | AB17 | 604 |
| I/O | 4 | P96 | N11 | V15 | 607 |
| I/O | 4 | - | R12 | Y16 | 610 |
| I/O | 4 | - | - | AA17 | 613 |
| I/O | 4 | - | - | W16 | 616 |
| I/O | 4 | P97 | P11 | AB18 | 619 |
| I/O, $V_{REF}$ | 4 | P98 | T12 | AB19 | 622 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | P99 | T13 | Y17 | 625 |
| I/O | 4 | - | N12 | V16 | 628 |
| I/O | 4 | - | - | AA18 | 631 |
| I/O | 4 | - | - | W17 | 634 |
| I/O | 4 | P100 | R13 | AB20 | 637 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | P12 | AA19 | 640 |
| I/O | 4 | - | - | V17 | 643 |
| I/O | 4 | - | - | Y18 | 646 |
| I/O | 4 | P101 | P13 | AA20 | 649 |
| I/O | 4 | P102 | T14 | W18 | 652 |
| GND | - | P103 | GND* | GND* | - |
| DONE | 3 | P104 | R14 | Y19 | 655 |
| $V_{CCO}$ | 4 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{PROGRAM}$ | - | P106 | P15 | W20 | 658 |
| I/O ($\overline{INIT}$) | 3 | P107 | N15 | V19 | 659 |
| I/O (D7) | 3 | P108 | N14 | Y21 | 662 |
| I/O | 3 | - | - | V20 | 665 |
| I/O | 3 | - | - | AA22 | 668 |
| I/O | 3 | - | T15 | W21 | 671 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P109 | M13 | U20 | 674 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 3 | - | - | U19 | 677 |
| I/O | 3 | - | - | V21 | 680 |
| I/O | 3 | - | R16 | T18 | 683 |
| I/O | 3 | P110 | M14 | W22 | 686 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P111 | L14 | U21 | 689 |
| I/O | 3 | P112 | M15 | T20 | 692 |
| I/O | 3 | - | - | T19 | 695 |
| I/O | 3 | - | - | V22 | 698 |
| I/O | 3 | - | L12 | T21 | 701 |
| I/O | 3 | P113 | P16 | R18 | 704 |
| I/O | 3 | - | - | U22 | 707 |
| I/O, $V_{REF}$ | 3 | P114 | L13 | R19 | 710 |
| I/O (D6) | 3 | P115 | N16 | T22 | 713 |
| GND | - | P116 | GND* | GND* | - |
| $V_{CCO}$ | 3 | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P119 | M16 | R21 | 716 |
| I/O | 3 | P120 | K14 | P18 | 719 |
| I/O | 3 | - | - | P19 | 725 |
| I/O | 3 | - | L16 | P20 | 728 |
| I/O | 3 | P121 | K13 | P21 | 731 |
| I/O | 3 | - | - | N19 | 734 |
| I/O | 3 | P122 | L15 | N18 | 740 |
| I/O | 3 | P123 | K12 | N20 | 743 |
| GND | - | P124 | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P125 | K16 | N21 | 746 |
| I/O (D4) | 3 | P126 | J16 | N22 | 749 |
| I/O | 3 | - | J14 | M19 | 752 |
| I/O | 3 | P127 | K15 | M20 | 755 |
| I/O | 3 | - | - | M18 | 758 |
| $V_{CCINT}$ | - | P128 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P129 | J15 | M22 | 764 |
| $V_{CCO}$ | 3 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P131 | GND* | GND* | - |