# E·XFL

#### AMD Xilinx - XC2S15-5TQG144C Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	96
Number of Logic Elements/Cells	432
Total RAM Bits	16384
Number of I/O	86
Number of Gates	15000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s15-5tqg144c

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# **Spartan-II Product Availability**

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination. The four global clock pins are usable as additional user I/Os when not used as a global clock pin. These pins are not included in user I/O counts.

#### Table 2: Spartan-II FPGA User I/O Chart(1)

		Available User I/O According to Package Type					
Device	Maximum User I/O	VQ100 VQG100	TQ144 TQG144	CS144 CSG144	PQ208 PQG208	FG256 FGG256	FG456 FGG456
XC2S15	86	60	86	(Note 2)	-	-	-
XC2S30	92	60	92	92	(Note 2)	-	-
XC2S50	176	-	92	-	140	176	-
XC2S100	176	-	92	-	140	176	(Note 2)
XC2S150	260	-	-	-	140	176	260
XC2S200	284	-	-	-	140	176	284

#### Notes:

1. All user I/O counts do not include the four global clock/user input pins.

2. Discontinued by PDN2004-01.

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DS001-2 (v2.8) June 13, 2008

# **Architectural Description**

# Spartan-II FPGA Array

The Spartan<sup>®</sup>-II field-programmable gate array, shown in Figure 2, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 2, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and

# Spartan-II FPGA Family: Functional Description

#### **Product Specification**

memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

# **Input/Output Block**

The Spartan-II FPGA IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. Table 3 lists several of the standards which are supported along with the required reference, output and termination voltages needed to meet the standard.



Figure 2: Spartan-II FPGA Input/Output Block (IOB)

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Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

#### Arithmetic Logic

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-II FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

### **BUFT**s

Each Spartan-II FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing," page 12. Each Spartan-II FPGA BUFT has an independent 3-state control pin and an independent input pin.

# **Block RAM**

Spartan-II FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks.

Table 5: Spartan-II Block RAM Amounts

Spartan-II Device	# of Blocks	Total Block RAM Bits
XC2S15	4	16K
XC2S30	6	24K
XC2S50	8	32K
XC2S100	10	40K
XC2S150	12	48K
XC2S200	14	56K

Each block RAM cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.



Figure 5: Dual-Port Block RAM

Table 6 shows the depth and width aspect ratios for the block RAM.

Table	6 <sup>.</sup>	Block	RAM	Port	Aspect	Ratios
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Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-II FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

# **Programmable Routing Matrix**

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times. Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 7 lists the boundary-scan instructions supported in Spartan-II FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Boundary-Scan Command	Binary Code[4:0]	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE	00001	Enables boundary-scan SAMPLE operation
USR1	00010	Access user-defined register 1
USR2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration
INTEST	00111	Enables boundary-scan INTEST operation
USRCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx <sup>®</sup> reserved instructions

# Table 7: Boundary-Scan Instructions

The public boundary-scan instructions are available prior to configuration. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

# 

# Signals

There are two kinds of pins that are used to configure Spartan-II devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the PROGRAM pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V<sub>CCO</sub> of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The  $\overline{\text{CS}}$  and  $\overline{\text{WRITE}}$  pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see "Pinout Tables" in Module 4 and XAPP176, Spartan-II FPGA Series Configuration and Readback.

# The Process

The sequence of steps necessary to configure Spartan-II devices are shown in Figure 11. The overall flow can be divided into three different phases.

- Initiating Configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

# Initiating Configuration

There are two different ways to initiate the configuration process: applying power to the device or asserting the PROGRAM input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Figure 12, page 19. Before configuration can begin,  $V_{CCO}$  Bank 2 must be greater than 1.0V. Furthermore, all  $V_{CCINT}$  power pins must be connected to a 2.5V supply. For more information on delaying configuration, see "Clearing Configuration Memory," page 19.

Once in user operation, the device can be re-configured simply by pulling the PROGRAM pin Low. The device acknowledges the beginning of the configuration process

by driving DONE Low, then enters the memory-clearing phase.



Figure 11: Configuration Flow Diagram

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The default timing for start-up is shown in the top half of Figure 13. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx software. Heavy lines show default settings.



Figure 13: Start-Up Waveforms

The bottom half of Figure 13 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

### **Serial Modes**

There are two serial configuration modes: In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 14 for the sequence for loading data into the Spartan-II FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 11. Note that CS and WRITE normally are not used during serial configuration. To ensure successful loading of the FPGA, do not toggle WRITE with CS Low during serial configuration.







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Symbol		Description		Units
T <sub>DCC</sub>		DIN setup	5	ns, min
T <sub>CCD</sub>		DIN hold	0	ns, min
т <sub>ссо</sub>		DOUT	12	ns, max
т <sub>ссн</sub>	COLK	High time	5	ns, min
T <sub>CCL</sub>		Low time	5	ns, min
F <sub>CC</sub>		Maximum frequency	66	MHz, max

Figure 16: Slave Serial Mode Timing

# **Design Considerations**

This section contains more detailed design information on the following features:

- Delay-Locked Loop . . . see page 27
- Block RAM . . . see page 32
- Versatile I/O . . . see page 36

# Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

# Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

### **Library DLL Primitives**

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.



Figure 22: Simplified DLL Macro BUFGDLL



DS001\_23\_032300





DS001\_24\_032300



At the third rising edge of CLKA, the  $T_{BCCS}$  parameter is violated with two writes to memory location 0x0F. The DOA and DOB busses reflect the contents of the DIA and DIB busses, but the stored value at 0x7E is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the  $T_{BCCS}$  parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

# Initialization

The block RAM memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 14. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

# **Initialization in VHDL**

The block RAM structures may be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization.

# **Initialization in Verilog**

The block RAM structures may be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization.

# **Block Memory Generation**

The CORE Generator<sup>™</sup> software generates memory structures using the block RAM features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

|--|

Property	Memory Cells
INIT_00	255 to 0
INIT_01	511 to 256
INIT_02	767 to 512
INIT_03	1023 to 768
INIT_04	1279 to 1024

	Table	14:	RAM	Initialization	Pro	perties
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Property	Memory Cells
INIT_05	1535 to 1280
INIT_06	1791 to 1536
INIT_07	2047 to 1792
INIT_08	2303 to 2048
INIT_09	2559 to 2304
INIT_0a	2815 to 2560
INIT_0b	3071 to 2816
INIT_0c	3327 to 3072
INIT_0d	3583 to 3328
INIT_0e	3839 to 3584
INIT_0f	4095 to 3840

For design examples and more information on using the Block RAM, see <u>XAPP173</u>, Using Block SelectRAM+ Memory in Spartan-II FPGAs.

# **Using Versatile I/O**

The Spartan-II FPGA family includes a highly configurable, high-performance I/O resource called Versatile I/O to provide support for a wide variety of I/O standards. The Versatile I/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and Versatile I/O features and the design considerations described in this document can improve and simplify system level design.

# Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high-performance I/O becomes more important. While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. Versatile I/O, the revolutionary input/output resources of Spartan-II devices, has resolved this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. The Spartan-II FPGA Versatile I/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each Versatile I/O block can support up to 16 I/O standards. Supporting such a variety of I/O standards allows the

support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage ( $V_{REF}$ ) and output source voltage ( $V_{CCO}$ ), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features, system-level design and board design can be greatly simplified and improved.

# **Fundamentals**

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 15, each buffer type can support a variety of voltage requirements.

# Table 15: Versatile I/O Supported Standards (Typical Values)

I/O Standard	Input Reference Voltage (V <sub>REF</sub> )	Output Source Voltage (V <sub>CCO</sub> )	Board Termination Voltage (V <sub>TT</sub> )
LVTTL (2-24 mA)	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	1.5
HSTL Class IV	0.9	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
СТТ	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

# **Overview of Supported I/O Standards**

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance JEDEC website at <a href="http://www.jedec.org">http://www.jedec.org</a>. For more details on the I/O standards and termination application examples, see <a href="http://www.seetandards">XAPP179</a>, "Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs."

# LVTTL — Low-Voltage TTL

The Low-Voltage TTL (LVTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage ( $V_{CCO}$ ), but does not require the use of a reference voltage ( $V_{REF}$ ) or a termination voltage ( $V_{TT}$ ).

# LVCMOS2 — Low-Voltage CMOS for 2.5V

The Low-Voltage CMOS for 2.5V or lower (LVCMOS2) standard is an extension of the LVCMOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage ( $V_{CCO}$ ), but does not require the use of a reference voltage ( $V_{REF}$ ) or a board termination voltage ( $V_{TT}$ ).

ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 18 provides the guidelines for the maximum numberof simultaneously switching outputs allowed per outputpower/ground pair to avoid the effects of ground bounce.Refer to Table 19 for the number of effective outputpower/ground pairs for each Spartan-II device and packagecombination.

# Table 18: Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair

	Package		
Standard	CS, FG	PQ, TQ, VQ	
LVTTL Slow Slew Rate, 2 mA drive	68	36	
LVTTL Slow Slew Rate, 4 mA drive	41	20	
LVTTL Slow Slew Rate, 6 mA drive	29	15	
LVTTL Slow Slew Rate, 8 mA drive	22	12	
LVTTL Slow Slew Rate, 12 mA drive	17	9	
LVTTL Slow Slew Rate, 16 mA drive	14	7	
LVTTL Slow Slew Rate, 24 mA drive	9	5	
LVTTL Fast Slew Rate, 2 mA drive	40	21	
LVTTL Fast Slew Rate, 4 mA drive	24	12	
LVTTL Fast Slew Rate, 6 mA drive	17	9	
LVTTL Fast Slew Rate, 8 mA drive	13	7	
LVTTL Fast Slew Rate, 12 mA drive	10	5	
LVTTL Fast Slew Rate, 16 mA drive	8	4	
LVTTL Fast Slew Rate, 24 mA drive	5	3	
LVCMOS2	10	5	
PCI	8	4	
GTL	4	4	
GTL+	4	4	
HSTL Class I	18	9	
HSTL Class III	9	5	
HSTL Class IV	5	3	
SSTL2 Class I	15	8	

# Table 18: Maximum Number of SimultaneouslySwitching Outputs per Power/Ground Pair

	Package		
Standard	CS, FG	PQ, TQ, VQ	
SSTL2 Class II	10	5	
SSTL3 Class I	11	6	
SSTL3 Class II	7	4	
СТТ	14	7	
AGP	9	5	

Notes:

1. This analysis assumes a 35 pF load for each output.

# Table 19: Effective Output Power/Ground Pairs for Spartan-II Devices

	Spartan-II Devices						
Pkg.	XC2S 15	XC2S 30	XC2S 50	XC2S 100	XC2S 150	XC2S 200	
VQ100	8	8	-	-	-	-	
CS144	12	12	-	-	-	-	
TQ144	12	12	12	12	-	-	
PQ208	-	16	16	16	16	16	
FG256	-	-	16	16	16	16	
FG456	-	-	-	48	48	48	

# **Termination Examples**

Creating a design with the Versatile I/O features requires the instantiation of the desired library primitive within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the Versatile I/O features. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

### SSTL2\_I

A sample circuit illustrating a valid termination technique for SSTL2\_I appears in Figure 49. DC voltage specifications appear in Table 27 for the SSTL2\_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

#### SSTL2 Class I



Figure 49: Terminated SSTL2 Class I

Table	27:	SSTL2_	Voltage	Specifications
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Parameter	Min	Тур	Max
V <sub>CCO</sub>	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \ge V_{REF} + 0.18$	1.33	1.43	3.0 <sup>(2)</sup>
$V_{IL} \leq V_{REF} - 0.18$	-0.3 <sup>(3)</sup>	1.07	1.17
V <sub>OH</sub> ≥ V <sub>REF</sub> + 0.61	1.76	-	-
$V_{OL} \le V_{REF} - 0.61$	-	-	0.74
I <sub>OH</sub> at V <sub>OH</sub> (mA)	-7.6	-	-
I <sub>OL</sub> at V <sub>OL</sub> (mA)	7.6	-	-

#### Notes:

- 1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
- 2.  $V_{IH}$  maximum is  $V_{CCO}$  + 0.3.
- 3. V<sub>IL</sub> minimum does not conform to the formula.

#### SSTL2 Class II

A sample circuit illustrating a valid termination technique for SSTL2\_II appears in Figure 50. DC voltage specifications appear in Table 28 for the SSTL2\_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.



Figure 50: Terminated SSTL2 Class II

#### Table 28: SSTL2\_II Voltage Specifications

Parameter	Min	Тур	Max
V <sub>CCO</sub>	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \ge V_{REF} + 0.18$	1.33	1.43	3.0 <sup>(2)</sup>
$V_{IL} \leq V_{REF} - 0.18$	-0.3 <sup>(3)</sup>	1.07	1.17
$V_{OH} \ge V_{REF} + 0.8$	1.95	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.55
I <sub>OH</sub> at V <sub>OH</sub> (mA)	-15.2	-	-
I <sub>OL</sub> at V <sub>OL</sub> (mA)	15.2	-	-

#### Notes:

- 1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
- 2.  $V_{IH}$  maximum is  $V_{CCO}$  + 0.3.
- 3. V<sub>IL</sub> minimum does not conform to the formula.

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# LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 32 for the LVTTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

#### Table 32: LVTTL Voltage Specifications

Parameter	Min	Тур	Max
V <sub>CCO</sub>	3.0	3.3	3.6
V <sub>REF</sub>	-	-	-
V <sub>TT</sub>	-	-	-
V <sub>IH</sub>	2.0	-	5.5
V <sub>IL</sub>	-0.5	-	0.8
V <sub>OH</sub>	2.4	-	-
V <sub>OL</sub>	-	-	0.4
I <sub>OH</sub> at V <sub>OH</sub> (mA)	-24	-	-
I <sub>OL</sub> at V <sub>OL</sub> (mA)	24	-	-

#### Notes:

1.  $V_{OL}$  and  $V_{OH}$  for lower drive currents sample tested.

#### LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 33 for the LVCMOS2 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

#### Table 33: LVCMOS2 Voltage Specifications

Parameter	Min	Тур	Max
V <sub>CCO</sub>	2.3	2.5	2.7
V <sub>REF</sub>	-	-	-
V <sub>TT</sub>	-	-	-
V <sub>IH</sub>	1.7	-	5.5
V <sub>IL</sub>	-0.5	-	0.7
V <sub>OH</sub>	1.9	-	-
V <sub>OL</sub>	-	-	0.4
I <sub>OH</sub> at V <sub>OH</sub> (mA)	-12	-	-
I <sub>OL</sub> at V <sub>OL</sub> (mA)	12	-	-

#### AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 34 for the AGP-2X standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

#### Table 34: AGP-2X Voltage Specifications

Parameter	Min	Тур	Max
V <sub>CCO</sub>	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}^{(1)}$	1.17	1.32	1.48
V <sub>TT</sub>	-	-	-
$V_{IH} \ge V_{REF} + 0.2$	1.37	1.52	-
$V_{IL} \leq V_{REF} - 0.2$	-	1.12	1.28
$V_{OH} \ge 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} \le 0.1 \times V_{CCO}$	-	0.33	0.36
I <sub>OH</sub> at V <sub>OH</sub> (mA)	Note 2	-	-
I <sub>OL</sub> at V <sub>OL</sub> (mA)	Note 2	-	-

#### Notes:

- 1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
- 2. Tested according to the relevant specification.

For design examples and more information on using the I/O, see <u>XAPP179</u>, Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs.



# Spartan-II FPGA Family: DC and Switching Characteristics

DS001-3 (v2.8) June 13, 2008

**Product Specification** 

# **Definition of Terms**

In this document, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All limits are representative of worst-case supply voltage and junction temperature conditions. Typical numbers are based on measurements taken at a nominal  $V_{CCINT}$  level of 2.5V and a junction temperature of 25°C. The parameters included are common to popular designs and typical applications. All specifications are subject to change without notice.

# **DC Specifications**

### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Description		Min	Max	Units
V <sub>CCINT</sub>	Supply voltage relative to GND <sup>(2)</sup>		-0.5	3.0	V
V <sub>CCO</sub>	Supply voltage relative to GND <sup>(2)</sup>		-0.5	4.0	V
V <sub>REF</sub>	Input reference voltage		-0.5	3.6	V
V <sub>IN</sub>	Input voltage relative to GND <sup>(3)</sup>	5V tolerant I/O <sup>(4)</sup>	-0.5	5.5	V
		No 5V tolerance <sup>(5)</sup>	-0.5	V <sub>CCO</sub> +0.5	V
V <sub>TS</sub>	Voltage applied to 3-state output	blied to 3-state output 5V tolerant I/O <sup>(4)</sup>		5.5	V
		No 5V tolerance <sup>(5)</sup>	-0.5	V <sub>CCO</sub> +0.5	V
T <sub>STG</sub>	Storage temperature (ambient)		-65	+150	°C
TJ	Junction temperature		-	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

2. Power supplies may turn on in any order.

3. V<sub>IN</sub> should not exceed V<sub>CCO</sub> by more than 3.6V over extended periods of time (e.g., longer than a day).

4. Spartan<sup>®</sup>-II device I/Os are 5V Tolerant whenever the LVTTL, LVCMOS2, or PCI33\_5 signal standard has been selected. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA, and undershoot must be limited to either -0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to -2.0V or overshoot to +7.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

5. Without 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either V<sub>CCO</sub> + 0.5V or 10 mA, and undershoot must be limited to -0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to -2.0V or overshoot to V<sub>CCO</sub> + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

6. For soldering guidelines, see the <u>Packaging Information</u> on the Xilinx<sup>®</sup> web site.

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# **IOB Output Switching Characteristics**

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59.

		Speed Grade				
		-6		-5		
Symbol	Description	Min	Max	Min	Max	Units
Propagation Delays	5					
T <sub>IOOP</sub>	O input to pad	-	2.9	-	3.4	ns
T <sub>IOOLP</sub>	O input to pad via transparent latch	-	3.4	-	4.0	ns
3-state Delays		1				
T <sub>IOTHZ</sub>	T input to pad high-impedance <sup>(1)</sup>	-	2.0	-	2.3	ns
T <sub>IOTON</sub>	T input to valid data on pad	-	3.0	-	3.6	ns
T <sub>IOTLPHZ</sub>	T input to pad high impedance via transparent latch <sup>(1)</sup>	-	2.5	-	2.9	ns
T <sub>IOTLPON</sub>	T input to valid data on pad via transparent latch	-	3.5	-	4.2	ns
T <sub>GTS</sub>	GTS to pad high impedance <sup>(1)</sup>	-	5.0	-	5.9	ns
Sequential Delays		1	I	1		
T <sub>IOCKP</sub>	Clock CLK to pad	-	2.9	-	3.4	ns
Т <sub>ЮСКНZ</sub>	Clock CLK to pad high impedance (synchronous) <sup>(1)</sup>	-	2.3	-	2.7	ns
T <sub>IOCKON</sub>	Clock CLK to valid data on pad (synchronous)	-	3.3	-	4.0	ns
Setup/Hold Times	with Respect to Clock CLK <sup>(2)</sup>	1	l.			
TIOOCK / TIOCKO	O input	1.1/0	-	1.3/0	-	ns
T <sub>IOOCECK</sub> /	OCE input	0.9 / 0.01	-	0.9/0.01	-	ns
TIOCKOCE						
T <sub>IOSRCKO</sub> /	SR input (OFF)	1.2/0	-	1.3 / 0	-	ns
TIOCKOSR				/ -		
TIOTCK / TIOCKT	3-state setup times, T input	0.8/0	-	0.9/0	-	ns
Т <sub>ІОТСЕСК</sub> /	3-state setup times, TCE input	1.0/0	-	1.0/0	-	ns
		11/0		10/0		
	3-state setup times, SK input (TFF)	1.170	-	1.2/0	-	ns
Set/Reset Delays						
	SR input to pad (asynchronous)	_	37	_	44	ns
	SR input to pad high impedance (asynchronous) <sup>(1)</sup>	-	3.1	-	37	ns
	SR input to valid data on pad (asynchronous)	-	4 1	-	4 Q	ns
	GSR to pad	_	9.1	_	11 7	ns
' IOGSRQ	OUN ID Pau	-	9.9	-	11.7	115

Notes:

1. Three-state turn-off delays should not be adjusted.

2. A zero hold time listing indicates no hold time or a negative hold time.

# **CLB Arithmetic Switching Characteristics**

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

		Speed Grade				
		-	6		5	-
Symbol	Description	Min	Мах	Min	Мах	Units
Combinatorial Dela	ays					
T <sub>OPX</sub>	F operand inputs to X via XOR	-	0.8	-	0.9	ns
T <sub>OPXB</sub>	F operand input to XB output	-	1.3	-	1.5	ns
T <sub>OPY</sub>	F operand input to Y via XOR	-	1.7	-	2.0	ns
Т <sub>ОРҮВ</sub>	F operand input to YB output	-	1.7	-	2.0	ns
T <sub>OPCYF</sub>	F operand input to COUT output	-	1.3	-	1.5	ns
T <sub>OPGY</sub>	G operand inputs to Y via XOR	-	0.9	-	1.1	ns
T <sub>OPGYB</sub>	G operand input to YB output	-	1.6	-	2.0	ns
T <sub>OPCYG</sub>	G operand input to COUT output	-	1.2	-	1.4	ns
T <sub>BXCY</sub>	BX initialization input to COUT	-	0.9	-	1.0	ns
T <sub>CINX</sub>	CIN input to X output via XOR	-	0.4	-	0.5	ns
T <sub>CINXB</sub>	CIN input to XB	-	0.1	-	0.1	ns
T <sub>CINY</sub>	CIN input to Y via XOR	-	0.5	-	0.6	ns
T <sub>CINYB</sub>	CIN input to YB	-	0.6	-	0.7	ns
T <sub>BYP</sub>	CIN input to COUT output	-	0.1	-	0.1	ns
Multiplier Operatio	n					
T <sub>FANDXB</sub>	F1/2 operand inputs to XB output via AND	-	0.5	-	0.5	ns
T <sub>FANDYB</sub>	F1/2 operand inputs to YB output via AND	-	0.9	-	1.1	ns
T <sub>FANDCY</sub>	F1/2 operand inputs to COUT output via AND	-	0.5	-	0.6	ns
T <sub>GANDYB</sub>	G1/2 operand inputs to YB output via AND	-	0.6	-	0.7	ns
T <sub>GANDCY</sub>	G1/2 operand inputs to COUT output via AND	-	0.2	-	0.2	ns
Setup/Hold Times	with Respect to Clock CLK <sup>(1)</sup>					
Т <sub>ССКХ</sub> / Т <sub>СКСХ</sub>	CIN input to FFX	1.1/0	-	1.2/0	-	ns
T <sub>CCKY</sub> / T <sub>CKCY</sub>	CIN input to FFY	1.2 / 0	-	1.3/0	-	ns

Notes:

1. A zero hold time listing indicates no hold time or a negative hold time.

Package	Leads	Туре	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass <sup>(1)</sup> (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	60	0.5	16 x 16	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	92	0.5	22 x 22	1.60	1.4
CS144 / CSG144	144	Chip Scale Ball Grid Array (CSBGA)	92	0.8	12 x 12	1.20	0.3
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	140	0.5	30.6 x 30.6	3.70	5.3
FG256 / FGG256	256	Fine-pitch Ball Grid Array (FBGA)	176	1.0	17 x 17	2.00	0.9
FG456 / FGG456	456	Fine-pitch Ball Grid Array (FBGA)	284	1.0	23 x 23	2.60	2.2

#### Table 36: Spartan-II Family Package Options

#### Notes:

1. Package mass is  $\pm 10\%$ .

Note: Some early versions of Spartan-II devices, including the XC2S15 and XC2S30 ES devices and the XC2S150 with date code 0045 or earlier, included a power-down pin. For more information, see <u>Answer Record 10500</u>.

# VCCO Banks

Some of the I/O standards require specific V<sub>CCO</sub> voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3 in Module 2). Each bank has multiple V<sub>CCO</sub> pins which must be connected to the same voltage. In the smaller packages, the V<sub>CCO</sub> pins are connected between banks, effectively reducing the number of independent banks available (see Table 37). These interconnected banks are shown in the Pinout Tables with V<sub>CCO</sub> pads for multiple banks connected to the same pin.

#### Table 37: Independent VCCO Banks Available

Package	VQ100	CS144	FG256
	PQ208	TQ144	FG456
Independent Banks	1	4	8

# Package Overview

Table 36 shows the six low-cost, space-saving productionpackage styles for the Spartan-II family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS144" package becomes "CSG144" when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 38. For additional package information, see <u>UG112</u>: *Device Package User Guide*.

# **Mechanical Drawings**

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 38.

Material Declaration Data Sheets (MDDS) are also available on the <u>Xilinx web site</u> for each package.

#### Table 38: Xilinx Package Documentation

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
CS144	Package Drawing	PK149_CS144
CSG144		PK103_CSG144
PQ208	Package Drawing	PK166_PQ208
PQG208		PK123_PQG208
FG256	Package Drawing	PK151_FG256
FGG256		PK105_FGG256
FG456	Package Drawing	PK154_FG456
FGG456		PK109_FGG456

# XC2S15 Device Pinouts (Continued)

XC2S15 Pad Name					Bndry
Function	Bank	VQ100	TQ144	CS144	Scan
GND	-	-	P61	J12	-
I/O (D5)	3	P57	P60	J13	245
I/O	3	P58	P59	H10	248
I/O, V <sub>REF</sub>	3	P59	P58	H11	251
I/O (D4)	3	P60	P57	H12	254
I/O	3	-	P56	H13	257
V <sub>CCINT</sub>	-	P61	P55	G12	-
I/O, TRDY <sup>(1)</sup>	3	P62	P54	G13	260
V <sub>CCO</sub>	3	P63	P53	G11	-
V <sub>CCO</sub>	2	P63	P53	G11	-
GND	-	P64	P52	G10	-
I/O, IRDY <sup>(1)</sup>	2	P65	P51	F13	263
I/O	2	-	P50	F12	266
I/O (D3)	2	P66	P49	F11	269
I/O, V <sub>REF</sub>	2	P67	P48	F10	272
I/O	2	P68	P47	E13	275
I/O (D2)	2	P69	P46	E12	278
GND	-	-	P45	E11	-
I/O (D1)	2	P70	P44	E10	281
I/O	2	P71	P43	D13	284
I/O, V <sub>REE</sub>	2	P72	P41	D11	287
I/O	2	-	P40	C13	290
I/O (DIN, D0)	2	P73	P39	C12	293
I/O (DOUT, BUSY)	2	P74	P38	C11	296
CCLK	2	P75	P37	B13	299
V <sub>CCO</sub>	2	P76	P36	B12	-
V <sub>CCO</sub>	1	P76	P35	A13	-
TDO	2	P77	P34	A12	-
GND	-	P78	P33	B11	-
TDI	-	P79	P32	A11	-
I/O (CS)	1	P80	P31	D10	0
I/O (WRITE)	1	P81	P30	C10	3
I/O	1	-	P29	B10	6
I/O, V <sub>REF</sub>	1	P82	P28	A10	9
I/O	1	P83	P27	D9	12
I/O	1	P84	P26	C9	15
GND	-	-	P25	B9	-
V <sub>CCINT</sub>	-	P85	P24	A9	-
I/O	1	-	P23	D8	18
I/O	1	-	P22	C8	21

# XC2S15 Device Pinouts (Continued)

XC2S15 Pad Name					Bndry
Function	Bank	VQ100	TQ144	CS144	Scan
I/O, V <sub>REF</sub>	1	P86	P21	B8	24
I/O	1	-	P20	A8	27
I/O	1	P87	P19	B7	30
I, GCK2	1	P88	P18	A7	36
GND	-	P89	P17	C7	-
V <sub>CCO</sub>	1	P90	P16	D7	-
V <sub>CCO</sub>	0	P90	P16	D7	-
I, GCK3	0	P91	P15	A6	37
V <sub>CCINT</sub>	-	P92	P14	B6	-
I/O	0	-	P13	C6	44
I/O, V <sub>REF</sub>	0	P93	P12	D6	47
I/O	0	-	P11	A5	50
I/O	0	-	P10	B5	53
V <sub>CCINT</sub>	-	P94	P9	C5	-
GND	-	-	P8	D5	-
I/O	0	P95	P7	A4	56
I/O	0	P96	P6	B4	59
I/O, V <sub>REF</sub>	0	P97	P5	C4	62
I/O	0	-	P4	A3	65
I/O	0	P98	P3	B3	68
ТСК	-	P99	P2	C3	-
V <sub>CCO</sub>	0	P100	P1	A2	-
V <sub>CCO</sub>	7	P100	P144	B2	-

#### 04/18/01

#### Notes:

- 1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
- 2. See "VCCO Banks" for details on  $V_{CCO}$  banking.

# Additional XC2S15 Package Pins

#### VQ100

		Not Conne	ected Pins			
P28	P29	-	-	-	-	
11/02/00						

#### TQ144

Not Connected Pins									
P42	P64	P78	P101	P104	P105				
P116	P138	-	-	-	-				
11/02/00		•							

CS144

00144									
Not Connected Pins									
D3	D12	J4	K13	M3	M4				
M10	N3	-	-	-	-				
11/02/00									

# XC2S100 Device Pinouts (Continued)

XC2S100 Name	Pad					Bndry
Function	Bank	TQ144	PQ208	FG256	FG456	Scan
V <sub>CCINT</sub>	-	-	P38	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	6	-	P39	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	P119	P40	GND*	GND*	-
I/O	6	P118	P41	K4	T1	314
I/O, V <sub>REF</sub>	6	P117	P42	M1	R4	317
I/O	6	-	-	-	T2	320
I/O	6	P116	P43	L4	U1	323
I/O	6	-	-	M2	R5	326
I/O	6	-	P44	L3	U2	332
I/O, V <sub>REF</sub>	6	P115	P45	N1	Т3	335
V <sub>CCO</sub>	6	-	-	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	-	-	GND*	GND*	-
I/O	6	-	P46	P1	T4	338
I/O	6	-	-	L5	W1	341
I/O	6	-	-	-	U4	344
I/O	6	P114	P47	N2	Y1	347
I/O	6	-	-	M4	W2	350
I/O	6	P113	P48	R1	Y2	356
I/O	6	P112	P49	M3	W3	359
M1	-	P111	P50	P2	U5	362
GND	-	P110	P51	GND*	GND*	-
MO	-	P109	P52	N3	AB2	363
V <sub>CCO</sub>	6	P108	P53	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
V <sub>CCO</sub>	5	P107	P53	V <sub>CCO</sub> Bank 5*	V <sub>CCO</sub> Bank 5*	-
M2	-	P106	P54	R3	Y4	364
I/O	5	-	-	N5	V7	374
I/O	5	P103	P57	T2	Y6	377
I/O	5	-	-	-	AA4	380
I/O	5	-	-	P5	W6	383
I/O	5	-	P58	Т3	Y7	386
GND	-	-	-	GND*	GND*	-
V <sub>CCO</sub>	5	-	-	V <sub>CCO</sub> Bank 5*	V <sub>CCO</sub> Bank 5*	-
I/O, V <sub>REF</sub>	5	P102	P59	T4	AA5	389
I/O	5	-	P60	M6	AB5	392
I/O	5	-	-	T5	AB6	398
I/O	5	P101	P61	N6	AA7	401
I/O	5	-	-	-	W7	404

# XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						Des ales a
Function	Bank	TQ144	PQ208	FG256	FG456	Scan
I/O, V <sub>REF</sub>	5	P100	P62	R5	W8	407
I/O	5	P99	P63	P6	Y8	410
GND	-	P98	P64	GND*	GND*	-
V <sub>CCO</sub>	5	-	P65	V <sub>CCO</sub> Bank 5*	V <sub>CCO</sub> Bank 5*	-
V <sub>CCINT</sub>	-	P97	P66	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	5	P96	P67	R6	AA8	413
I/O	5	P95	P68	M7	V9	416
I/O	5	-	-	-	AB9	419
I/O	5	-	P69	N7	Y9	422
I/O	5	-	P70	T6	W10	428
I/O	5	-	P71	P7	AB10	431
GND	-	-	P72	GND*	GND*	-
I/O, V <sub>REF</sub>	5	P94	P73	P8	Y10	434
I/O	5	-	P74	R7	V11	437
I/O	5	-	-	T7	W11	440
I/O	5	P93	P75	Т8	AB11	443
V <sub>CCINT</sub>	-	P92	P76	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I, GCK1	5	P91	P77	R8	Y11	455
V <sub>CCO</sub>	5	P90	P78	V <sub>CCO</sub> Bank 5*	V <sub>CCO</sub> Bank 5*	-
V <sub>CCO</sub>	4	P90	P78	V <sub>CCO</sub> Bank 4*	V <sub>CCO</sub> Bank 4*	-
GND	-	P89	P79	GND*	GND*	-
I, GCK0	4	P88	P80	N8	W12	456
I/O	4	P87	P81	N9	U12	460
I/O	4	P86	P82	R9	Y12	466
I/O	4	-	-	N10	AA12	469
I/O	4	-	P83	Т9	AB13	472
I/O, V <sub>REF</sub>	4	P85	P84	P9	AA13	475
GND	-	-	P85	GND*	GND*	-
I/O	4	-	P86	M10	Y13	478
I/O	4	-	P87	R10	V13	481
I/O	4	-	P88	P10	AA14	487
I/O	4	-	-	-	V14	490
I/O	4	P84	P89	T10	AB15	493
I/O	4	P83	P90	R11	AA15	496
V <sub>CCINT</sub>	-	P82	P91	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	4	-	P92	V <sub>CCO</sub> Bank 4*	V <sub>CCO</sub> Bank 4*	-
GND	-	P81	P93	GND*	GND*	-
I/O	4	P80	P94	M11	Y15	499

# XC2S200 Device Pinouts (Continued)

XC2S200 Pad	Name				Bndry
Function	Bank	PQ208	FG256	FG456	Scan
V <sub>CCO</sub>	1	P156	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
TDO	2	P157	B14	A21	-
GND	-	P158	GND*	GND*	-
TDI	-	P159	A15	B20	-
I/O ( <u>CS</u> )	1	P160	B13	C19	0
I/O (WRITE)	1	P161	C13	A20	3
I/O	1	-	-	B19	9
I/O	1	-	-	C18	12
I/O	1	-	C12	D17	15
GND	-	-	GND*	GND*	-
I/O, V <sub>REF</sub>	1	P162	A14	A19	18
I/O	1	-	-	B18	21
I/O	1	-	-	E16	27
I/O	1	-	D12	C17	30
I/O	1	P163	B12	D16	33
GND	-	-	GND*	GND*	-
V <sub>CCO</sub>	1	-	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
I/O, V <sub>REF</sub>	1	P164	C11	A18	36
I/O	1	P165	A13	B17	39
I/O	1	-	-	E15	42
I/O	1	-	-	A17	45
I/O	1	-	D11	D15	48
GND	-	-	GND*	GND*	-
I/O	1	P166	A12	C16	51
I/O	1	-	-	D14	54
I/O, V <sub>REF</sub>	1	P167	E11	E14	60
I/O	1	P168	B11	A16	63
GND	-	P169	GND*	GND*	-
V <sub>CCO</sub>	1	P170	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
V <sub>CCINT</sub>	-	P171	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	1	P172	A11	C15	66
I/O	1	P173	C10	B15	69
I/O	1	-	-	E13	72
I/O	1	-	-	A15	75
I/O	1	-	-	F12	78
GND	-	-	GND*	GND*	-
I/O	1	P174	B10	C14	81
I/O	1	-	-	B14	84
I/O	1	-	-	A14	87

# XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O	1	P175	D10	D13	90
I/O	1	P176	A10	C13	93
GND	-	P177	GND*	GND*	-
V <sub>CCO</sub>	1	-	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
I/O, V <sub>REF</sub>	1	P178	B9	B13	96
I/O	1	P179	E10	E12	99
I/O	1	-	-	A13	105
I/O	1	-	A9	B12	108
I/O	1	P180	D9	D12	111
I/O	1	-	-	C12	114
I/O	1	P181	A8	D11	120
I, GCK2	1	P182	C9	A11	126
GND	-	P183	GND*	GND*	-
V <sub>CCO</sub>	1	P184	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
V <sub>CCO</sub>	0	P184	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
I, GCK3	0	P185	B8	C11	127
V <sub>CCINT</sub>	-	P186	$V_{CCINT}^{*}$	$V_{CCINT}^{*}$	-
I/O	0	-	-	E11	137
I/O	0	P187	A7	A10	140
I/O	0	-	D8	B10	143
I/O	0	-	-	F11	146
I/O	0	P188	A6	C10	152
I/O, V <sub>REF</sub>	0	P189	B7	A9	155
V <sub>CCO</sub>	0	-	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
GND	-	P190	GND*	GND*	-
I/O	0	P191	C8	B9	158
I/O	0	P192	D7	E10	161
I/O	0	-	-	C9	164
I/O	0	-	-	D10	167
I/O	0	P193	E7	A8	170
GND	-	-	GND*	GND*	-
I/O	0	-	-	D9	173
I/O	0	-	-	B8	176
I/O	0	-	-	C8	179
I/O	0	P194	C7	E9	182
I/O	0	P195	B6	A7	185
V <sub>CCINT</sub>	-	P196	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	0	P197	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-