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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 96 |
| Number of Logic Elements/Cells | 432 |
| Total RAM Bits | 16384 |
| Number of I/O | 60 |
| Number of Gates | 15000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s15-5vq100c |

# Spartan-II FPGA Family: Introduction and Ordering Information

DS001-1 (v2.8) June 13, 2008

**Product Specification**

## Introduction

The Spartan®-II Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The six-member family offers densities ranging from 15,000 to 200,000 system gates, as shown in Table 1. System performance is supported up to 200 MHz. Features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards, and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-II family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

## Features

- Second generation ASIC replacement technology
  - Densities as high as 5,292 logic cells with up to 200,000 system gates
  - Streamlined features based on Virtex® FPGA architecture
  - Unlimited reprogrammability
  - Very low cost
  - Cost-effective 0.18 micron process
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K bit block RAM
    - Fast interfaces to external RAM
  - Fully PCI compliant
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 16 high-performance interface standards
  - Hot swap Compact PCI friendly
  - Zero hold time simplifies system timing
- Core logic powered at 2.5V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing

*Table 1:* **Spartan-II FPGA Family Members**

| Device | Logic Cells | System Gates (Logic and RAM) | CLB Array (R x C) | Total CLBs | Maximum Available User I/O(1) | Total Distributed RAM Bits | Total Block RAM Bits |
|---|---|---|---|---|---|---|---|
| XC2S15 | 432 | 15,000 | 8 x 12 | 96 | 86 | 6,144 | 16K |
| XC2S30 | 972 | 30,000 | 12 x 18 | 216 | 92 | 13,824 | 24K |
| XC2S50 | 1,728 | 50,000 | 16 x 24 | 384 | 176 | 24,576 | 32K |
| XC2S100 | 2,700 | 100,000 | 20 x 30 | 600 | 176 | 38,400 | 40K |
| XC2S150 | 3,888 | 150,000 | 24 x 36 | 864 | 260 | 55,296 | 48K |
| XC2S200 | 5,292 | 200,000 | 28 x 42 | 1,176 | 284 | 75,264 | 56K |

**Notes:**
1. All user I/O counts do not include the four global clock/user input pins. See details in Table 2, page 4.

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## Revision History

| Date | Version No. | Description |
|---|---|---|
| 09/18/00 | 2.0 | Sectioned the Spartan-II Family data sheet into four modules. Added industrial temperature range information. |
| 10/31/00 | 2.1 | Removed Power down feature. |
| 03/05/01 | 2.2 | Added statement on PROMs. |
| 11/01/01 | 2.3 | Updated Product Availability chart. Minor text edits. |
| 09/03/03 | 2.4 | Added device part marking. |
| 08/02/04 | 2.5 | Added information on Pb-free packaging options and removed discontinued options. |
| 06/13/08 | 2.8 | Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |

PN 011311

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The default timing for start-up is shown in the top half of Figure 13. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx software. Heavy lines show default settings.

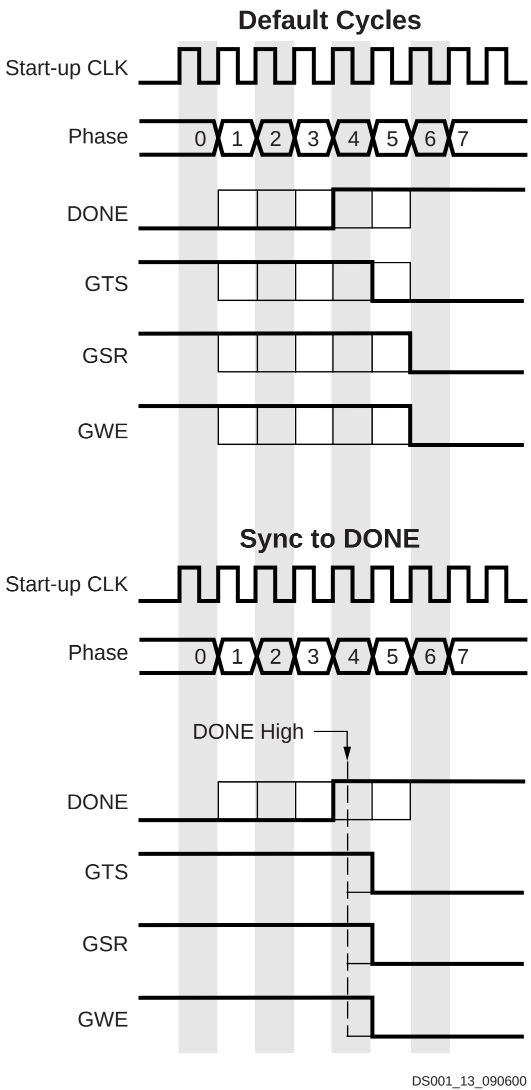


*Figure 13:* **Start-Up Waveforms**

The bottom half of Figure 13 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

## Serial Modes

There are two serial configuration modes: In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 14 for the sequence for loading data into the Spartan-II FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 11. Note that $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ normally are not used during serial configuration. To ensure successful loading of the FPGA, do not toggle $\overline{\text{WRITE}}$ with $\overline{\text{CS}}$ Low during serial configuration.

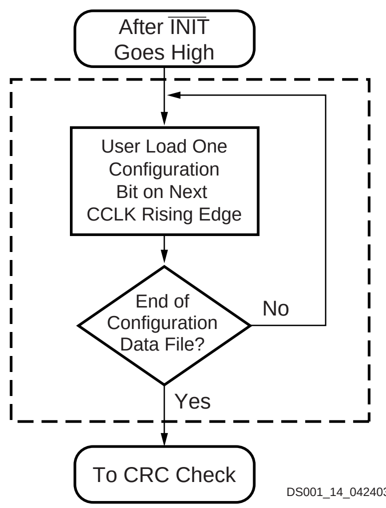


*Figure 14:* **Loading Serial Mode Configuration Data**

## Design Considerations

This section contains more detailed design information on the following features:

- Delay-Locked Loop . . . see page 27
- Block RAM . . . see page 32
- Versatile I/O . . . see page 36

## Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

### Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

### Library DLL Primitives

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.

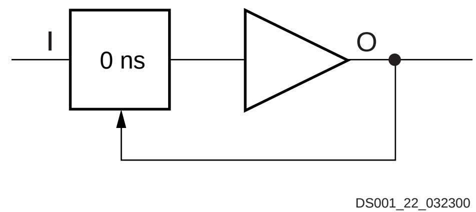


*Figure 22:* **Simplified DLL Macro BUFGDLL**

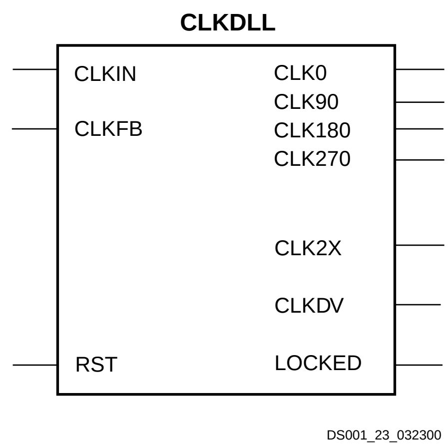


*Figure 23:* **Standard DLL Primitive CLKDLL**

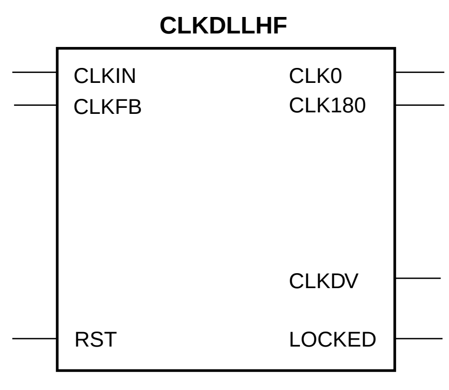


*Figure 24:* **High-Frequency DLL Primitive CLKDLLHF**

## BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 25.

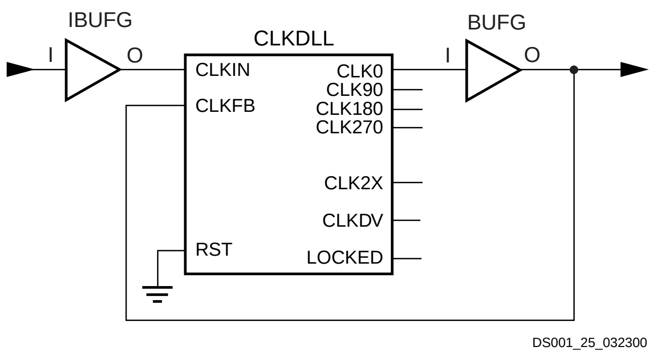


*Figure 25:* **BUFGDLL Block Diagram**

This macro does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This macro also does not provide access to the RST or LOCKED pins of the DLL. For access to these features, a designer must use the DLL primitives described in the following sections.

### *Source Clock Input — I*

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

### *Clock Output — O*

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG primitive, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50/50 duty cycle unless you deactivate the duty cycle correction property.

## CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

### *Source Clock Input — CLKIN*

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

### *Feedback Clock Input — CLKFB*

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. Either a global clock buffer (BUFG) or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feed back to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software to determine which DLL clock output sources the CLKFB pin.

### *Reset Input — RST*

When the reset pin RST activates, the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or be tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer deskew with respect to one another. The DLL must be reset when the input clock frequency changes, if the device is reconfigured in Boundary-Scan mode, if the device undergoes a hot swap, and after the device is configured if the input clock is not stable during the startup sequence.

### *2x Clock Output — CLK2X*

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

### *Clock Divide Output — CLKDV*

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction. The CLKDV output pin has a 50/50 duty cycle for all values of the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage ($V_{REF}$) and output source voltage ($V_{CCO}$), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features, system-level design and board design can be greatly simplified and improved.

## Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 15, each buffer type can support a variety of voltage requirements.

*Table 15:* **Versatile I/O Supported Standards (Typical Values)**

| I/O Standard | Input Reference Voltage ($V_{REF}$) | Output Source Voltage ($V_{CCO}$) | Board Termination Voltage ($V_{TT}$) |
|---|---|---|---|
| LVTTL (2-24 mA) | N/A | 3.3 | N/A |
| LVCMOS2 | N/A | 2.5 | N/A |
| PCI (3V/5V, 33 MHz/66 MHz) | N/A | 3.3 | N/A |
| GTL | 0.8 | N/A | 1.2 |
| GTL+ | 1.0 | N/A | 1.5 |
| HSTL Class I | 0.75 | 1.5 | 0.75 |
| HSTL Class III | 0.9 | 1.5 | 1.5 |
| HSTL Class IV | 0.9 | 1.5 | 1.5 |
| SSTL3 Class I and II | 1.5 | 3.3 | 1.5 |
| SSTL2 Class I and II | 1.25 | 2.5 | 1.25 |
| CTT | 1.5 | 3.3 | 1.5 |
| AGP-2X | 1.32 | 3.3 | N/A |

## Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance JEDEC website at http://www.jedec.org. For more details on the I/O standards and termination application examples, see XAPP179, "*Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs.*"

### *LVTTL — Low-Voltage TTL*

The Low-Voltage TTL (LVTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a termination voltage ($V_{TT}$).

### *LVCMOS2 — Low-Voltage CMOS for 2.5V*

The Low-Voltage CMOS for 2.5V or lower (LVCMOS2) standard is an extension of the LVCMOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$).

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF primitive names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24). The default is slew rate limited with 12 mA drive.

OBUF placement restrictions require that within a given $V_{CCO}$ bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within any $V_{CCO}$ bank. Table 17 summarizes the output compatibility requirements. The LOC property can specify a location for the OBUF.

*Table 17:* **Output Standards Compatibility Requirements**

| | |
|---|---|
| Rule 1 | Only outputs with standards which share compatible $V_{CCO}$ may be used within the same bank. |
| Rule 2 | There are no placement restrictions for outputs with standards that do not require a $V_{CCO}$. |
| $V_{CCO}$ | Compatible Standards |
| 3.3 | LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3 |
| 2.5 | SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+ |
| 1.5 | HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+ |

### *OBUFT*

The generic 3-state output buffer OBUFT, shown in Figure 39, typically implements 3-state outputs or bidirectional I/O.

With no extension or property specified for the generic OBUFT primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT primitive names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

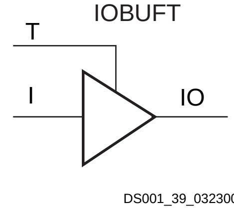


*Figure 39:* **3-State Output Buffer Primitive (OBUFT**

The Versatile I/O OBUFT placement restrictions require that within a given $V_{CCO}$ bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a $V_{REF}$ have automatic placement of a $V_{REF}$ in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding $V_{REF}$) are explicitly placed.

The LOC property can specify a location for the OBUFT.

### *IOBUF*

Use the IOBUF primitive for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 40.

With no extension or property specified for the generic IOBUF primitive, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF primitive names is as follows:

ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 18 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 19 for the number of effective output power/ground pairs for each Spartan-II device and package combination.

*Table 18:* **Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

| Standard | Package | |
|---|---|---|
| | CS, FG | PQ, TQ, VQ |
| LVTTL Slow Slew Rate, 2 mA drive | 68 | 36 |
| LVTTL Slow Slew Rate, 4 mA drive | 41 | 20 |
| LVTTL Slow Slew Rate, 6 mA drive | 29 | 15 |
| LVTTL Slow Slew Rate, 8 mA drive | 22 | 12 |
| LVTTL Slow Slew Rate, 12 mA drive | 17 | 9 |
| LVTTL Slow Slew Rate, 16 mA drive | 14 | 7 |
| LVTTL Slow Slew Rate, 24 mA drive | 9 | 5 |
| LVTTL Fast Slew Rate, 2 mA drive | 40 | 21 |
| LVTTL Fast Slew Rate, 4 mA drive | 24 | 12 |
| LVTTL Fast Slew Rate, 6 mA drive | 17 | 9 |
| LVTTL Fast Slew Rate, 8 mA drive | 13 | 7 |
| LVTTL Fast Slew Rate, 12 mA drive | 10 | 5 |
| LVTTL Fast Slew Rate, 16 mA drive | 8 | 4 |
| LVTTL Fast Slew Rate, 24 mA drive | 5 | 3 |
| LVCMOS2 | 10 | 5 |
| PCI | 8 | 4 |
| GTL | 4 | 4 |
| GTL+ | 4 | 4 |
| HSTL Class I | 18 | 9 |
| HSTL Class III | 9 | 5 |
| HSTL Class IV | 5 | 3 |
| SSTL2 Class I | 15 | 8 |
| SSTL2 Class II | 10 | 5 |
| SSTL3 Class I | 11 | 6 |
| SSTL3 Class II | 7 | 4 |
| CTT | 14 | 7 |
| AGP | 9 | 5 |

*Table 18:* **Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

**Notes:**
1. This analysis assumes a 35 pF load for each output.

*Table 19:* **Effective Output Power/Ground Pairs for Spartan-II Devices**

| Pkg. | Spartan-II Devices | | | | | |
|---|---|---|---|---|---|---|
| | XC2S 15 | XC2S 30 | XC2S 50 | XC2S 100 | XC2S 150 | XC2S 200 |
| VQ100 | 8 | 8 | - | - | - | - |
| CS144 | 12 | 12 | - | - | - | - |
| TQ144 | 12 | 12 | 12 | 12 | - | - |
| PQ208 | - | 16 | 16 | 16 | 16 | 16 |
| FG256 | - | - | 16 | 16 | 16 | 16 |
| FG456 | - | - | - | 48 | 48 | 48 |

## Termination Examples

Creating a design with the Versatile I/O features requires the instantiation of the desired library primitive within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the Versatile I/O features. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

## Revision History

| Date | Version | Description |
|---|---|---|
| 09/18/00 | 2.0 | Sectioned the Spartan-II Family data sheet into four modules. Corrected banking description. |
| 03/05/01 | 2.1 | Clarified guidelines for applying power to $V_{CCINT}$ and $V_{CCO}$ |
| 09/03/03 | 2.2 | The following changes were made:<br>• "Serial Modes," page 20 cautions about toggling $\overline{\text{WRITE}}$ during serial configuration.<br>• Maximum $V_{IH}$ values in Table 32 and Table 33 changed to 5.5V.<br>• In "Boundary Scan," page 13, removed sentence about lack of INTEST support.<br>• In Table 9, page 17, added note about the state of I/Os after power-on.<br>• In "Slave Parallel Mode," page 23, explained configuration bit alignment to SelectMap port. |
| 06/13/08 | 2.8 | Added note that TDI, TMS, and TCK have a default pull-up resistor. Added note on maximum daisy chain limit. Updated Figure 15 and Figure 18 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated DLL section. Recommended using property or attribute instead of primitive to define I/O properties. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| CTT | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.4 | $V_{REF}$ + 0.4 | 8 | –8 |
| AGP | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note (2) | Note (2) |

**Notes:**
1. $V_{OL}$ and $V_{OH}$ for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

# Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

## Global Clock Input to Output Delay for LVTTL, *with* DLL (Pin-to-Pin)(1)

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | All | -6 | -5 | |
| | | | Min | Max | Max | |
| $T_{ICKOFDLL}$ | Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *with* DLL. | All | | 2.9 | 3.3 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

## Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)(1)

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | All | -6 | -5 | |
| | | | Min | Max | Max | |
| $T_{ICKOF}$ | Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *without* DLL. | XC2S15 | | 4.5 | 5.4 | ns |
| | | XC2S30 | | 4.5 | 5.4 | ns |
| | | XC2S50 | | 4.5 | 5.4 | ns |
| | | XC2S100 | | 4.6 | 5.5 | ns |
| | | XC2S150 | | 4.6 | 5.5 | ns |
| | | XC2S200 | | 4.7 | 5.6 | ns |

**Notes:**
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

## IOB Input Delay Adjustments for Different Standards(1)

Input delays associated with the pad are specified for LVTTL. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol | Description | Standard | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -6 | -5 | |
| **Data Input Delay Adjustments** | | | | | |
| $T_{ILVTTL}$ | Standard-specific data input delay adjustments | LVTTL | 0 | 0 | ns |
| $T_{ILVCMOS2}$ | | LVCMOS2 | –0.04 | –0.05 | ns |
| $T_{IPCI33\_3}$ | | PCI, 33 MHz, 3.3V | –0.11 | –0.13 | ns |
| $T_{IPCI33\_5}$ | | PCI, 33 MHz, 5.0V | 0.26 | 0.30 | ns |
| $T_{IPCI66\_3}$ | | PCI, 66 MHz, 3.3V | –0.11 | –0.13 | ns |
| $T_{IGTL}$ | | GTL | 0.20 | 0.24 | ns |
| $T_{IGTLP}$ | | GTL+ | 0.11 | 0.13 | ns |
| $T_{IHSTL}$ | | HSTL | 0.03 | 0.04 | ns |
| $T_{ISSTL2}$ | | SSTL2 | –0.08 | –0.09 | ns |
| $T_{ISSTL3}$ | | SSTL3 | –0.04 | –0.05 | ns |
| $T_{ICTT}$ | | CTT | 0.02 | 0.02 | ns |
| $T_{IAGP}$ | | AGP | –0.06 | –0.07 | ns |

**Notes:**
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.

## DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| $F_{CLKINHF}$ | Input clock frequency (CLKDLLHF) | 60 | 200 | 60 | 180 | MHz |
| $F_{CLKINLF}$ | Input clock frequency (CLKDLL) | 25 | 100 | 25 | 90 | MHz |
| $T_{DLLPWHF}$ | Input clock pulse width (CLKDLLHF) | 2.0 | - | 2.4 | - | ns |
| $T_{DLLPWLF}$ | Input clock pulse width (CLKDLL) | 2.5 | - | 3.0 | - | ns |

## DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 52, page 63, provides definitions for various parameters in the table below.

| Symbol | Description | $F_{CLKIN}$ | CLKDLLHF | | CLKDLL | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $T_{IPTOL}$ | Input clock period tolerance | | - | 1.0 | - | 1.0 | ns |
| $T_{IJITCC}$ | Input clock jitter tolerance (cycle-to-cycle) | | - | ±150 | - | ±300 | ps |
| $T_{LOCK}$ | Time required for DLL to acquire lock | > 60 MHz | - | 20 | - | 20 | µs |
| | | 50-60 MHz | - | - | - | 25 | µs |
| | | 40-50 MHz | - | - | - | 50 | µs |
| | | 30-40 MHz | - | - | - | 90 | µs |
| | | 25-30 MHz | - | - | - | 120 | µs |
| $T_{OJITCC}$ | Output jitter (cycle-to-cycle) for any DLL clock output(1) | | - | ±60 | - | ±60 | ps |
| $T_{PHIO}$ | Phase offset between CLKIN and CLKO(2) | | - | ±100 | - | ±100 | ps |
| $T_{PHOO}$ | Phase offset between clock outputs on the DLL(3) | | - | ±140 | - | ±140 | ps |
| $T_{PHIOM}$ | Maximum phase difference between CLKIN and CLKO(4) | | - | ±160 | - | ±160 | ps |
| $T_{PHOOM}$ | Maximum phase difference between clock outputs on the DLL(5) | | - | ±200 | - | ±200 | ps |

**Notes:**

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

*Table 36:* **Spartan-II Family Package Options**

| Package | Leads | Type | Maximum I/O | Lead Pitch (mm) | Footprint Area (mm) | Height (mm) | Mass[(1)] (g) |
|---|---|---|---|---|---|---|---|
| VQ100 / VQG100 | 100 | Very Thin Quad Flat Pack (VQFP) | 60 | 0.5 | 16 x 16 | 1.20 | 0.6 |
| TQ144 / TQG144 | 144 | Thin Quad Flat Pack (TQFP) | 92 | 0.5 | 22 x 22 | 1.60 | 1.4 |
| CS144 / CSG144 | 144 | Chip Scale Ball Grid Array (CSBGA) | 92 | 0.8 | 12 x 12 | 1.20 | 0.3 |
| PQ208 / PQG208 | 208 | Plastic Quad Flat Pack (PQFP) | 140 | 0.5 | 30.6 x 30.6 | 3.70 | 5.3 |
| FG256 / FGG256 | 256 | Fine-pitch Ball Grid Array (FBGA) | 176 | 1.0 | 17 x 17 | 2.00 | 0.9 |
| FG456 / FGG456 | 456 | Fine-pitch Ball Grid Array (FBGA) | 284 | 1.0 | 23 x 23 | 2.60 | 2.2 |

**Notes:**

1. Package mass is ±10%.

Note: Some early versions of Spartan-II devices, including the XC2S15 and XC2S30 ES devices and the XC2S150 with date code 0045 or earlier, included a power-down pin. For more information, see Answer Record 10500.

## VCCO Banks

Some of the I/O standards require specific $V_{CCO}$ voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3 in Module 2). Each bank has multiple $V_{CCO}$ pins which must be connected to the same voltage. In the smaller packages, the $V_{CCO}$ pins are connected between banks, effectively reducing the number of independent banks available (see Table 37). These interconnected banks are shown in the Pinout Tables with $V_{CCO}$ pads for multiple banks connected to the same pin.

*Table 37:* **Independent VCCO Banks Available**

| Package | VQ100 PQ208 | CS144 TQ144 | FG256 FG456 |
|---|---|---|---|
| Independent Banks | 1 | 4 | 8 |

## Package Overview

Table 36 shows the six low-cost, space-saving production package styles for the Spartan-II family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS144" package becomes "CSG144" when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 38.

For additional package information, see UG112: *Device Package User Guide*.

## Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 38.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

*Table 38:* **Xilinx Package Documentation**

| Package | Drawing | MDDS |
|---|---|---|
| VQ100 | Package Drawing | PK173_VQ100 |
| VQG100 | | PK130_VQG100 |
| TQ144 | Package Drawing | PK169_TQ144 |
| TQG144 | | PK126_TQG144 |
| CS144 | Package Drawing | PK149_CS144 |
| CSG144 | | PK103_CSG144 |
| PQ208 | Package Drawing | PK166_PQ208 |
| PQG208 | | PK123_PQG208 |
| FG256 | Package Drawing | PK151_FG256 |
| FGG256 | | PK105_FGG256 |
| FG456 | Package Drawing | PK154_FG456 |
| FGG456 | | PK109_FGG456 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| **Function** | **Bank** | **VQ100** | **TQ144** | **CS144** | **PQ208** | **Bndry Scan** |
| I/O | 4 | - | - | - | P87 | 295 |
| I/O | 4 | - | - | - | P88 | 298 |
| I/O | 4 | - | P84 | K8 | P89 | 301 |
| I/O | 4 | - | P83 | N9 | P90 | 304 |
| $V_{CCINT}$ | - | P42 | P82 | M9 | P91 | - |
| $V_{CCO}$ | 4 | - | - | - | P92 | - |
| GND | - | - | P81 | L9 | P93 | - |
| I/O | 4 | P43 | P80 | K9 | P94 | 307 |
| I/O | 4 | P44 | P79 | N10 | P95 | 310 |
| I/O | 4 | - | P78 | M10 | P96 | 313 |
| I/O, $V_{REF}$ | 4 | P45 | P77 | L10 | P98 | 316 |
| I/O | 4 | - | - | - | P99 | 319 |
| I/O | 4 | - | P76 | N11 | P100 | 322 |
| I/O | 4 | P46 | P75 | M11 | P101 | 325 |
| I/O | 4 | P47 | P74 | L11 | P102 | 328 |
| GND | - | P48 | P73 | N12 | P103 | - |
| DONE | 3 | P49 | P72 | M12 | P104 | 331 |
| $V_{CCO}$ | 4 | P50 | P71 | N13 | P105 | - |
| $V_{CCO}$ | 3 | P50 | P70 | M13 | P105 | - |
| $\overline{\text{PROGRAM}}$ | - | P51 | P69 | L12 | P106 | 334 |
| I/O ($\overline{\text{INIT}}$) | 3 | P52 | P68 | L13 | P107 | 335 |
| I/O (D7) | 3 | P53 | P67 | K10 | P108 | 338 |
| I/O | 3 | - | P66 | K11 | P109 | 341 |
| I/O | 3 | - | - | - | P110 | 344 |
| I/O, $V_{REF}$ | 3 | P54 | P65 | K12 | P111 | 347 |
| I/O | 3 | - | P64 | K13 | P113 | 350 |
| I/O | 3 | P55 | P63 | J10 | P114 | 353 |
| I/O (D6) | 3 | P56 | P62 | J11 | P115 | 356 |
| GND | - | - | P61 | J12 | P116 | - |
| $V_{CCO}$ | 3 | - | - | - | P117 | - |
| I/O (D5) | 3 | P57 | P60 | J13 | P119 | 359 |
| I/O | 3 | P58 | P59 | H10 | P120 | 362 |
| I/O | 3 | - | - | - | P121 | 365 |
| I/O | 3 | - | - | - | P122 | 368 |
| I/O | 3 | - | - | - | P123 | 371 |
| GND | - | - | - | - | P124 | - |
| I/O, $V_{REF}$ | 3 | P59 | P58 | H11 | P125 | 374 |
| I/O (D4) | 3 | P60 | P57 | H12 | P126 | 377 |
| I/O | 3 | - | P56 | H13 | P127 | 380 |
| $V_{CCINT}$ | - | P61 | P55 | G12 | P128 | - |
| I/O, TRDY(1) | 3 | P62 | P54 | G13 | P129 | 386 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| **Function** | **Bank** | **VQ100** | **TQ144** | **CS144** | **PQ208** | **Bndry Scan** |
| $V_{CCO}$ | 3 | P63 | P53 | G11 | P130 | - |
| $V_{CCO}$ | 2 | P63 | P53 | G11 | P130 | - |
| GND | - | P64 | P52 | G10 | P131 | - |
| I/O, IRDY(1) | 2 | P65 | P51 | F13 | P132 | 389 |
| I/O | 2 | - | - | - | P133 | 392 |
| I/O | 2 | - | P50 | F12 | P134 | 395 |
| I/O (D3) | 2 | P66 | P49 | F11 | P135 | 398 |
| I/O, $V_{REF}$ | 2 | P67 | P48 | F10 | P136 | 401 |
| GND | - | - | - | - | P137 | - |
| I/O | 2 | - | - | - | P138 | 404 |
| I/O | 2 | - | - | - | P139 | 407 |
| I/O | 2 | - | - | - | P140 | 410 |
| I/O | 2 | P68 | P47 | E13 | P141 | 413 |
| I/O (D2) | 2 | P69 | P46 | E12 | P142 | 416 |
| $V_{CCO}$ | 2 | - | - | - | P144 | - |
| GND | - | - | P45 | E11 | P145 | - |
| I/O (D1) | 2 | P70 | P44 | E10 | P146 | 419 |
| I/O | 2 | P71 | P43 | D13 | P147 | 422 |
| I/O | 2 | - | P42 | D12 | P148 | 425 |
| I/O, $V_{REF}$ | 2 | P72 | P41 | D11 | P150 | 428 |
| I/O | 2 | - | - | - | P151 | 431 |
| I/O | 2 | - | P40 | C13 | P152 | 434 |
| I/O (DIN, D0) | 2 | P73 | P39 | C12 | P153 | 437 |
| I/O (DOUT, BUSY) | 2 | P74 | P38 | C11 | P154 | 440 |
| CCLK | 2 | P75 | P37 | B13 | P155 | 443 |
| $V_{CCO}$ | 2 | P76 | P36 | B12 | P156 | - |
| $V_{CCO}$ | 1 | P76 | P35 | A13 | P156 | - |
| TDO | 2 | P77 | P34 | A12 | P157 | - |
| GND | - | P78 | P33 | B11 | P158 | - |
| TDI | - | P79 | P32 | A11 | P159 | - |
| I/O ($\overline{\text{CS}}$) | 1 | P80 | P31 | D10 | P160 | 0 |
| I/O ($\overline{\text{WRITE}}$) | 1 | P81 | P30 | C10 | P161 | 3 |
| I/O | 1 | - | P29 | B10 | P162 | 6 |
| I/O | 1 | - | - | - | P163 | 9 |
| I/O, $V_{REF}$ | 1 | P82 | P28 | A10 | P164 | 12 |
| I/O | 1 | - | - | - | P166 | 15 |
| I/O | 1 | P83 | P27 | D9 | P167 | 18 |
| I/O | 1 | P84 | P26 | C9 | P168 | 21 |
| GND | - | - | P25 | B9 | P169 | - |
| $V_{CCO}$ | 1 | - | - | - | P170 | - |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| $V_{CCINT}$ | - | P85 | P24 | A9 | P171 | - |
| I/O | 1 | - | P23 | D8 | P172 | 24 |
| I/O | 1 | - | P22 | C8 | P173 | 27 |
| I/O | 1 | - | - | - | P174 | 30 |
| I/O | 1 | - | - | - | P175 | 33 |
| I/O | 1 | - | - | - | P176 | 36 |
| GND | - | - | - | - | P177 | - |
| I/O, $V_{REF}$ | 1 | P86 | P21 | B8 | P178 | 39 |
| I/O | 1 | - | - | - | P179 | 42 |
| I/O | 1 | - | P20 | A8 | P180 | 45 |
| I/O | 1 | P87 | P19 | B7 | P181 | 48 |
| I, GCK2 | 1 | P88 | P18 | A7 | P182 | 54 |
| GND | - | P89 | P17 | C7 | P183 | - |
| $V_{CCO}$ | 1 | P90 | P16 | D7 | P184 | - |
| $V_{CCO}$ | 0 | P90 | P16 | D7 | P184 | - |
| I, GCK3 | 0 | P91 | P15 | A6 | P185 | 55 |
| $V_{CCINT}$ | - | P92 | P14 | B6 | P186 | - |
| I/O | 0 | - | P13 | C6 | P187 | 62 |
| I/O | 0 | - | - | - | P188 | 65 |
| I/O, $V_{REF}$ | 0 | P93 | P12 | D6 | P189 | 68 |
| GND | - | - | - | - | P190 | - |
| I/O | 0 | - | - | - | P191 | 71 |
| I/O | 0 | - | - | - | P192 | 74 |
| I/O | 0 | - | - | - | P193 | 77 |
| I/O | 0 | - | P11 | A5 | P194 | 80 |
| I/O | 0 | - | P10 | B5 | P195 | 83 |
| $V_{CCINT}$ | - | P94 | P9 | C5 | P196 | - |
| $V_{CCO}$ | 0 | - | - | - | P197 | - |
| GND | - | - | P8 | D5 | P198 | - |
| I/O | 0 | P95 | P7 | A4 | P199 | 86 |
| I/O | 0 | P96 | P6 | B4 | P200 | 89 |
| I/O | 0 | - | - | - | P201 | 92 |

## XC2S30 Device Pinouts *(Continued)*

| XC2S30 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | VQ100 | TQ144 | CS144 | PQ208 | Bndry Scan |
| I/O, $V_{REF}$ | 0 | P97 | P5 | C4 | P203 | 95 |
| I/O | 0 | - | - | - | P204 | 98 |
| I/O | 0 | - | P4 | A3 | P205 | 101 |
| I/O | 0 | P98 | P3 | B3 | P206 | 104 |
| TCK | - | P99 | P2 | C3 | P207 | - |
| $V_{CCO}$ | 0 | P100 | P1 | A2 | P208 | - |
| $V_{CCO}$ | 7 | P100 | P144 | B2 | P208 | - |

04/18/01

**Notes:**
1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S30 Package Pins

**VQ100**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P28 | P29 | - | - | - | - |

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**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P104 | P105 | - | - | - | - |

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**CS144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| M3 | N3 | - | - | - | - |

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**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P7 | P13 | P38 | P44 | P55 | P56 |
| P60 | P97 | P112 | P118 | P143 | P149 |
| P165 | P202 | - | - | - | - |

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**Notes:**
1. For the PQ208 package, P13, P38, P118, and P143, which are Not Connected Pins on the XC2S30, are assigned to $V_{CCINT}$ on larger devices.

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O, $V_{REF}$ | 4 | P79 | P95 | T11 | AB16 | 502 |
| I/O | 4 | - | - | - | AB17 | 505 |
| I/O | 4 | P78 | P96 | N11 | V15 | 508 |
| I/O | 4 | - | - | R12 | Y16 | 511 |
| I/O | 4 | - | P97 | P11 | AB18 | 517 |
| I/O, $V_{REF}$ | 4 | P77 | P98 | T12 | AB19 | 520 |
| $V_{CCO}$ | 4 | - | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 4 | - | P99 | T13 | Y17 | 523 |
| I/O | 4 | - | - | N12 | V16 | 526 |
| I/O | 4 | - | - | - | W17 | 529 |
| I/O | 4 | P76 | P100 | R13 | AB20 | 532 |
| I/O | 4 | - | - | P12 | AA19 | 535 |
| I/O | 4 | P75 | P101 | P13 | AA20 | 541 |
| I/O | 4 | P74 | P102 | T14 | W18 | 544 |
| GND | - | P73 | P103 | GND* | GND* | - |
| DONE | 3 | P72 | P104 | R14 | Y19 | 547 |
| $V_{CCO}$ | 4 | P71 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P70 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{\text{PROGRAM}}$ | - | P69 | P106 | P15 | W20 | 550 |
| I/O ($\overline{\text{INIT}}$) | 3 | P68 | P107 | N15 | V19 | 551 |
| I/O (D7) | 3 | P67 | P108 | N14 | Y21 | 554 |
| I/O | 3 | - | - | T15 | W21 | 560 |
| I/O | 3 | P66 | P109 | M13 | U20 | 563 |
| I/O | 3 | - | - | - | U19 | 566 |
| I/O | 3 | - | - | R16 | T18 | 569 |
| I/O | 3 | - | P110 | M14 | W22 | 572 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P65 | P111 | L14 | U21 | 575 |
| I/O | 3 | - | P112 | M15 | T20 | 578 |
| I/O | 3 | - | - | L12 | T21 | 584 |
| I/O | 3 | P64 | P113 | P16 | R18 | 587 |
| I/O | 3 | - | - | - | U22 | 590 |
| I/O, $V_{REF}$ | 3 | P63 | P114 | L13 | R19 | 593 |
| I/O (D6) | 3 | P62 | P115 | N16 | T22 | 596 |
| GND | - | P61 | P116 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 3 | - | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P60 | P119 | M16 | R21 | 599 |
| I/O | 3 | P59 | P120 | K14 | P18 | 602 |
| I/O | 3 | - | - | L16 | P20 | 605 |
| I/O | 3 | - | P121 | K13 | P21 | 608 |
| I/O | 3 | - | P122 | L15 | N18 | 614 |
| I/O | 3 | - | P123 | K12 | N20 | 617 |
| GND | - | - | P124 | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P58 | P125 | K16 | N21 | 620 |
| I/O (D4) | 3 | P57 | P126 | J16 | N22 | 623 |
| I/O | 3 | - | - | J14 | M19 | 626 |
| I/O | 3 | P56 | P127 | K15 | M20 | 629 |
| $V_{CCINT}$ | - | P55 | P128 | E5 | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P54 | P129 | J15 | M22 | 638 |
| $V_{CCO}$ | 3 | P53 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P53 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P52 | P131 | GND* | GND* | - |
| I/O, IRDY(1) | 2 | P51 | P132 | H16 | L20 | 641 |
| I/O | 2 | - | P133 | H14 | L17 | 644 |
| I/O | 2 | P50 | P134 | H15 | L21 | 650 |
| I/O | 2 | - | - | J13 | L22 | 653 |
| I/O (D3) | 2 | P49 | P135 | G16 | K20 | 656 |
| I/O, $V_{REF}$ | 2 | P48 | P136 | H13 | K21 | 659 |
| GND | - | - | P137 | GND* | GND* | - |
| I/O | 2 | - | P138 | G14 | K22 | 662 |
| I/O | 2 | - | P139 | G15 | J21 | 665 |
| I/O | 2 | - | P140 | G12 | J18 | 671 |
| I/O | 2 | - | - | F16 | J22 | 674 |
| I/O | 2 | P47 | P141 | G13 | H19 | 677 |
| I/O (D2) | 2 | P46 | P142 | F15 | H20 | 680 |
| $V_{CCINT}$ | - | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | - | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P45 | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P44 | P146 | E16 | H22 | 683 |
| I/O, $V_{REF}$ | 2 | P43 | P147 | F14 | H18 | 686 |
| I/O | 2 | - | - | - | G21 | 689 |
| I/O | 2 | P42 | P148 | D16 | G18 | 692 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 2 | - | - | F12 | G20 | 695 |
| I/O | 2 | - | P149 | E15 | F19 | 701 |
| I/O, $V_{REF}$ | 2 | P41 | P150 | F13 | F21 | 704 |
| $V_{CCO}$ | 2 | - | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 2 | - | P151 | E14 | F20 | 707 |
| I/O | 2 | - | - | C16 | F18 | 710 |
| I/O | 2 | - | - | - | E21 | 713 |
| I/O | 2 | P40 | P152 | E13 | D22 | 716 |
| I/O | 2 | - | - | B16 | E20 | 719 |
| I/O (DIN, D0) | 2 | P39 | P153 | D14 | D20 | 725 |
| I/O (DOUT, BUSY) | 2 | P38 | P154 | C15 | C21 | 728 |
| CCLK | 2 | P37 | P155 | D15 | B22 | 731 |
| $V_{CCO}$ | 2 | P36 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| $V_{CCO}$ | 1 | P35 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P34 | P157 | B14 | A21 | - |
| GND | - | P33 | P158 | GND* | GND* | - |
| TDI | - | P32 | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P31 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P30 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | C12 | D17 | 9 |
| I/O | 1 | P29 | P162 | A14 | A19 | 12 |
| I/O | 1 | - | - | - | B18 | 15 |
| I/O | 1 | - | - | D12 | C17 | 18 |
| I/O | 1 | - | P163 | B12 | D16 | 21 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P28 | P164 | C11 | A18 | 24 |
| I/O | 1 | - | P165 | A13 | B17 | 27 |
| I/O | 1 | - | - | D11 | D15 | 33 |
| I/O | 1 | - | P166 | A12 | C16 | 36 |
| I/O | 1 | - | - | - | D14 | 39 |
| I/O, $V_{REF}$ | 1 | P27 | P167 | E11 | E14 | 42 |
| I/O | 1 | P26 | P168 | B11 | A16 | 45 |
| GND | - | P25 | P169 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 1 | - | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P24 | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P23 | P172 | A11 | C15 | 48 |
| I/O | 1 | P22 | P173 | C10 | B15 | 51 |
| I/O | 1 | - | - | - | F12 | 54 |
| I/O | 1 | - | P174 | B10 | C14 | 57 |
| I/O | 1 | - | P175 | D10 | D13 | 63 |
| I/O | 1 | - | P176 | A10 | C13 | 66 |
| GND | - | - | P177 | GND* | GND* | - |
| I/O, $V_{REF}$ | 1 | P21 | P178 | B9 | B13 | 69 |
| I/O | 1 | - | P179 | E10 | E12 | 72 |
| I/O | 1 | - | - | A9 | B12 | 75 |
| I/O | 1 | P20 | P180 | D9 | D12 | 78 |
| I/O | 1 | P19 | P181 | A8 | D11 | 84 |
| I, GCK2 | 1 | P18 | P182 | C9 | A11 | 90 |
| GND | - | P17 | P183 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P16 | P184 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P16 | P184 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P15 | P185 | B8 | C11 | 91 |
| $V_{CCINT}$ | - | P14 | P186 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 0 | P13 | P187 | A7 | A10 | 101 |
| I/O | 0 | - | - | D8 | B10 | 104 |

## Additional XC2S150 Package Pins

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

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**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

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## Additional XC2S150 Package Pins *(Continued)*

**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| F7 | F8 | F9 | F10 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U7 | U8 | U9 | U10 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A6 | A12 | A13 | A14 | B11 |
| B16 | C2 | C8 | C9 | D1 | D4 |
| D18 | D19 | E13 | E17 | E19 | F11 |
| G2 | G22 | H21 | J1 | J4 | K2 |
| K18 | K19 | L2 | L19 | M2 | M17 |
| M21 | N1 | P1 | P5 | P22 | R3 |
| R20 | R22 | U3 | U18 | V6 | W4 |
| W13 | W15 | W19 | Y5 | Y22 | AA1 |
| AA3 | AA9 | AA10 | AA11 | AA16 | AB7 |
| AB8 | AB12 | AB14 | AB21 | - | - |

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## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 6 | - | - | T2 | 449 |
| I/O | 6 | P43 | L4 | U1 | 452 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | M2 | R5 | 455 |
| I/O | 6 | - | - | V1 | 458 |
| I/O | 6 | - | - | T5 | 461 |
| I/O | 6 | P44 | L3 | U2 | 464 |
| I/O, $V_{REF}$ | 6 | P45 | N1 | T3 | 467 |
| $V_{CCO}$ | 6 | - | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | P46 | P1 | T4 | 470 |
| I/O | 6 | - | L5 | W1 | 473 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | - | V2 | 476 |
| I/O | 6 | - | - | U4 | 482 |
| I/O, $V_{REF}$ | 6 | P47 | N2 | Y1 | 485 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | M4 | W2 | 488 |
| I/O | 6 | - | - | V3 | 491 |
| I/O | 6 | - | - | V4 | 494 |
| I/O | 6 | P48 | R1 | Y2 | 500 |
| I/O | 6 | P49 | M3 | W3 | 503 |
| M1 | - | P50 | P2 | U5 | 506 |
| GND | - | P51 | GND* | GND* | - |
| M0 | - | P52 | N3 | AB2 | 507 |
| $V_{CCO}$ | 6 | P53 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| $V_{CCO}$ | 5 | P53 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| M2 | - | P54 | R3 | Y4 | 508 |
| I/O | 5 | - | - | W5 | 518 |
| I/O | 5 | - | - | AB3 | 521 |
| I/O | 5 | - | N5 | V7 | 524 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 5 | P57 | T2 | Y6 | 527 |
| I/O | 5 | - | - | AA4 | 530 |
| I/O | 5 | - | - | AB4 | 536 |
| I/O | 5 | - | P5 | W6 | 539 |
| I/O | 5 | P58 | T3 | Y7 | 542 |
| GND | - | - | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P59 | T4 | AA5 | 545 |
| I/O | 5 | P60 | M6 | AB5 | 548 |
| I/O | 5 | - | - | V8 | 551 |
| I/O | 5 | - | - | AA6 | 554 |
| I/O | 5 | - | T5 | AB6 | 557 |
| GND | - | - | GND* | GND* | - |
| I/O | 5 | P61 | N6 | AA7 | 560 |
| I/O | 5 | - | - | W7 | 563 |
| I/O, $V_{REF}$ | 5 | P62 | R5 | W8 | 569 |
| I/O | 5 | P63 | P6 | Y8 | 572 |
| GND | - | P64 | GND* | GND* | - |
| $V_{CCO}$ | 5 | P65 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCINT}$ | - | P66 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 5 | P67 | R6 | AA8 | 575 |
| I/O | 5 | P68 | M7 | V9 | 578 |
| I/O | 5 | - | - | AB8 | 581 |
| I/O | 5 | - | - | W9 | 584 |
| I/O | 5 | - | - | AB9 | 587 |
| GND | - | - | GND* | GND* | - |
| I/O | 5 | P69 | N7 | Y9 | 590 |
| I/O | 5 | - | - | V10 | 593 |
| I/O | 5 | - | - | AA9 | 596 |
| I/O | 5 | P70 | T6 | W10 | 599 |
| I/O | 5 | P71 | P7 | AB10 | 602 |
| GND | - | P72 | GND* | GND* | - |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P73 | P8 | Y10 | 605 |
| I/O | 5 | P74 | R7 | V11 | 608 |
| I/O | 5 | - | - | AA10 | 614 |
| I/O | 5 | - | T7 | W11 | 617 |
| I/O | 5 | P75 | T8 | AB11 | 620 |
| I/O | 5 | - | - | U11 | 623 |
| $V_{CCINT}$ | - | P76 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P77 | R8 | Y11 | 635 |
| $V_{CCO}$ | 5 | P78 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCO}$ | 4 | P78 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P79 | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | Bndry |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Scan |
| I, GCK0 | 4 | P80 | N8 | W12 | 636 |
| I/O | 4 | P81 | N9 | U12 | 640 |
| I/O | 4 | - | - | V12 | 646 |
| I/O | 4 | P82 | R9 | Y12 | 649 |
| I/O | 4 | - | N10 | AA12 | 652 |
| I/O | 4 | - | - | W13 | 655 |
| I/O | 4 | P83 | T9 | AB13 | 661 |
| I/O, $V_{REF}$ | 4 | P84 | P9 | AA13 | 664 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P85 | GND* | GND* | - |
| I/O | 4 | P86 | M10 | Y13 | 667 |
| I/O | 4 | P87 | R10 | V13 | 670 |
| I/O | 4 | - | - | AB14 | 673 |
| I/O | 4 | - | - | W14 | 676 |
| I/O | 4 | P88 | P10 | AA14 | 679 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | - | V14 | 682 |
| I/O | 4 | - | - | Y14 | 685 |
| I/O | 4 | - | - | W15 | 688 |
| I/O | 4 | P89 | T10 | AB15 | 691 |
| I/O | 4 | P90 | R11 | AA15 | 694 |
| $V_{CCINT}$ | - | P91 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | P92 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P93 | GND* | GND* | - |
| I/O | 4 | P94 | M11 | Y15 | 697 |
| I/O, $V_{REF}$ | 4 | P95 | T11 | AB16 | 700 |
| I/O | 4 | - | - | AB17 | 706 |
| I/O | 4 | P96 | N11 | V15 | 709 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | R12 | Y16 | 712 |
| I/O | 4 | - | - | AA17 | 715 |
| I/O | 4 | - | - | W16 | 718 |
| I/O | 4 | P97 | P11 | AB18 | 721 |
| I/O, $V_{REF}$ | 4 | P98 | T12 | AB19 | 724 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | P99 | T13 | Y17 | 727 |
| I/O | 4 | - | N12 | V16 | 730 |
| I/O | 4 | - | - | AA18 | 733 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | Bndry |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Scan |
| I/O | 4 | - | - | W17 | 739 |
| I/O, $V_{REF}$ | 4 | P100 | R13 | AB20 | 742 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | P12 | AA19 | 745 |
| I/O | 4 | - | - | V17 | 748 |
| I/O | 4 | - | - | Y18 | 751 |
| I/O | 4 | P101 | P13 | AA20 | 757 |
| I/O | 4 | P102 | T14 | W18 | 760 |
| GND | - | P103 | GND* | GND* | - |
| DONE | 3 | P104 | R14 | Y19 | 763 |
| $V_{CCO}$ | 4 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{\text{PROGRAM}}$ | - | P106 | P15 | W20 | 766 |
| I/O ($\overline{\text{INIT}}$) | 3 | P107 | N15 | V19 | 767 |
| I/O (D7) | 3 | P108 | N14 | Y21 | 770 |
| I/O | 3 | - | - | V20 | 776 |
| I/O | 3 | - | - | AA22 | 779 |
| I/O | 3 | - | T15 | W21 | 782 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P109 | M13 | U20 | 785 |
| I/O | 3 | - | - | U19 | 788 |
| I/O | 3 | - | - | V21 | 794 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | - | R16 | T18 | 797 |
| I/O | 3 | P110 | M14 | W22 | 800 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P111 | L14 | U21 | 803 |
| I/O | 3 | P112 | M15 | T20 | 806 |
| I/O | 3 | - | - | T19 | 809 |
| I/O | 3 | - | - | V22 | 812 |
| I/O | 3 | - | L12 | T21 | 815 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P113 | P16 | R18 | 818 |
| I/O | 3 | - | - | U22 | 821 |
| I/O, $V_{REF}$ | 3 | P114 | L13 | R19 | 827 |
| I/O (D6) | 3 | P115 | N16 | T22 | 830 |
| GND | - | P116 | GND* | GND* | - |