AMD Xilinx - XC2S15-5VQG100I Datasheet

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	96
Number of Logic Elements/Cells	432
Total RAM Bits	16384
Number of I/O	60
Number of Gates	15000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s15-5vqg100i

XILINX®

Spartan-II FPGA Family: Introduction and Ordering Information

DS001-1 (v2.8) June 13, 2008

Product Specification

Introduction

The Spartan®-II Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The six-member family offers densities ranging from 15,000 to 200,000 system gates, as shown in Table 1. System performance is supported up to 200 MHz. Features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards, and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-II family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 5,292 logic cells with up to 200,000 system gates
  - Streamlined features based on Virtex® FPGA architecture
  - Unlimited reprogrammability
  - Very low cost
  - Cost-effective 0.18 micron process
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K bit block RAM
    - Fast interfaces to external RAM
  - Fully PCI compliant
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 16 high-performance interface standards
  - Hot swap Compact PCI friendly
  - Zero hold time simplifies system timing
- Core logic powered at 2.5V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing

Table 1: **Spartan-II FPGA Family Members**

Device	Logic Cells	System Gates (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O[1]	Total Distributed RAM Bits	Total Block RAM Bits
XC2S15	432	15,000	8 x 12	96	86	6,144	16K
XC2S30	972	30,000	12 x 18	216	92	13,824	24K
XC2S50	1,728	50,000	16 x 24	384	176	24,576	32K
XC2S100	2,700	100,000	20 x 30	600	176	38,400	40K
XC2S150	3,888	150,000	24 x 36	864	260	55,296	48K
XC2S200	5,292	200,000	28 x 42	1,176	284	75,264	56K

Notes:

1. All user I/O counts do not include the four global clock/user input pins. See details in Table 2, page 4.

Spartan-II FPGA Family: Functional Description

DS001-2 (v2.8) June 13, 2008

Product Specification

Architectural Description

Spartan-II FPGA Array

The Spartan®-II field-programmable gate array, shown in Figure 2, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 2, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

Input/Output Block

The Spartan-II FPGA IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. Table 3 lists several of the standards which are supported along with the required reference, output and termination voltages needed to meet the standard.

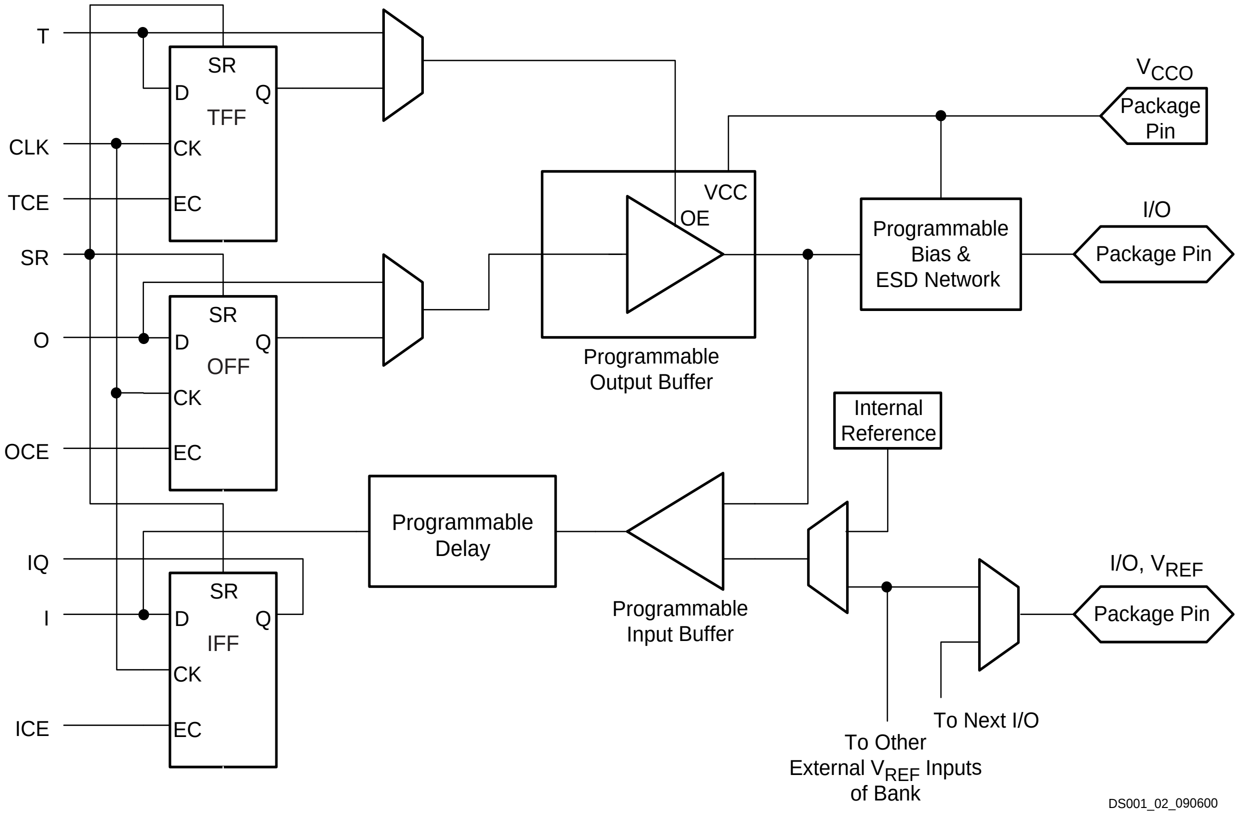

Figure 2: **Spartan-II FPGA Input/Output Block (IOB)**

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 7 lists the boundary-scan instructions supported in Spartan-II FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Table 7: **Boundary-Scan Instructions**

Boundary-Scan Command	Binary Code[4:0]	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE	00001	Enables boundary-scan SAMPLE operation
USR1	00010	Access user-defined register 1
USR2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration
INTEST	00111	Enables boundary-scan INTEST operation
USRCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIZ	01010	Disables output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx® reserved instructions

The public boundary-scan instructions are available prior to configuration. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Using Block RAM Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block RAM memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block RAM memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Block RAM memory supports two operating modes.

- Read Through
- Write Back

Read Through (One Clock Edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (One Clock Edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

Block RAM Characteristics

1. All inputs are registered with the port clock and have a setup to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The block RAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

Library Primitives

Figure 31 and Figure 32 show the two generic library block RAM primitives. Table 11 describes all of the available primitives for synthesis and simulation.

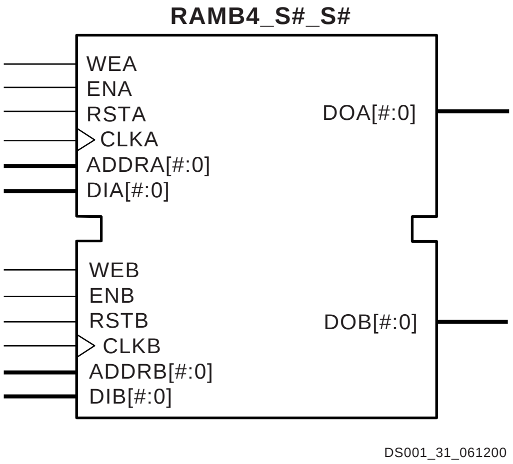

Figure 31: **Dual-Port Block RAM Memory**

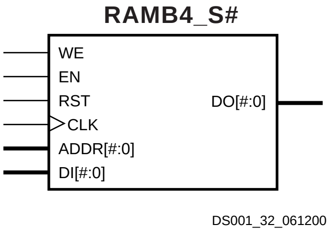

Figure 32: **Single-Port Block RAM Memory**

Table 11: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16

Table 11: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S4 RAMB4_S4_S4 RAMB4_S4_S8 RAMB4_S4_S16	4	N/A 4 8 16
RAMB4_S8 RAMB4_S8_S8 RAMB4_S8_S16	8	N/A 8 16
RAMB4_S16 RAMB4_S16_S16	16	N/A 16

Port Signals

Each block RAM port operates independently of the others while accessing the same set of 4096 memory cells.

Table 12 describes the depth and width aspect ratios for the block RAM memory.

Table 12: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A|B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A|B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A|B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A|B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 12.

Data In Bus—DI[A|B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 12.

Data Output Bus—DO[A|B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 12.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$\text{Start} = ([\text{ADDR}_{\text{port}} + 1] * \text{Width}_{\text{port}}) - 1$$

$$\text{End} = \text{ADDR}_{\text{port}} * \text{Width}_{\text{port}}$$

Table 13 shows low order address mapping for each port width.

Table 13: **Port Address Mapping**

Port Width	Port Addresses																
1	4095...	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features, system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 15, each buffer type can support a variety of voltage requirements.

Table 15: **Versatile I/O Supported Standards (Typical Values)**

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL (2-24 mA)	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	1.5
HSTL Class IV	0.9	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance JEDEC website at http://www.jedec.org. For more details on the I/O standards and termination application examples, see XAPP179, "*Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs.*"

LVTTL — Low-Voltage TTL

The Low-Voltage TTL (LVTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5V

The Low-Voltage CMOS for 2.5V or lower (LVCMOS2) standard is an extension of the LVCMOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

Spartan-II FPGA Family: DC and Switching Characteristics

DS001-3 (v2.8) June 13, 2008

Product Specification

Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All limits are representative of worst-case supply voltage and junction temperature conditions. Typical numbers are based on measurements taken at a nominal V_{CCINT} level of 2.5V and a junction temperature of 25°C. The parameters included are common to popular designs and typical applications. **All specifications are subject to change without notice.**

DC Specifications

Absolute Maximum Ratings(1)

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND(2)		–0.5	3.0	V
V_{CCO}	Supply voltage relative to GND(2)		–0.5	4.0	V
V_{REF}	Input reference voltage		–0.5	3.6	V
V_{IN}	Input voltage relative to GND(3)	5V tolerant I/O(4)	–0.5	5.5	V
		No 5V tolerance(5)	–0.5	V_{CCO} + 0.5	V
V_{TS}	Voltage applied to 3-state output	5V tolerant I/O(4)	–0.5	5.5	V
		No 5V tolerance(5)	–0.5	V_{CCO} + 0.5	V
T_{STG}	Storage temperature (ambient)		–65	+150	°C
T_J	Junction temperature		-	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Power supplies may turn on in any order.
3. V_{IN} should not exceed V_{CCO} by more than 3.6V over extended periods of time (e.g., longer than a day).
4. Spartan®-II device I/Os are 5V Tolerant whenever the LVTTL, LVCMOS2, or PCI33_5 signal standard has been selected. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA, and undershoot must be limited to either –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to +7.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
5. Without 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either V_{CCO} + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to V_{CCO} + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the Packaging Information on the Xilinx® web site.

Power-On Requirements

Spartan-II FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CCINT} lines for a successful power-on. If more current is available, the FPGA can consume more than I_{CCPO} minimum, though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Therefore the use of foldback/crowbar supplies and fuses deserves special attention. In these cases, limit the I_{CCPO} current to a level below the trip point for over-current protection in order to avoid inadvertently shutting down the supply.

		Conditions		New Requirements(1) For Devices with Date Code 0321 or Later		Old Requirements(1) For Devices with Date Code before 0321		
Symbol	**Description**	**Junction Temperature(2)**	**Device Temperature Grade**	**Min**	**Max**	**Min**	**Max**	**Units**
I_{CCPO}(3)	Total V_{CCINT} supply current required during power-on	–40°C ≤ T_J < –20°C	Industrial	1.50	-	2.00	-	A
		–20°C ≤ T_J < 0°C	Industrial	1.00	-	2.00	-	A
		0°C ≤ T_J ≤ 85°C	Commercial	0.25	-	0.50	-	A
		85°C < T_J ≤ 100°C	Industrial	0.50	-	0.50	-	A
T_{CCPO}(4,5)	V_{CCINT} ramp time	–40°C ≤ T_J ≤ 100°C	All	-	50	-	50	ms

Notes:

1. The date code is printed on the top of the device's package. See the "Device Part Marking" section in Module 1.
2. The expected T_J range for the design determines the I_{CCPO} minimum requirement. Use the applicable ranges in the junction temperature column to find the associated current values in the appropriate new or old requirements column according to the date code. Then choose the highest of these current values to serve as the minimum I_{CCPO} requirement that must be met. For example, if the junction temperature for a given design is -25°C ≤ T_J ≤ 75°C, then the new minimum I_{CCPO} requirement is 1.5A. If 5°C ≤ T_J ≤ 90°C, then the new minimum I_{CCPO} requirement is 0.5A.
3. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CCINT} ramps from 0 to 2.5V.
4. The ramp time is measured from GND to V_{CCINT} max on a fully loaded board.
5. During power-on, the V_{CCINT} ramp must increase steadily in voltage with no dips.
6. For more information on designing to meet the power-on specifications, refer to the application note **XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families"**

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	**V_{IL}**		**V_{IH}**		**V_{OL}**	**V_{OH}**	**I_{OL}**	**I_{OH}**
	V, Min	**V, Max**	**V, Min**	**V, Max**	**V, Max**	**V, Min**	**mA**	**mA**
LVTTL(1)	–0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3V	–0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)
PCI, 5.0V	–0.5	0.8	2.0	5.5	0.55	2.4	Note (2)	Note (2)
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	N/A	40	N/A
GTL+	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	N/A	36	N/A
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	15.2	–15.2

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Delay Adjustments for Different Standards," page 57.

Symbol	Description	Device	Speed Grade				Units
			-6		-5		
			Min	Max	Min	Max	
Propagation Delays							
T_{IOPI}	Pad to I output, no delay	All	-	0.8	-	1.0	ns
T_{IOPID}	Pad to I output, with delay	All	-	1.5	-	1.8	ns
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	-	1.7	-	2.0	ns
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S15	-	3.8	-	4.5	ns
		XC2S30	-	3.8	-	4.5	ns
		XC2S50	-	3.8	-	4.5	ns
		XC2S100	-	3.8	-	4.5	ns
		XC2S150	-	4.0	-	4.7	ns
		XC2S200	-	4.0	-	4.7	ns
Sequential Delays							
T_{IOCKIQ}	Clock CLK to output IQ	All	-	0.7	-	0.8	ns
Setup/Hold Times with Respect to Clock CLK(2)							
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	1.7 / 0	-	1.9 / 0	-	ns
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay(1)	XC2S15	3.8 / 0	-	4.4 / 0	-	ns
		XC2S30	3.8 / 0	-	4.4 / 0	-	ns
		XC2S50	3.8 / 0	-	4.4 / 0	-	ns
		XC2S100	3.8 / 0	-	4.4 / 0	-	ns
		XC2S150	3.9 / 0	-	4.6 / 0	-	ns
		XC2S200	3.9 / 0	-	4.6 / 0	-	ns
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	0.9 / 0.01	-	0.9 / 0.01	-	ns
Set/Reset Delays							
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All	-	1.1	-	1.2	ns
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	-	1.5	-	1.7	ns
T_{GSRQ}	GSR to output IQ	All	-	9.9	-	11.7	ns

Notes:

1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.
2. A zero hold time listing indicates no hold time or a negative hold time.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Propagation Delays						
T_{IOOP}	O input to pad	-	2.9	-	3.4	ns
T_{IOOLP}	O input to pad via transparent latch	-	3.4	-	4.0	ns
3-state Delays						
T_{IOTHZ}	T input to pad high-impedance(1)	-	2.0	-	2.3	ns
T_{IOTON}	T input to valid data on pad	-	3.0	-	3.6	ns
$T_{IOTLPHZ}$	T input to pad high impedance via transparent latch(1)	-	2.5	-	2.9	ns
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	-	3.5	-	4.2	ns
T_{GTS}	GTS to pad high impedance(1)	-	5.0	-	5.9	ns
Sequential Delays						
T_{IOCKP}	Clock CLK to pad	-	2.9	-	3.4	ns
T_{IOCKHZ}	Clock CLK to pad high impedance (synchronous)(1)	-	2.3	-	2.7	ns
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	-	3.3	-	4.0	ns
Setup/Hold Times with Respect to Clock CLK(2)						
T_{IOOCK} / T_{IOCKO}	O input	1.1 / 0	-	1.3 / 0	-	ns
$T_{IOOCECK}$ / $T_{IOCKOCE}$	OCE input	0.9 / 0.01	-	0.9 / 0.01	-	ns
$T_{IOSRCKO}$ / $T_{IOCKOSR}$	SR input (OFF)	1.2 / 0	-	1.3 / 0	-	ns
T_{IOTCK} / T_{IOCKT}	3-state setup times, T input	0.8 / 0	-	0.9 / 0	-	ns
$T_{IOTCECK}$ / $T_{IOCKTCE}$	3-state setup times, TCE input	1.0 / 0	-	1.0 / 0	-	ns
$T_{IOSRCKT}$ / $T_{IOCKTSR}$	3-state setup times, SR input (TFF)	1.1 / 0	-	1.2 / 0	-	ns
Set/Reset Delays						
T_{IOSRP}	SR input to pad (asynchronous)	-	3.7	-	4.4	ns
T_{IOSRHZ}	SR input to pad high impedance (asynchronous)(1)	-	3.1	-	3.7	ns
T_{IOSRON}	SR input to valid data on pad (asynchronous)	-	4.1	-	4.9	ns
T_{IOGSRQ}	GSR to pad	-	9.9	-	11.7	ns

Notes:

1. Three-state turn-off delays should not be adjusted.
2. A zero hold time listing indicates no hold time or a negative hold time.

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O Input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard as listed in the table "Constants for Calculating TIOOP", below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, T_{IOOP1}.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

Adj	is selected from "IOB Output Delay Adjustments for Different Standards", page 59, according to the I/O standard used
C_{LOAD}	is the capacitive load for the design
F_L	is the capacitance scaling factor

Delay Measurement Methodology

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} Typ[2]
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.80
GTL+	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.0
HSTL Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL Class III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL Class IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL3 I and II	$V_{REF} - 1.0$	$V_{REF} + 1.0$	V_{REF}	1.5
SSTL2 I and II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
CTT	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.5
AGP	$V_{REF} -$ $(0.2xV_{CCO})$	$V_{REF} +$ $(0.2xV_{CCO})$	V_{REF}	Per AGP Spec

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the table, "Constants for Calculating TIOOP". See Xilinx application note XAPP179 for the appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Constants for Calculating T_{IOOP}

Standard	C_{SL}[1] (pF)	F_L (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVCMOS2	35	0.041
PCI 33 MHz 5V	50	0.050
PCI 33 MHZ 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

1. I/O parameter measurements are made with the capacitance values shown above. See Xilinx application note XAPP179 for the appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Combinatorial Delays						
T_{ILO}	4-input function: F/G inputs to X/Y outputs	-	0.6	-	0.7	ns
T_{IF5}	5-input function: F/G inputs to F5 output	-	0.7	-	0.9	ns
T_{IF5X}	5-input function: F/G inputs to X output	-	0.9	-	1.1	ns
T_{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX	-	1.0	-	1.1	ns
T_{F5INY}	6-input function: F5IN input to Y output	-	0.4	-	0.4	ns
T_{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs	-	0.7	-	0.9	ns
T_{BYYB}	BY input to YB output	-	0.6	-	0.7	ns
Sequential Delays						
T_{CKO}	FF clock CLK to XQ/YQ outputs	-	1.1	-	1.3	ns
T_{CKLO}	Latch clock CLK to XQ/YQ outputs	-	1.2	-	1.5	ns
Setup/Hold Times with Respect to Clock CLK(1)						
T_{ICK} / T_{CKI}	4-input function: F/G inputs	1.3 / 0	-	1.4 / 0	-	ns
T_{IF5CK} / T_{CKIF5}	5-input function: F/G inputs	1.6 / 0	-	1.8 / 0	-	ns
T_{F5INCK} / T_{CKF5IN}	6-input function: F5IN input	1.0 / 0	-	1.1 / 0	-	ns
T_{IF6CK} / T_{CKIF6}	6-input function: F/G inputs via F6 MUX	1.6 / 0	-	1.8 / 0	-	ns
T_{DICK} / T_{CKDI}	BX/BY inputs	0.8 / 0	-	0.8 / 0	-	ns
T_{CECK} / T_{CKCE}	CE input	0.9 / 0	-	0.9 / 0	-	ns
T_{RCK} / T_{CKR}	SR/BY inputs (synchronous)	0.8 / 0	-	0.8 / 0	-	ns
Clock CLK						
T_{CH}	Minimum pulse width, High	-	1.9	-	1.9	ns
T_{CL}	Minimum pulse width, Low	-	1.9	-	1.9	ns
Set/Reset						
T_{RPW}	Minimum pulse width, SR/BY inputs	3.1	-	3.1	-	ns
T_{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	-	1.1	-	1.3	ns
T_{IOGSRQ}	Delay from GSR to XQ/YQ outputs	-	9.9	-	11.7	ns
F_{TOG}	Toggle frequency (for export control)	-	263	-	263	MHz

Notes:

1. A zero hold time listing indicates no hold time or a negative hold time.

Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Sequential Delays						
T_{BCKO}	Clock CLK to DOUT output	-	3.4	-	4.0	ns
Setup/Hold Times with Respect to Clock CLK[1]						
T_{BACK} / T_{BCKA}	ADDR inputs	1.4 / 0	-	1.4 / 0	-	ns
T_{BDCK}/ T_{BCKD}	DIN inputs	1.4 / 0	-	1.4 / 0	-	ns
T_{BECK}/ T_{BCKE}	EN inputs	2.9 / 0	-	3.2 / 0	-	ns
T_{BRCK}/ T_{BCKR}	RST input	2.7 / 0	-	2.9 / 0	-	ns
T_{BWCK}/ T_{BCKW}	WEN input	2.6 / 0	-	2.8 / 0	-	ns
Clock CLK						
T_{BPWH}	Minimum pulse width, High	-	1.9	-	1.9	ns
T_{BPWL}	Minimum pulse width, Low	-	1.9	-	1.9	ns
T_{BCCS}	CLKA -> CLKB setup time for different ports	-	3.0	-	4.0	ns

Notes:

1. A zero hold time listing indicates no hold time or a negative hold time.

TBUF Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
Combinatorial Delays				
T_{IO}	IN input to OUT output	0	0	ns
T_{OFF}	TRI input to OUT output high impedance	0.1	0.2	ns
T_{ON}	TRI input to valid data on OUT output	0.1	0.2	ns

JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Setup and Hold Times with Respect to TCK						
T_{TAPTCK} / T_{TCKTAP}	TMS and TDI setup and hold times	4.0 / 2.0	-	4.0 / 2.0	-	ns
Sequential Delays						
T_{TCKTDO}	Output delay from clock TCK to output TDO	-	11.0	-	11.0	ns
FTCK	Maximum TCK clock frequency	-	33	-	33	MHz

XC2S30 Device Pinouts

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
GND	-	P1	P143	A1	P1	-
TMS	-	P2	P142	B1	P2	-
I/O	7	P3	P141	C2	P3	113
I/O	7	-	P140	C1	P4	116
I/O	7	-	-	-	P5	119
I/O, V_{REF}	7	P4	P139	D4	P6	122
I/O	7	-	P138	D3	P8	125
I/O	7	P5	P137	D2	P9	128
I/O	7	P6	P136	D1	P10	131
GND	-	-	P135	E4	P11	-
V_{CCO}	7	-	-	-	P12	-
I/O	7	P7	P134	E3	P14	134
I/O	7	-	P133	E2	P15	137
I/O	7	-	-	-	P16	140
I/O	7	-	-	-	P17	143
I/O	7	-	-	-	P18	146
GND	-	-	-	-	P19	-
I/O, V_{REF}	7	P8	P132	E1	P20	149
I/O	7	P9	P131	F4	P21	152
I/O	7	-	P130	F3	P22	155
I/O	7	-	-	-	P23	158
I/O, IRDY(1)	7	P10	P129	F2	P24	161
GND	-	P11	P128	F1	P25	-
V_{CCO}	7	P12	P127	G2	P26	-
V_{CCO}	6	P12	P127	G2	P26	-
I/O, TRDY(1)	6	P13	P126	G1	P27	164
V_{CCINT}	-	P14	P125	G3	P28	-
I/O	6	-	P124	G4	P29	170
I/O	6	P15	P123	H1	P30	173
I/O, V_{REF}	6	P16	P122	H2	P31	176
GND	-	-	-	-	P32	-
I/O	6	-	-	-	P33	179
I/O	6	-	-	-	P34	182
I/O	6	-	-	-	P35	185
I/O	6	-	P121	H3	P36	188
I/O	6	P17	P120	H4	P37	191
V_{CCO}	6	-	-	-	P39	-
GND	-	-	P119	J1	P40	-
I/O	6	P18	P118	J2	P41	194
I/O	6	P19	P117	J3	P42	197
I/O	6	-	P116	J4	P43	200

XC2S30 Device Pinouts *(Continued)*

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
I/O, V_{REF}	6	P20	P115	K1	P45	203
I/O	6	-	-	-	P46	206
I/O	6	-	P114	K2	P47	209
I/O	6	P21	P113	K3	P48	212
I/O	6	P22	P112	L1	P49	215
M1	-	P23	P111	L2	P50	218
GND	-	P24	P110	L3	P51	-
M0	-	P25	P109	M1	P52	219
V_{CCO}	6	P26	P108	M2	P53	-
V_{CCO}	5	P26	P107	N1	P53	-
M2	-	P27	P106	N2	P54	220
I/O	5	-	P103	K4	P57	227
I/O	5	-	-	-	P58	230
I/O, V_{REF}	5	P30	P102	L4	P59	233
I/O	5	-	P101	M4	P61	236
I/O	5	P31	P100	N4	P62	239
I/O	5	P32	P99	K5	P63	242
GND	-	-	P98	L5	P64	-
V_{CCO}	5	-	-	-	P65	-
V_{CCINT}	-	P33	P97	M5	P66	-
I/O	5	-	P96	N5	P67	245
I/O	5	-	P95	K6	P68	248
I/O	5	-	-	-	P69	251
I/O	5	-	-	-	P70	254
I/O	5	-	-	-	P71	257
GND	-	-	-	-	P72	-
I/O, V_{REF}	5	P34	P94	L6	P73	260
I/O	5	-	-	-	P74	263
I/O	5	-	P93	M6	P75	266
V_{CCINT}	-	P35	P92	N6	P76	-
I, GCK1	5	P36	P91	M7	P77	275
V_{CCO}	5	P37	P90	N7	P78	-
V_{CCO}	4	P37	P90	N7	P78	-
GND	-	P38	P89	L7	P79	-
I, GCK0	4	P39	P88	K7	P80	276
I/O	4	P40	P87	N8	P81	280
I/O	4	-	P86	M8	P82	283
I/O	4	-	-	-	P83	286
I/O, V_{REF}	4	P41	P85	L8	P84	289
GND	-	-	-	-	P85	-
I/O	4	-	-	-	P86	292

XC2S30 Device Pinouts *(Continued)*

XC2S30 Pad Name						
Function	Bank	VQ100	TQ144	CS144	PQ208	Bndry Scan
V_{CCINT}	-	P85	P24	A9	P171	-
I/O	1	-	P23	D8	P172	24
I/O	1	-	P22	C8	P173	27
I/O	1	-	-	-	P174	30
I/O	1	-	-	-	P175	33
I/O	1	-	-	-	P176	36
GND	-	-	-	-	P177	-
I/O, V_{REF}	1	P86	P21	B8	P178	39
I/O	1	-	-	-	P179	42
I/O	1	-	P20	A8	P180	45
I/O	1	P87	P19	B7	P181	48
I, GCK2	1	P88	P18	A7	P182	54
GND	-	P89	P17	C7	P183	-
V_{CCO}	1	P90	P16	D7	P184	-
V_{CCO}	0	P90	P16	D7	P184	-
I, GCK3	0	P91	P15	A6	P185	55
V_{CCINT}	-	P92	P14	B6	P186	-
I/O	0	-	P13	C6	P187	62
I/O	0	-	-	-	P188	65
I/O, V_{REF}	0	P93	P12	D6	P189	68
GND	-	-	-	-	P190	-
I/O	0	-	-	-	P191	71
I/O	0	-	-	-	P192	74
I/O	0	-	-	-	P193	77
I/O	0	-	P11	A5	P194	80
I/O	0	-	P10	B5	P195	83
V_{CCINT}	-	P94	P9	C5	P196	-
V_{CCO}	0	-	-	-	P197	-
GND	-	-	P8	D5	P198	-
I/O	0	P95	P7	A4	P199	86
I/O	0	P96	P6	B4	P200	89
I/O	0	-	-	-	P201	92
I/O, V_{REF}	0	P97	P5	C4	P203	95
I/O	0	-	-	-	P204	98
I/O	0	-	P4	A3	P205	101
I/O	0	P98	P3	B3	P206	104
TCK	-	P99	P2	C3	P207	-
V_{CCO}	0	P100	P1	A2	P208	-
V_{CCO}	7	P100	P144	B2	P208	-

04/18/01

Notes:

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S30 Package Pins

VQ100

Not Connected Pins					
P28	P29	-	-	-	-

11/02/00

TQ144

Not Connected Pins					
P104	P105	-	-	-	-

11/02/00

CS144

Not Connected Pins					
M3	N3	-	-	-	-

11/02/00

PQ208

Not Connected Pins					
P7	P13	P38	P44	P55	P56
P60	P97	P112	P118	P143	P149
P165	P202	-	-	-	-

11/02/00

Notes:

1. For the PQ208 package, P13, P38, P118, and P143, which are Not Connected Pins on the XC2S30, are assigned to V_{CCINT} on larger devices.

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name						
Function	**Bank**	**TQ144**	**PQ208**	**FG256**	**FG456**	**Bndry Scan**
I/O, V_{REF}	4	P79	P95	T11	AB16	502
I/O	4	-	-	-	AB17	505
I/O	4	P78	P96	N11	V15	508
I/O	4	-	-	R12	Y16	511
I/O	4	-	P97	P11	AB18	517
I/O, V_{REF}	4	P77	P98	T12	AB19	520
V_{CCO}	4	-	-	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	-	-	GND*	GND*	-
I/O	4	-	P99	T13	Y17	523
I/O	4	-	-	N12	V16	526
I/O	4	-	-	-	W17	529
I/O	4	P76	P100	R13	AB20	532
I/O	4	-	-	P12	AA19	535
I/O	4	P75	P101	P13	AA20	541
I/O	4	P74	P102	T14	W18	544
GND	-	P73	P103	GND*	GND*	-
DONE	3	P72	P104	R14	Y19	547
V_{CCO}	4	P71	P105	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
V_{CCO}	3	P70	P105	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
$\overline{\text{PROGRAM}}$	-	P69	P106	P15	W20	550
I/O ($\overline{\text{INIT}}$)	3	P68	P107	N15	V19	551
I/O (D7)	3	P67	P108	N14	Y21	554
I/O	3	-	-	T15	W21	560
I/O	3	P66	P109	M13	U20	563
I/O	3	-	-	-	U19	566
I/O	3	-	-	R16	T18	569
I/O	3	-	P110	M14	W22	572
GND	-	-	-	GND*	GND*	-
V_{CCO}	3	-	-	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
I/O, V_{REF}	3	P65	P111	L14	U21	575
I/O	3	-	P112	M15	T20	578
I/O	3	-	-	L12	T21	584
I/O	3	P64	P113	P16	R18	587
I/O	3	-	-	-	U22	590
I/O, V_{REF}	3	P63	P114	L13	R19	593
I/O (D6)	3	P62	P115	N16	T22	596
GND	-	P61	P116	GND*	GND*	-

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name						
Function	**Bank**	**TQ144**	**PQ208**	**FG256**	**FG456**	**Bndry Scan**
V_{CCO}	3	-	P117	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
V_{CCINT}	-	-	P118	V_{CCINT}*	V_{CCINT}*	-
I/O (D5)	3	P60	P119	M16	R21	599
I/O	3	P59	P120	K14	P18	602
I/O	3	-	-	L16	P20	605
I/O	3	-	P121	K13	P21	608
I/O	3	-	P122	L15	N18	614
I/O	3	-	P123	K12	N20	617
GND	-	-	P124	GND*	GND*	-
I/O, V_{REF}	3	P58	P125	K16	N21	620
I/O (D4)	3	P57	P126	J16	N22	623
I/O	3	-	-	J14	M19	626
I/O	3	P56	P127	K15	M20	629
V_{CCINT}	-	P55	P128	E5	V_{CCINT}*	-
I/O, TRDY$^{(1)}$	3	P54	P129	J15	M22	638
V_{CCO}	3	P53	P130	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
V_{CCO}	2	P53	P130	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	P52	P131	GND*	GND*	-
I/O, IRDY$^{(1)}$	2	P51	P132	H16	L20	641
I/O	2	-	P133	H14	L17	644
I/O	2	P50	P134	H15	L21	650
I/O	2	-	-	J13	L22	653
I/O (D3)	2	P49	P135	G16	K20	656
I/O, V_{REF}	2	P48	P136	H13	K21	659
GND	-	-	P137	GND*	GND*	-
I/O	2	-	P138	G14	K22	662
I/O	2	-	P139	G15	J21	665
I/O	2	-	P140	G12	J18	671
I/O	2	-	-	F16	J22	674
I/O	2	P47	P141	G13	H19	677
I/O (D2)	2	P46	P142	F15	H20	680
V_{CCINT}	-	-	P143	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	2	-	P144	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	P45	P145	GND*	GND*	-
I/O (D1)	2	P44	P146	E16	H22	683
I/O, V_{REF}	2	P43	P147	F14	H18	686
I/O	2	-	-	-	G21	689
I/O	2	P42	P148	D16	G18	692

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name						
Function	**Bank**	**TQ144**	**PQ208**	**FG256**	**FG456**	**Bndry Scan**
I/O	2	-	-	F12	G20	695
I/O	2	-	P149	E15	F19	701
I/O, V_{REF}	2	P41	P150	F13	F21	704
V_{CCO}	2	-	-	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	-	-	GND*	GND*	-
I/O	2	-	P151	E14	F20	707
I/O	2	-	-	C16	F18	710
I/O	2	-	-	-	E21	713
I/O	2	P40	P152	E13	D22	716
I/O	2	-	-	B16	E20	719
I/O (DIN, D0)	2	P39	P153	D14	D20	725
I/O (DOUT, BUSY)	2	P38	P154	C15	C21	728
CCLK	2	P37	P155	D15	B22	731
V_{CCO}	2	P36	P156	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
V_{CCO}	1	P35	P156	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
TDO	2	P34	P157	B14	A21	-
GND	-	P33	P158	GND*	GND*	-
TDI	-	P32	P159	A15	B20	-
I/O ($\overline{CS}$)	1	P31	P160	B13	C19	0
I/O ($\overline{WRITE}$)	1	P30	P161	C13	A20	3
I/O	1	-	-	C12	D17	9
I/O	1	P29	P162	A14	A19	12
I/O	1	-	-	-	B18	15
I/O	1	-	-	D12	C17	18
I/O	1	-	P163	B12	D16	21
GND	-	-	-	GND*	GND*	-
V_{CCO}	1	-	-	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
I/O, V_{REF}	1	P28	P164	C11	A18	24
I/O	1	-	P165	A13	B17	27
I/O	1	-	-	D11	D15	33
I/O	1	-	P166	A12	C16	36
I/O	1	-	-	-	D14	39
I/O, V_{REF}	1	P27	P167	E11	E14	42
I/O	1	P26	P168	B11	A16	45
GND	-	P25	P169	GND*	GND*	-

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name						
Function	**Bank**	**TQ144**	**PQ208**	**FG256**	**FG456**	**Bndry Scan**
V_{CCO}	1	-	P170	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
V_{CCINT}	-	P24	P171	V_{CCINT}*	V_{CCINT}*	-
I/O	1	P23	P172	A11	C15	48
I/O	1	P22	P173	C10	B15	51
I/O	1	-	-	-	F12	54
I/O	1	-	P174	B10	C14	57
I/O	1	-	P175	D10	D13	63
I/O	1	-	P176	A10	C13	66
GND	-	-	P177	GND*	GND*	-
I/O, V_{REF}	1	P21	P178	B9	B13	69
I/O	1	-	P179	E10	E12	72
I/O	1	-	-	A9	B12	75
I/O	1	P20	P180	D9	D12	78
I/O	1	P19	P181	A8	D11	84
I, GCK2	1	P18	P182	C9	A11	90
GND	-	P17	P183	GND*	GND*	-
V_{CCO}	1	P16	P184	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
V_{CCO}	0	P16	P184	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
I, GCK3	0	P15	P185	B8	C11	91
V_{CCINT}	-	P14	P186	V_{CCINT}*	V_{CCINT}*	-
I/O	0	P13	P187	A7	A10	101
I/O	0	-	-	D8	B10	104

Additional XC2S100 Package Pins

TQ144

Not Connected Pins					
P104	P105	-	-	-	-

11/02/00

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

11/02/00

FG256

V_{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V_{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V_{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V_{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V_{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V_{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V_{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V_{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V_{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

11/02/00

FG456

V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					
F10	F7	F8	F9	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U10	U7	U8	U9
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A4	A5	A6	A12	A13
A14	A15	A17	B3	B6	B8
B11	B14	B16	B19	C1	C2
C8	C9	C12	C18	C22	D1
D4	D5	D10	D18	D19	D21
E4	E11	E13	E15	E16	E17
E19	E22	F4	F11	F22	G2
G3	G4	G19	G22	H1	H21
J1	J3	J4	J19	J20	K2
K18	K19	L2	L5	L18	L19
M2	M6	M17	M18	M21	N1
N5	N19	P1	P5	P19	P22
R1	R3	R20	R22	T5	T19
U3	U11	U18	V1	V2	V10
V12	V17	V3	V4	V6	V8
V20	V21	V22	W4	W5	W9
W13	W14	W15	W16	W19	Y5
Y14	Y18	Y22	AA1	AA3	AA6
AA9	AA10	AA11	AA16	AA17	AA18
AA22	AB3	AB4	AB7	AB8	AB12
AB14	AB21	-	-	-	-

11/02/00

XC2S150 Device Pinouts

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	221
I/O	7	-	-	E4	224
I/O	7	-	-	C1	227
I/O	7	-	A2	F5	230
GND	-	-	GND*	GND*	-
I/O	7	P4	B1	D2	233
I/O	7	-	-	E3	236
I/O	7	-	-	F4	239
I/O	7	-	E3	G5	242
I/O	7	P5	D2	F3	245
GND	-	-	GND*	GND*	-
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P6	C1	E2	248
I/O	7	P7	F3	E1	251
I/O	7	-	-	G4	254
I/O	7	-	-	G3	257
I/O	7	-	E2	H5	260
I/O	7	P8	E4	F2	263
I/O	7	-	-	F1	266
I/O, V_{REF}	7	P9	D1	H4	269
I/O	7	P10	E1	G1	272
GND	-	P11	GND*	GND*	-
V_{CCO}	7	P12	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCINT}	-	P13	V_{CCINT}*	V_{CCINT}*	-
I/O	7	P14	F2	H3	275
I/O	7	P15	G3	H2	278
I/O	7	-	-	H1	284
I/O	7	-	F1	J5	287
I/O	7	P16	F4	J2	290
I/O	7	-	-	J3	293
I/O	7	P17	F5	K5	299
I/O	7	P18	G2	K1	302
GND	-	P19	GND*	GND*	-
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P20	H3	K3	305
I/O	7	P21	G4	K4	308
I/O	7	-	H2	L6	311

XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	7	P22	G5	L1	314
I/O	7	-	-	L5	317
I/O	7	P23	H4	L4	320
I/O, IRDY(1)	7	P24	G1	L3	323
GND	-	P25	GND*	GND*	-
V_{CCO}	7	P26	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCO}	6	P26	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P27	J2	M1	326
V_{CCINT}	-	P28	V_{CCINT}*	V_{CCINT}*	-
I/O	6	-	-	M6	332
I/O	6	P29	H1	M3	335
I/O	6	-	J4	M4	338
I/O	6	P30	J1	M5	341
I/O, V_{REF}	6	P31	J3	N2	344
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	347
I/O	6	P34	K2	N4	350
I/O	6	-	-	N5	356
I/O	6	P35	K1	P2	359
I/O	6	-	K3	P4	362
I/O	6	-	-	R1	365
I/O	6	P36	L1	P3	371
I/O	6	P37	L2	R2	374
V_{CCINT}	-	P38	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	6	P39	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	377
I/O, V_{REF}	6	P42	M1	R4	380
I/O	6	-	-	T2	383
I/O	6	P43	L4	U1	386
I/O	6	-	M2	R5	389
I/O	6	-	-	V1	392
I/O	6	-	-	T5	395
I/O	6	P44	L3	U2	398
I/O, V_{REF}	6	P45	N1	T3	401
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-

XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	4	P90	R11	AA15	595
V_{CCINT}	-	P91	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	4	P92	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P93	GND*	GND*	-
I/O	4	P94	M11	Y15	598
I/O, V_{REF}	4	P95	T11	AB16	601
I/O	4	-	-	AB17	604
I/O	4	P96	N11	V15	607
I/O	4	-	R12	Y16	610
I/O	4	-	-	AA17	613
I/O	4	-	-	W16	616
I/O	4	P97	P11	AB18	619
I/O, V_{REF}	4	P98	T12	AB19	622
V_{CCO}	4	-	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	-	GND*	GND*	-
I/O	4	P99	T13	Y17	625
I/O	4	-	N12	V16	628
I/O	4	-	-	AA18	631
I/O	4	-	-	W17	634
I/O	4	P100	R13	AB20	637
GND	-	-	GND*	GND*	-
I/O	4	-	P12	AA19	640
I/O	4	-	-	V17	643
I/O	4	-	-	Y18	646
I/O	4	P101	P13	AA20	649
I/O	4	P102	T14	W18	652
GND	-	P103	GND*	GND*	-
DONE	3	P104	R14	Y19	655
V_{CCO}	4	P105	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
V_{CCO}	3	P105	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
$\overline{\text{PROGRAM}}$	-	P106	P15	W20	658
I/O ($\overline{\text{INIT}}$)	3	P107	N15	V19	659
I/O (D7)	3	P108	N14	Y21	662
I/O	3	-	-	V20	665
I/O	3	-	-	AA22	668
I/O	3	-	T15	W21	671
GND	-	-	GND*	GND*	-
I/O	3	P109	M13	U20	674

XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	3	-	-	U19	677
I/O	3	-	-	V21	680
I/O	3	-	R16	T18	683
I/O	3	P110	M14	W22	686
GND	-	-	GND*	GND*	-
V_{CCO}	3	-	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
I/O, V_{REF}	3	P111	L14	U21	689
I/O	3	P112	M15	T20	692
I/O	3	-	-	T19	695
I/O	3	-	-	V22	698
I/O	3	-	L12	T21	701
I/O	3	P113	P16	R18	704
I/O	3	-	-	U22	707
I/O, V_{REF}	3	P114	L13	R19	710
I/O (D6)	3	P115	N16	T22	713
GND	-	P116	GND*	GND*	-
V_{CCO}	3	P117	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
V_{CCINT}	-	P118	V_{CCINT}*	V_{CCINT}*	-
I/O (D5)	3	P119	M16	R21	716
I/O	3	P120	K14	P18	719
I/O	3	-	-	P19	725
I/O	3	-	L16	P20	728
I/O	3	P121	K13	P21	731
I/O	3	-	-	N19	734
I/O	3	P122	L15	N18	740
I/O	3	P123	K12	N20	743
GND	-	P124	GND*	GND*	-
V_{CCO}	3	-	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
I/O, V_{REF}	3	P125	K16	N21	746
I/O (D4)	3	P126	J16	N22	749
I/O	3	-	J14	M19	752
I/O	3	P127	K15	M20	755
I/O	3	-	-	M18	758
V_{CCINT}	-	P128	V_{CCINT}*	V_{CCINT}*	-
I/O, TRDY(1)	3	P129	J15	M22	764
V_{CCO}	3	P130	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
V_{CCO}	2	P130	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	P131	GND*	GND*	-