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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	96
Number of Logic Elements/Cells	432
Total RAM Bits	16384
Number of I/O	86
Number of Gates	15000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-TFBGA, CSPBGA
Supplier Device Package	144-LCSBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s15-6cs144c

Architectural Description

Spartan-II FPGA Array

The Spartan®-II field-programmable gate array, shown in Figure 2, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 2, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

Input/Output Block

The Spartan-II FPGA IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. Table 3 lists several of the standards which are supported along with the required reference, output and termination voltages needed to meet the standard.

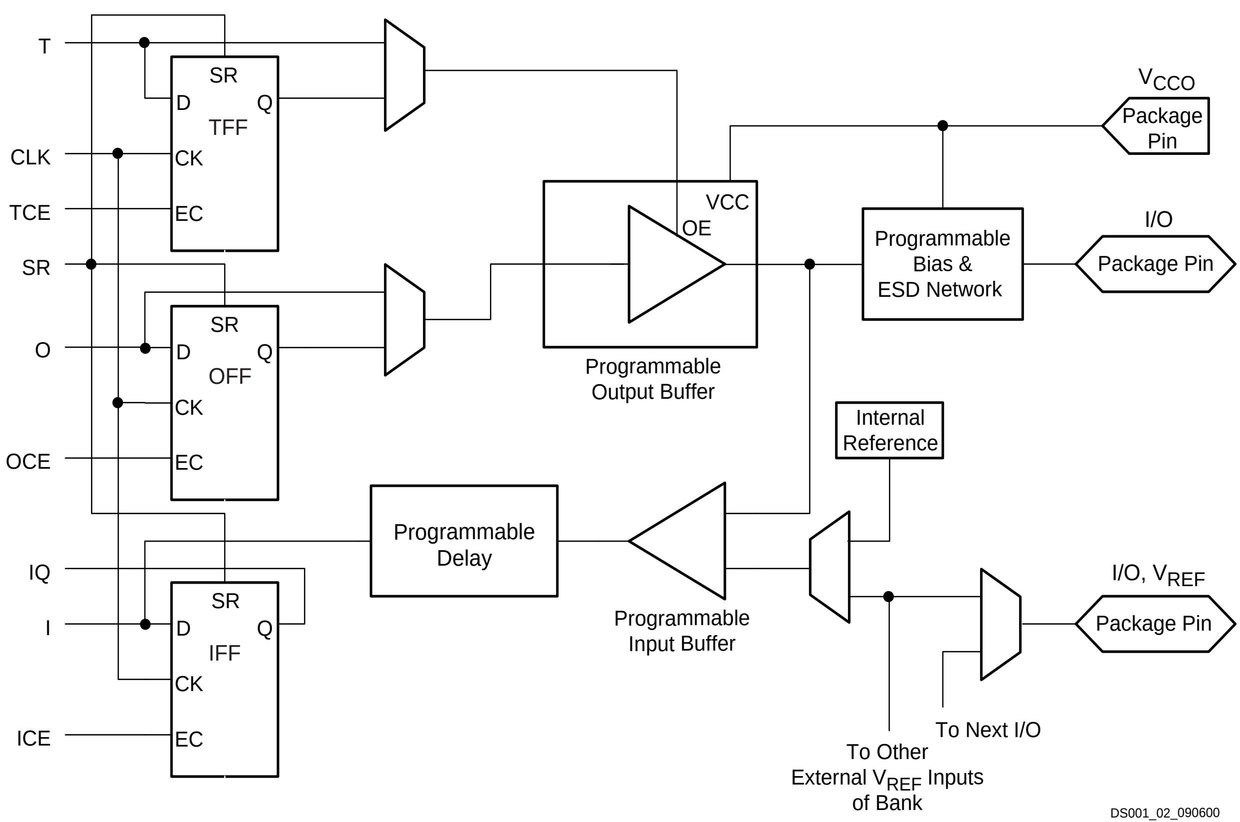


Figure 2: **Spartan-II FPGA Input/Output Block (IOB)**

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-II FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-II FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing," page 12. Each Spartan-II FPGA BUFT has an independent 3-state control pin and an independent input pin.

Block RAM

Spartan-II FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks.

Table 5: **Spartan-II Block RAM Amounts**

Spartan-II Device	# of Blocks	Total Block RAM Bits
XC2S15	4	16K
XC2S30	6	24K
XC2S50	8	32K
XC2S100	10	40K
XC2S150	12	48K
XC2S200	14	56K

Each block RAM cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

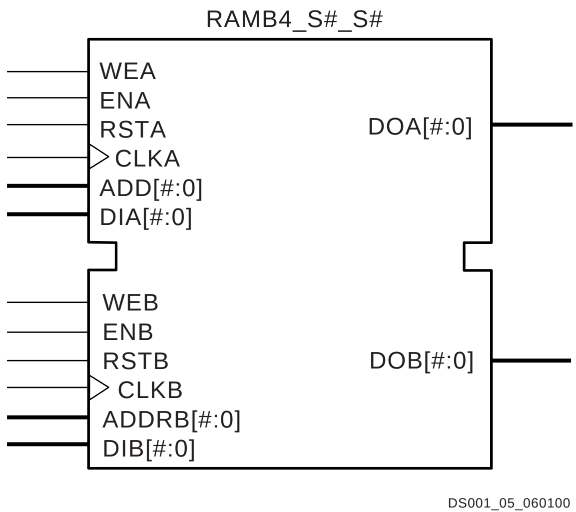


Figure 5: **Dual-Port Block RAM**

Table 6 shows the depth and width aspect ratios for the block RAM.

Table 6: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-II FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The local routing resources, as shown in Figure 6, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM)
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

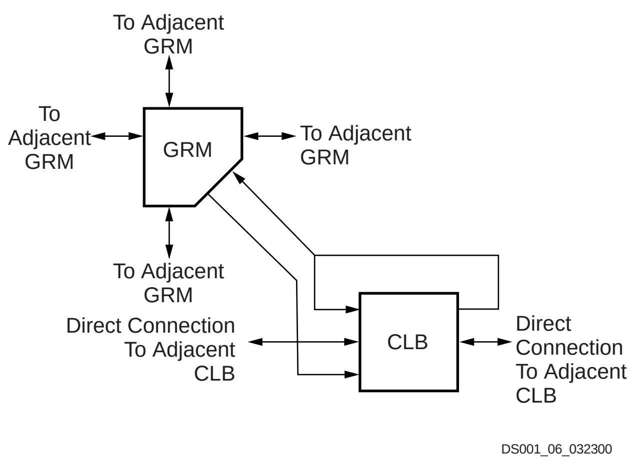


Figure 6: **Spartan-II Local Routing**

General Purpose Routing

Most Spartan-II FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-II devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Dedicated Routing

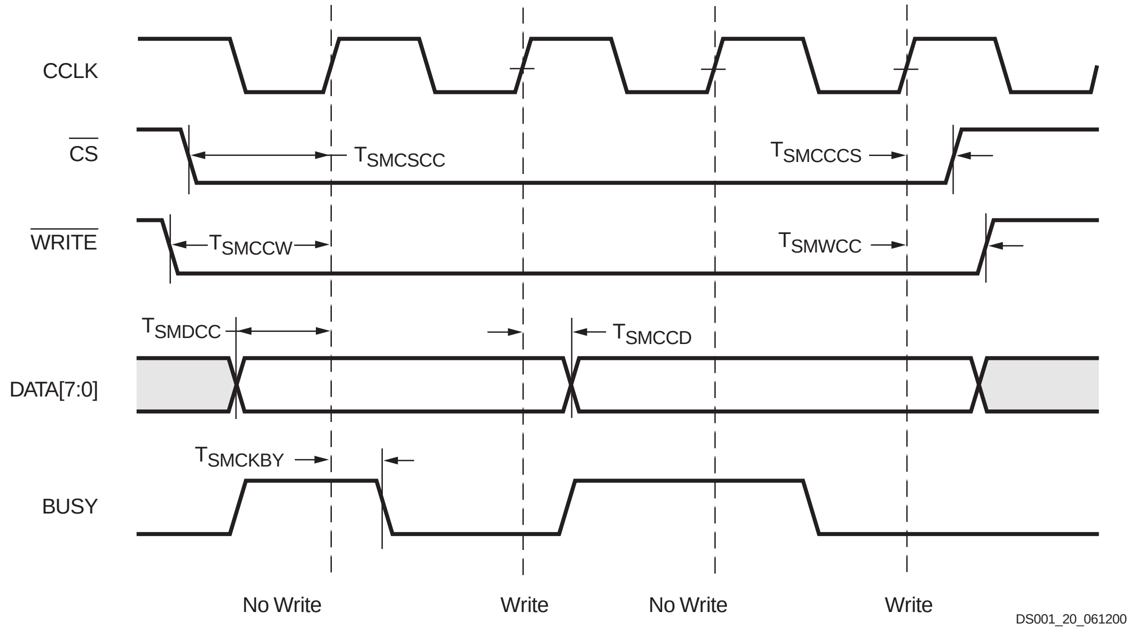
Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-II architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 7.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-II devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.



Symbol		Description		Units
T_{SMDCC}	CCLK	D0-D7 setup/hold	5	ns, min
T_{SMCCD}		D0-D7 hold	0	ns, min
T_{SMCSCC}		$\overline{CS}$ setup	7	ns, min
T_{SMCCCS}		$\overline{CS}$ hold	0	ns, min
T_{SMCCW}		$\overline{WRITE}$ setup	7	ns, min
T_{SMWCC}		$\overline{WRITE}$ hold	0	ns, min
T_{SMCKBY}		BUSY propagation delay	12	ns, max
F_{CC}		Maximum frequency	66	MHz, max
F_{CCNH}		Maximum frequency with no handshake	50	MHz, max

Figure 20: **Slave Parallel Write Timing**

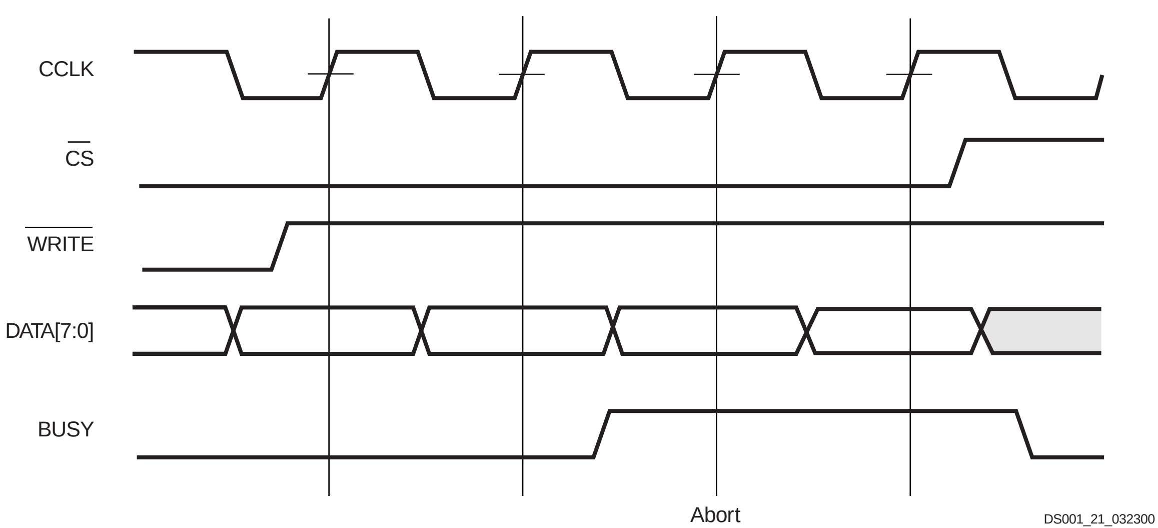


Figure 21: **Slave Parallel Write Abort Waveforms**

Design Considerations

This section contains more detailed design information on the following features:

- Delay-Locked Loop . . . see page 27
- Block RAM . . . see page 32
- Versatile I/O . . . see page 36

Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Primitives

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.

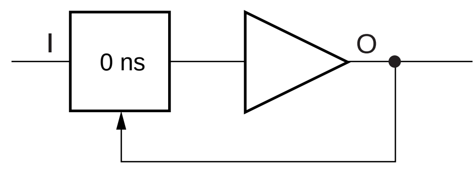


Figure 22: **Simplified DLL Macro BUFGDLL**

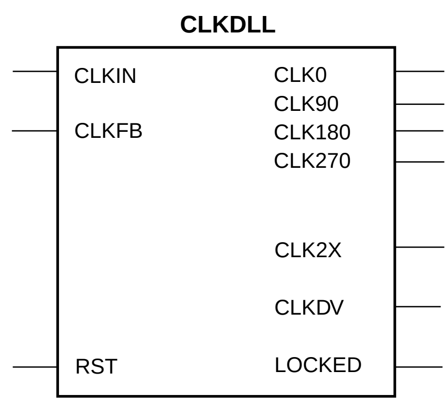


Figure 23: **Standard DLL Primitive CLKDLL**

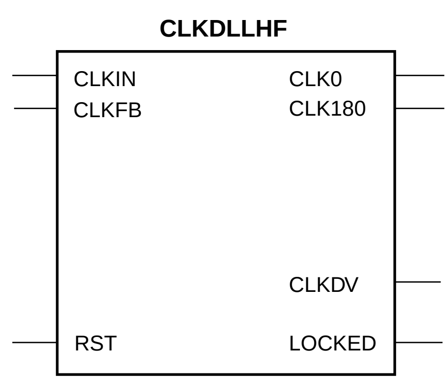


Figure 24: **High-Frequency DLL Primitive CLKDLLHF**

Using Block RAM Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block RAM memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block RAM memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Block RAM memory supports two operating modes.

- Read Through
- Write Back

Read Through (One Clock Edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (One Clock Edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

Block RAM Characteristics

1. All inputs are registered with the port clock and have a setup to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The block RAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

Library Primitives

Figure 31 and Figure 32 show the two generic library block RAM primitives. Table 11 describes all of the available primitives for synthesis and simulation.

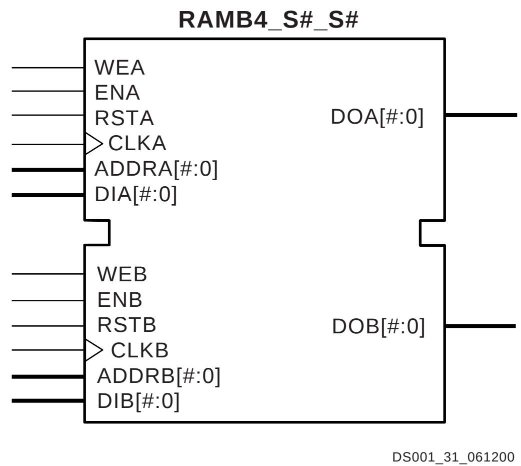


Figure 31: **Dual-Port Block RAM Memory**

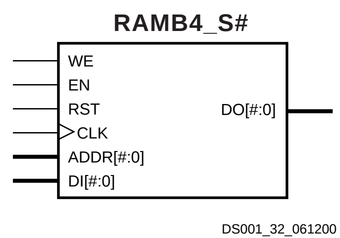


Figure 32: **Single-Port Block RAM Memory**

Table 11: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16

Table 11: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S4 RAMB4_S4_S4 RAMB4_S4_S8 RAMB4_S4_S16	4	N/A 4 8 16
RAMB4_S8 RAMB4_S8_S8 RAMB4_S8_S16	8	N/A 8 16
RAMB4_S16 RAMB4_S16_S16	16	N/A 16

Port Signals

Each block RAM port operates independently of the others while accessing the same set of 4096 memory cells.

Table 12 describes the depth and width aspect ratios for the block RAM memory.

Table 12: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A|B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A|B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A|B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A|B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 12.

Data In Bus—DI[A|B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 12.

Data Output Bus—DO[A|B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 12.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$\text{Start} = ([\text{ADDR}_{\text{port}} + 1] * \text{Width}_{\text{port}}) - 1$$

$$\text{End} = \text{ADDR}_{\text{port}} * \text{Width}_{\text{port}}$$

Table 13 shows low order address mapping for each port width.

Table 13: **Port Address Mapping**

Port Width	Port Addresses																
1	4095...	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features, system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 15, each buffer type can support a variety of voltage requirements.

Table 15: **Versatile I/O Supported Standards (Typical Values)**

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL (2-24 mA)	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	1.5
HSTL Class IV	0.9	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance JEDEC website at http://www.jedec.org. For more details on the I/O standards and termination application examples, see XAPP179, "*Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs.*"

LVTTL — Low-Voltage TTL

The Low-Voltage TTL (LVTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5V

The Low-Voltage CMOS for 2.5V or lower (LVCMOS2) standard is an extension of the LVCMOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

SSTL3 Class I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 47. DC voltage specifications appear in Table 25 for the SSTL3_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

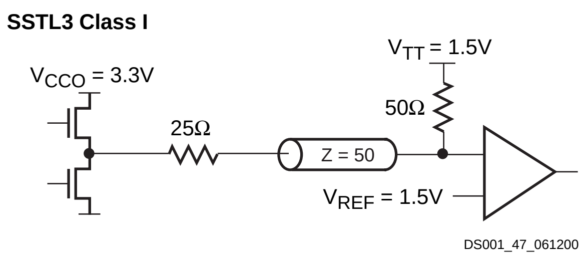


Figure 47: **Terminated SSTL3 Class I**

Table 25: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.6$	1.9	-	-
$V_{OL} \leq V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3.
2. V_{IL} minimum does not conform to the formula.

SSTL3 Class II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 48. DC voltage specifications appear in Table 26 for the SSTL3_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

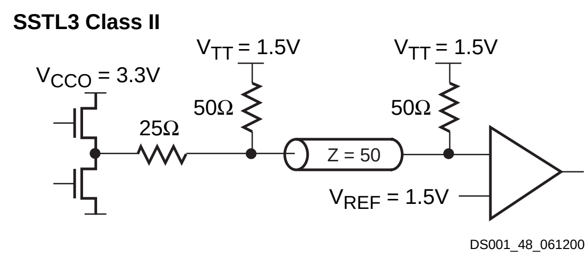


Figure 48: **Terminated SSTL3 Class II**

Table 26: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.8$	2.1	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T_J	Junction temperature[1]	Commercial	0	85	°C
		Industrial	–40	100	°C
V_{CCINT}	Supply voltage relative to GND[2,5]	Commercial	2.5 – 5%	2.5 + 5%	V
		Industrial	2.5 – 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND[3,5]	Commercial	1.4	3.6	V
		Industrial	1.4	3.6	V
T_{IN}	Input signal transition time[4]		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Functional operation is guaranteed down to a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} – 10%). For every 50 mV reduction in V_{CCINT} below 2.375V (nominal V_{CCINT} – 5%), all delay parameters increase by 3%.
3. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
4. Input and output measurement threshold is ~50% of V_{CCO}. See "Delay Measurement Methodology," page 60 for specific levels.
5. Supply voltages may be applied in any order desired.

DC Characteristics Over Operating Conditions

Symbol	Description			Min	Typ	Max	Units
V_{DRINT}	Data Retention V_{CCINT} voltage (below which configuration data may be lost)			2.0	-	-	V
V_{DRIO}	Data Retention V_{CCO} voltage (below which configuration data may be lost)			1.2	-	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current[1]	XC2S15	Commercial	-	10	30	mA
			Industrial	-	10	60	mA
		XC2S30	Commercial	-	10	30	mA
			Industrial	-	10	60	mA
		XC2S50	Commercial	-	12	50	mA
			Industrial	-	12	100	mA
		XC2S100	Commercial	-	12	50	mA
			Industrial	-	12	100	mA
		XC2S150	Commercial	-	15	50	mA
			Industrial	-	15	100	mA
		XC2S200	Commercial	-	15	75	mA
			Industrial	-	15	150	mA
I_{CCOQ}	Quiescent V_{CCO} supply current[1]			-	-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin			-	-	20	µA
I_L	Input or output leakage current[2]			–10	-	+10	µA
C_{IN}	Input capacitance (sample tested)	VQ, CS, TQ, PQ, FG packages		-	-	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)[3]			-	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested)[3]			-	-	0.15	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. The I/O leakage current specification applies only when the V_{CCINT} and V_{CCO} supply voltages have reached their respective minimum Recommended Operating Conditions.
3. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

Power-On Requirements

Spartan-II FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CCINT} lines for a successful power-on. If more current is available, the FPGA can consume more than I_{CCPO} minimum, though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Therefore the use of foldback/crowbar supplies and fuses deserves special attention. In these cases, limit the I_{CCPO} current to a level below the trip point for over-current protection in order to avoid inadvertently shutting down the supply.

Symbol	Description	Conditions		New Requirements[1] For Devices with Date Code 0321 or Later		Old Requirements[1] For Devices with Date Code before 0321		Units
		Junction Temperature[2]	Device Temperature Grade	Min	Max	Min	Max	
I_{CCPO}[3]	Total V_{CCINT} supply current required during power-on	$-40°C \leq T_J < -20°C$	Industrial	1.50	-	2.00	-	A
		$-20°C \leq T_J < 0°C$	Industrial	1.00	-	2.00	-	A
		$0°C \leq T_J \leq 85°C$	Commercial	0.25	-	0.50	-	A
		$85°C < T_J \leq 100°C$	Industrial	0.50	-	0.50	-	A
T_{CCPO}[4,5]	V_{CCINT} ramp time	$-40°C \leq T_J \leq 100°C$	All	-	50	-	50	ms

Notes:
1. The date code is printed on the top of the device's package. See the "Device Part Marking" section in Module 1.
2. The expected T_J range for the design determines the I_{CCPO} minimum requirement. Use the applicable ranges in the junction temperature column to find the associated current values in the appropriate new or old requirements column according to the date code. Then choose the highest of these current values to serve as the minimum I_{CCPO} requirement that must be met. For example, if the junction temperature for a given design is $-25°C \leq T_J \leq 75°C$, then the new minimum I_{CCPO} requirement is 1.5A. If $5°C \leq T_J \leq 90°C$, then the new minimum I_{CCPO} requirement is 0.5A.
3. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CCINT} ramps from 0 to 2.5V.
4. The ramp time is measured from GND to V_{CCINT} max on a fully loaded board.
5. During power-on, the V_{CCINT} ramp must increase steadily in voltage with no dips.
6. For more information on designing to meet the power-on specifications, refer to the application note **XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families"**

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL[1]	–0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3V	–0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)
PCI, 5.0V	–0.5	0.8	2.0	5.5	0.55	2.4	Note (2)	Note (2)
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	N/A	40	N/A
GTL+	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	N/A	36	N/A
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	15.2	–15.2

Calculation of T_{IOOP} as a Function of Capacitance

T_{IOOP} is the propagation delay from the O Input of the IOB to the pad. The values for T_{IOOP} are based on the standard capacitive load (C_{SL}) for each I/O standard as listed in the table "Constants for Calculating TIOOP", below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, T_{IOOP1}.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

Adj is selected from "IOB Output Delay Adjustments for Different Standards", page 59, according to the I/O standard used

C_{LOAD} is the capacitive load for the design

F_L is the capacitance scaling factor

Delay Measurement Methodology

Standard	V_L (1)	V_H (1)	Meas. Point	V_{REF} Typ(2)
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	0.80
GTL+	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.0
HSTL Class I	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.75
HSTL Class III	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
HSTL Class IV	$V_{REF} - 0.5$	$V_{REF} + 0.5$	V_{REF}	0.90
SSTL3 I and II	$V_{REF} - 1.0$	$V_{REF} + 1.0$	V_{REF}	1.5
SSTL2 I and II	$V_{REF} - 0.75$	$V_{REF} + 0.75$	V_{REF}	1.25
CTT	$V_{REF} - 0.2$	$V_{REF} + 0.2$	V_{REF}	1.5
AGP	$V_{REF} - (0.2xV_{CCO})$	$V_{REF} + (0.2xV_{CCO})$	V_{REF}	Per AGP Spec

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the table, "Constants for Calculating TIOOP". See Xilinx application note XAPP179 for the appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Constants for Calculating T_{IOOP}

Standard	C_{SL} (1) (pF)	F_L (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVCMOS2	35	0.041
PCI 33 MHz 5V	50	0.050
PCI 33 MHZ 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

1. I/O parameter measurements are made with the capacitance values shown above. See Xilinx application note XAPP179 for the appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Sequential Delays						
T_{BCKO}	Clock CLK to DOUT output	-	3.4	-	4.0	ns
Setup/Hold Times with Respect to Clock CLK(1)						
T_{BACK} / T_{BCKA}	ADDR inputs	1.4 / 0	-	1.4 / 0	-	ns
T_{BDCK}/ T_{BCKD}	DIN inputs	1.4 / 0	-	1.4 / 0	-	ns
T_{BECK}/ T_{BCKE}	EN inputs	2.9 / 0	-	3.2 / 0	-	ns
T_{BRCK}/ T_{BCKR}	RST input	2.7 / 0	-	2.9 / 0	-	ns
T_{BWCK}/ T_{BCKW}	WEN input	2.6 / 0	-	2.8 / 0	-	ns
Clock CLK						
T_{BPWH}	Minimum pulse width, High	-	1.9	-	1.9	ns
T_{BPWL}	Minimum pulse width, Low	-	1.9	-	1.9	ns
T_{BCCS}	CLKA -> CLKB setup time for different ports	-	3.0	-	4.0	ns

Notes:
1. A zero hold time listing indicates no hold time or a negative hold time.

TBUF Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
Combinatorial Delays				
T_{IO}	IN input to OUT output	0	0	ns
T_{OFF}	TRI input to OUT output high impedance	0.1	0.2	ns
T_{ON}	TRI input to valid data on OUT output	0.1	0.2	ns

JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Setup and Hold Times with Respect to TCK						
T_{TAPTCK} / T_{TCKTAP}	TMS and TDI setup and hold times	4.0 / 2.0	-	4.0 / 2.0	-	ns
Sequential Delays						
T_{TCKTDO}	Output delay from clock TCK to output TDO	-	11.0	-	11.0	ns
FTCK	Maximum TCK clock frequency	-	33	-	33	MHz

Revision History

Date	Version No.	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Updated timing to reflect the latest speed files. Added current supply numbers and XC2S200 -5 timing numbers. Approved -5 timing numbers as preliminary information with exceptions as noted.
11/02/00	2.1	Removed Power Down feature.
01/19/01	2.2	DC and timing numbers updated to Preliminary for the XC2S50 and XC2S100. Industrial power-on current specifications and -6 DLL timing numbers added. Power-on specification clarified.
03/09/01	2.3	Added note on power sequencing. Clarified power-on current requirement.
08/28/01	2.4	Added -6 preliminary timing. Added typical and industrial standby current numbers. Specified min. power-on current by junction temperature instead of by device type (Commercial vs. Industrial). Eliminated minimum V_{CCINT} ramp time requirement. Removed footnote limiting DLL operation to the Commercial temperature range.
07/26/02	2.5	Clarified that I/O leakage current is specified over the Recommended Operating Conditions for V_{CCINT} and V_{CCO}.
08/26/02	2.6	Added references for XAPP450 to Power-On Current Specification.
09/03/03	2.7	Added relaxed minimum power-on current (I_{CCPO}) requirements to page 53. On page 64, moved T_{RPW} values from maximum to minimum column.
06/13/08	2.8	Updated I/O measurement thresholds. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.

Introduction

This section describes how the various pins on a Spartan®-II FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-II FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-II FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-II FPGA packages, as outlined in Table 35.

Table 35: **Pin Definitions**

Pin Name	Dedicated	Direction	Description
GCK0, GCK1, GCK2, GCK3	No	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin. It is an input for slave-parallel and slave-serial modes, and output in master-serial mode.
$\overline{\text{PROGRAM}}$	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
$\overline{\text{INIT}}$	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. This pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{\text{WRITE}}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{\text{CS}}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	Power supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power supply pins for output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx® PCI cores. If the cores are not used, these pins are available as user I/Os.

XC2S50 Device Pinouts *(Continued)*

XC2S50 Pad Name					
Function	Bank	TQ144	PQ208	FG256	Bndry Scan
I/O	3	-	-	J14	503
I/O	3	P56	P127	K15	506
V_{CCINT}	-	P55	P128	V_{CCINT}*	-
I/O, TRDY(1)	3	P54	P129	J15	512
V_{CCO}	3	P53	P130	V_{CCO} Bank 3*	-
V_{CCO}	2	P53	P130	V_{CCO} Bank 2*	-
GND	-	P52	P131	GND*	-
I/O, IRDY(1)	2	P51	P132	H16	515
I/O	2	-	P133	H14	518
I/O	2	P50	P134	H15	521
I/O	2	-	-	J13	524
I/O (D3)	2	P49	P135	G16	527
I/O, V_{REF}	2	P48	P136	H13	530
GND	-	-	P137	GND*	-
I/O	2	-	P138	G14	533
I/O	2	-	P139	G15	536
I/O	2	-	P140	G12	539
I/O	2	-	-	F16	542
I/O	2	P47	P141	G13	545
I/O (D2)	2	P46	P142	F15	548
V_{CCINT}	-	-	P143	V_{CCINT}*	-
V_{CCO}	2	-	P144	V_{CCO} Bank 2*	-
GND	-	P45	P145	GND*	-
I/O (D1)	2	P44	P146	E16	551
I/O	2	P43	P147	F14	554
I/O	2	P42	P148	D16	557
I/O	2	-	-	F12	560
I/O	2	-	P149	E15	563
I/O, V_{REF}	2	P41	P150	F13	566
GND	-	-	-	GND*	-
I/O	2	-	P151	E14	569
I/O	2	-	-	C16	572
I/O	2	P40	P152	E13	575
I/O	2	-	-	B16	578
I/O (DIN, D0)	2	P39	P153	D14	581
I/O (DOUT, BUSY)	2	P38	P154	C15	584
CCLK	2	P37	P155	D15	587
V_{CCO}	2	P36	P156	V_{CCO} Bank 2*	-

XC2S50 Device Pinouts *(Continued)*

XC2S50 Pad Name					
Function	Bank	TQ144	PQ208	FG256	Bndry Scan
V_{CCO}	1	P35	P156	V_{CCO} Bank 1*	-
TDO	2	P34	P157	B14	-
GND	-	P33	P158	GND*	-
TDI	-	P32	P159	A15	-
I/O ($\overline{CS}$)	1	P31	P160	B13	0
I/O ($\overline{WRITE}$)	1	P30	P161	C13	3
I/O	1	-	-	C12	6
I/O	1	P29	P162	A14	9
I/O	1	-	-	D12	12
I/O	1	-	P163	B12	15
GND	-	-	-	GND*	-
I/O, V_{REF}	1	P28	P164	C11	18
I/O	1	-	P165	A13	21
I/O	1	-	-	D11	24
I/O	1	-	P166	A12	27
I/O	1	P27	P167	E11	30
I/O	1	P26	P168	B11	33
GND	-	P25	P169	GND*	-
V_{CCO}	1	-	P170	V_{CCO} Bank 1*	-
V_{CCINT}	-	P24	P171	V_{CCINT}*	-
I/O	1	P23	P172	A11	36
I/O	1	P22	P173	C10	39
I/O	1	-	P174	B10	45
I/O	1	-	P175	D10	48
I/O	1	-	P176	A10	51
GND	-	-	P177	GND*	-
I/O, V_{REF}	1	P21	P178	B9	54
I/O	1	-	P179	E10	57
I/O	1	-	-	A9	60
I/O	1	P20	P180	D9	63
I/O	1	P19	P181	A8	66
I, GCK2	1	P18	P182	C9	72
GND	-	P17	P183	GND*	-
V_{CCO}	1	P16	P184	V_{CCO} Bank 1*	-
V_{CCO}	0	P16	P184	V_{CCO} Bank 0*	-
I, GCK3	0	P15	P185	B8	73
V_{CCINT}	-	P14	P186	V_{CCINT}*	-
I/O	0	P13	P187	A7	80

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name						
Function	Bank	TQ144	PQ208	FG256	FG456	Bndry Scan
I/O	0	-	P188	A6	C10	107
I/O, V_{REF}	0	P12	P189	B7	A9	110
GND	-	-	P190	GND*	GND*	-
I/O	0	-	P191	C8	B9	113
I/O	0	-	P192	D7	E10	116
I/O	0	-	P193	E7	A8	122
I/O	0	-	-	-	D9	125
I/O	0	P11	P194	C7	E9	128
I/O	0	P10	P195	B6	A7	131
V_{CCINT}	-	P9	P196	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	0	-	P197	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
GND	-	P8	P198	GND*	GND*	-
I/O	0	P7	P199	A5	B7	134
I/O, V_{REF}	0	P6	P200	C6	E8	137
I/O	0	-	-	-	D8	140
I/O	0	-	P201	B5	C7	143
I/O	0	-	-	D6	D7	146
I/O	0	-	P202	A4	D6	152
I/O, V_{REF}	0	P5	P203	B4	C6	155
V_{CCO}	0	-	-	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
GND	-	-	-	GND*	GND*	-
I/O	0	-	P204	E6	B5	158
I/O	0	-	-	D5	E7	161
I/O	0	-	-	-	E6	164
I/O	0	P4	P205	A3	B4	167
I/O	0	-	-	C5	A3	170
I/O	0	P3	P206	B3	C5	176
TCK	-	P2	P207	C4	C4	-
V_{CCO}	0	P1	P208	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
V_{CCO}	7	P144	P208	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-

04/18/01

Notes:
1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S100 Package Pins

TQ144

Not Connected Pins					
P104	P105	-	-	-	-

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PQ208

Not Connected Pins					
P55	P56	-	-	-	-

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FG256

V_{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V_{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V_{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V_{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V_{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V_{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V_{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V_{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V_{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

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FG456

V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					

Additional XC2S100 Package Pins *(Continued)*

F10	F7	F8	F9	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U10	U7	U8	U9
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A4	A5	A6	A12	A13
A14	A15	A17	B3	B6	B8
B11	B14	B16	B19	C1	C2
C8	C9	C12	C18	C22	D1
D4	D5	D10	D18	D19	D21
E4	E11	E13	E15	E16	E17
E19	E22	F4	F11	F22	G2
G3	G4	G19	G22	H1	H21
J1	J3	J4	J19	J20	K2
K18	K19	L2	L5	L18	L19
M2	M6	M17	M18	M21	N1
N5	N19	P1	P5	P19	P22
R1	R3	R20	R22	T5	T19
U3	U11	U18	V1	V2	V10
V12	V17	V3	V4	V6	V8
V20	V21	V22	W4	W5	W9
W13	W14	W15	W16	W19	Y5
Y14	Y18	Y22	AA1	AA3	AA6
AA9	AA10	AA11	AA16	AA17	AA18
AA22	AB3	AB4	AB7	AB8	AB12
AB14	AB21	-	-	-	-

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XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name					
Function	Bank	PQ208	FG256	FG456	Bndry Scan
I/O	6	P46	P1	T4	404
I/O	6	-	L5	W1	407
I/O	6	-	-	V2	410
I/O	6	-	-	U4	413
I/O	6	P47	N2	Y1	416
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	419
I/O	6	-	-	V3	422
I/O	6	-	-	V4	425
I/O	6	P48	R1	Y2	428
I/O	6	P49	M3	W3	431
M1	-	P50	P2	U5	434
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	435
V_{CCO}	6	P53	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
V_{CCO}	5	P53	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
M2	-	P54	R3	Y4	436
I/O	5	-	-	W5	443
I/O	5	-	-	AB3	446
I/O	5	-	N5	V7	449
GND	-	-	GND*	GND*	-
I/O	5	P57	T2	Y6	452
I/O	5	-	-	AA4	455
I/O	5	-	-	AB4	458
I/O	5	-	P5	W6	461
I/O	5	P58	T3	Y7	464
GND	-	-	GND*	GND*	-
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P59	T4	AA5	467
I/O	5	P60	M6	AB5	470
I/O	5	-	-	V8	473
I/O	5	-	-	AA6	476
I/O	5	-	T5	AB6	479
I/O	5	P61	N6	AA7	482
I/O	5	-	-	W7	485
I/O, V_{REF}	5	P62	R5	W8	488
I/O	5	P63	P6	Y8	491
GND	-	P64	GND*	GND*	-

XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name					
Function	Bank	PQ208	FG256	FG456	Bndry Scan
V_{CCO}	5	P65	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCINT}	-	P66	V_{CCINT}*	V_{CCINT}*	-
I/O	5	P67	R6	AA8	494
I/O	5	P68	M7	V9	497
I/O	5	-	-	W9	503
I/O	5	-	-	AB9	506
I/O	5	P69	N7	Y9	509
I/O	5	-	-	V10	512
I/O	5	P70	T6	W10	518
I/O	5	P71	P7	AB10	521
GND	-	P72	GND*	GND*	-
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P73	P8	Y10	524
I/O	5	P74	R7	V11	527
I/O	5	-	T7	W11	530
I/O	5	P75	T8	AB11	533
I/O	5	-	-	U11	536
V_{CCINT}	-	P76	V_{CCINT}*	V_{CCINT}*	-
I, GCK1	5	P77	R8	Y11	545
V_{CCO}	5	P78	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCO}	4	P78	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-
I, GCK0	4	P80	N8	W12	546
I/O	4	P81	N9	U12	550
I/O	4	-	-	V12	553
I/O	4	P82	R9	Y12	556
I/O	4	-	N10	AA12	559
I/O	4	P83	T9	AB13	562
I/O, V_{REF}	4	P84	P9	AA13	565
V_{CCO}	4	-	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P85	GND*	GND*	-
I/O	4	P86	M10	Y13	568
I/O	4	P87	R10	V13	571
I/O	4	-	-	W14	577
I/O	4	P88	P10	AA14	580
I/O	4	-	-	V14	583
I/O	4	-	-	Y14	586
I/O	4	P89	T10	AB15	592

Additional XC2S200 Package Pins *(Continued)*

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FG456

V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					
F7	F8	F9	F10	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U7	U8	U9	U10
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					

Additional XC2S200 Package Pins *(Continued)*

G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A6	A12	B11	B16	C2
D1	D4	D18	D19	E17	E19
G2	G22	L2	L19	M2	M21
R3	R20	U3	U18	V6	W4
W19	Y5	Y22	AA1	AA3	AA11
AA16	AB7	AB12	AB21	-	-

11/02/00

Revision History

Version No.	Date	Description
2.0	09/18/00	Sectioned the Spartan-II Family data sheet into four modules. Corrected all known errors in the pinout tables.
2.1	10/04/00	Added notes requiring $\overline{PWDN}$ to be tied to V_{CCINT} when unused.
2.2	11/02/00	Removed the Power Down feature.
2.3	03/05/01	Added notes on pinout tables for IRDY and TRDY.
2.4	04/30/01	Reinstated XC2S50 V_{CCO} Bank 7, GND, and "not connected" pins missing in version 2.3.
2.5	09/03/03	Added caution about Not Connected Pins to XC2S30 pinout tables on page 76.
2.8	06/13/08	Added "Package Overview" section. Added notes to clarify shared V_{CCO} banks. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.