# E·XFL

#### AMD Xilinx - XC2S150-5FG256C Datasheet



Welcome to <u>E-XFL.COM</u>

#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	176
Number of Gates	150000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s150-5fg256c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# 

DS001-1 (v2.8) June 13, 2008

# Spartan-II FPGA Family: Introduction and Ordering Information

#### **Product Specification**

# Introduction

The Spartan<sup>®</sup>-II Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The six-member family offers densities ranging from 15,000 to 200,000 system gates, as shown in Table 1. System performance is supported up to 200 MHz. Features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards, and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-II family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

# **Features**

- Second generation ASIC replacement technology
  - Densities as high as 5,292 logic cells with up to 200,000 system gates
  - Streamlined features based on Virtex<sup>®</sup> FPGA architecture
  - Unlimited reprogrammability
  - Very low cost
  - Cost-effective 0.18 micron process

- System level features
  - SelectRAM<sup>™</sup> hierarchical memory:
    - · 16 bits/LUT distributed RAM
    - Configurable 4K bit block RAM
    - Fast interfaces to external RAM
  - Fully PCI compliant
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 16 high-performance interface standards
  - Hot swap Compact PCI friendly
  - Zero hold time simplifies system timing
- Core logic powered at 2.5V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx<sup>®</sup> ISE<sup>®</sup> development system
  - Fully automatic mapping, placement, and routing

Table 1: Spa	rtan-II FPG	A Family Members					
Device	Logic Cells	System Gates (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O <sup>(1)</sup>	Total Distributed RAM Bits	Total Block RAM Bits
XC2S15	432	15,000	8 x 12	96	86	6,144	16K
XC2S30	972	30,000	12 x 18	216	92	13,824	24K
XC2S50	1,728	50,000	16 x 24	384	176	24,576	32K
XC2S100	2,700	100,000	20 x 30	600	176	38,400	40K
XC2S150	3,888	150,000	24 x 36	864	260	55,296	48K
XC2S200	5,292	200,000	28 x 42	1,176	284	75,264	56K

#### Notes:

1. All user I/O counts do not include the four global clock/user input pins. See details in Table 2, page 4.

© 2000-2008 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, the Brand Window, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate  $V_{REF}$  voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

#### I/O Banking

Some of the I/O standards described above require  $V_{CCO}$  and/or  $V_{REF}$  voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3). Each bank has multiple  $V_{CCO}$  pins which must be connected to the same voltage. Voltage is determined by the output standards in use.



DS001\_03\_060100

Figure 3: Spartan-II I/O Banks

Within a bank, output standards may be mixed only if they use the same  $V_{CCO}$ . Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on  $V_{CCO}$ .

#### Table 4: Compatible Output Standards

V <sub>cco</sub>	Compatible Standards
3.3V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage,  $V_{\text{REF}}$  In this case, certain user-I/O pins are

automatically configured as inputs for the V<sub>REF</sub> voltage. About one in six of the I/O pins in the bank assume this role.

 $V_{\text{REF}}$  pins within a bank are interconnected internally and consequently only one  $V_{\text{REF}}$  voltage can be used within each bank. All  $V_{\text{REF}}$  pins in the bank, however, must be connected to the external voltage source for correct operation.

In a bank, inputs requiring V<sub>REF</sub> can be mixed with those that do not but only one V<sub>REF</sub> voltage may be used within a bank. Input buffers that use V<sub>REF</sub> are not 5V tolerant. LVTTL, LVCMOS2, and PCI are 5V tolerant. The V<sub>CCO</sub> and V<sub>REF</sub> pins for each bank appear in the device pinout tables.

Within a given package, the number of V<sub>REF</sub> and V<sub>CCO</sub> pins can vary depending on the size of device. In larger devices, more I/O pins convert to V<sub>REF</sub> pins. Since these are always a superset of the V<sub>REF</sub> pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device. All V<sub>REF</sub> pins for the largest device anticipated must be connected to the V<sub>REF</sub> voltage, and not used for I/O.

Independent Banks Available

Package	VQ100	CS144	FG256
	PQ208	TQ144	FG456
Independent Banks	1	4	8

### **Configurable Logic Block**

The basic building block of the Spartan-II FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. Output from the function generator in each LC drives the CLB output and the D input of the flip-flop. Each Spartan-II FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 4.

In addition to the four basic LCs, the Spartan-II FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

#### Look-Up Tables

Spartan-II FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-II FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.



Figure 4: Spartan-II CLB Slice (two identical slices in each CLB)

#### Storage Elements

Storage elements in the Spartan-II FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

#### Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.



#### Notes: (referring to waveform above:)

1. Before configuration can begin,  $V_{CCINT}$  must be greater than 1.6V and  $V_{CCO}$  Bank 2 must be greater than 1.0V.

Figure 12: Configuration Timing on Power-Up

#### **Clearing Configuration Memory**

The device indicates that clearing the configuration memory is in progress by driving INIT Low. At this time, the user can delay configuration by holding either PROGRAM or INIT Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional INIT line is driving a Low logic level during memory clearing. To avoid contention, use an open-drain driver to keep INIT Low.

With no delay in force, the device indicates that the memory is completely clear by driving INIT High. The FPGA samples its mode pins on this Low-to-High transition.

#### Loading Configuration Data

Once INIT is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 14. Loading data using the Slave Parallel mode is shown in Figure 19, page 25.

#### **CRC Error Checking**

During the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives INIT Low to indicate that a frame error has occurred and configuration is aborted.

To reconfigure the device, the PROGRAM pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See "Clearing Configuration Memory".

#### Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

During start-up, the device performs four operations:

- 1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
- 2. The release of the Global Three State net. This activates I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-down resistors present.
- 3. Negates Global Set Reset (GSR). This allows all flip-flops to change state.
- 4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

#### Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK. Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is 2<sup>20</sup>-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until INIT pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.



DS001\_15\_060608

#### Notes:

1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a  $330\Omega$  resistor.

#### Figure 15: Master/Slave Serial Configuration Circuit Diagram

division factor N except for non-integer division in High Frequency (HF) mode. For division factor 1.5 the duty cycle in the HF mode is 33.3% High and 66.7% Low. For division factor 2.5, the duty cycle in the HF mode is 40.0% High and 60.0% Low.

#### 1x Clock Outputs — CLK[0/90/180/270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 degree phase-shifted version. The relationship between phase shift and the corresponding period shift appears in Table 10.

The timing diagrams in Figure 26 illustrate the DLL clock output characteristics.

# Table 10: Relationship of Phase-Shifted Output Clock to Period Shift

Phase (degrees)	Period Shift (percent)
0	0%
90	25%
180	50%
270	75%

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY\_CYCLE\_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY\_CYCLE\_CORRECTION=FALSE property to the DLL primitive. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

#### Locked Output — LOCKED

In order to achieve lock, the DLL may need to sample several thousand clock cycles. After the DLL achieves lock the LOCKED signal activates. The "DLL Timing Parameters" section of Module 3 provides estimates for locking times.

In order to guarantee that the system clock is established prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP\_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other

spurious movement. In particular the CLK2X output will appear as a 1x clock with a 25/75 duty cycle.

#### **DLL Properties**

Properties provide access to some of the Spartan-II family DLL features, (for example, clock division and duty cycle correction).

#### **Duty Cycle Correction Property**

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, such that they exhibit a 50/50 duty cycle. The DUTY\_CYCLE\_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY\_CYCLE\_CORRECTION=FALSE property to the DLL primitive.



Figure 26: DLL Output Characteristics

#### Clock Divide Property

The CLKDV\_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

#### Startup Delay Property

This property, STARTUP\_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the Startup Sequence following device configuration is paused at a user-specified point until the DLL locks. <u>XAPP176</u>: *Configuration and Readback of the Spartan-II and Spartan-IIE Families* explains how this can result in delaying the assertion of the DONE pin until the DLL locks.

#### **DLL Location Constraints**

The DLLs are distributed such that there is one DLL in each corner of the device. The location constraint LOC, attached to the DLL primitive with the numeric identifier 0, 1, 2, or 3, controls DLL location. The orientation of the four DLLs and their corresponding clock resources appears in Figure 27.

The LOC property uses the following form.

LOC = DLL2



Figure 27: Orientation of DLLs

#### **Design Considerations**

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

#### Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the "DLL Timing Parameters" section of the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

#### Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock in a way that has little impact to the DLL. Stopping the clock should be limited to less than approximately 100  $\mu$ s to keep device cooling to a minimum and maintain the validity of the current tap setting. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED will stay High and remain High when the clock is restored. If these conditions may not be met in the design, apply a manual reset to the DLL after re-starting the input clock, even if the LOCKED signal has not changed.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

#### **Output Clocks**

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). One DLL output can drive more than one OBUF; however, this adds skew.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

#### **Useful Application Examples**

The Spartan-II FPGA DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications.

#### Standard Usage

The circuit shown in Figure 28 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.



DS001\_28\_061200

Figure 28: Standard DLL Implementation

#### Deskew of Clock and Its 2x Multiple

The circuit shown in Figure 29 implements a 2x clock multiplier and also uses the CLK0 clock output with zero ns skew between registers on the same chip. A clock divider circuit could alternatively be implemented using similar connections.



DS001\_29\_061200

Figure 29: DLL Deskew of Clock and 2x Multiple

Because any single DLL can only access at most two BUFGs, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

#### Generating a 4x Clock

By connecting two DLL circuits each implementing a 2x clock multiplier in series as shown in Figure 30, a 4x clock multiply can be implemented with zero skew between registers in the same device.

If other clock output is needed, the clock could access a BUFG only if the DLLs are constrained to exist on opposite edges (Top or Bottom) of the device.



DS001\_30\_061200

Figure 30: DLL Generation of 4x Clock

When using this circuit it is vital to use the SRL16 cell to reset the second DLL after the initial chip reset. If this is not done, the second DLL may not recognize the change of frequencies from when the input changes from a 1x (25/75) waveform to a 2x (50/50) waveform. It is not recommended to cascade more than two DLLs.

For design examples and more information on using the DLL, see <u>XAPP174</u>, Using Delay-Locked Loops in Spartan-II FPGAs.



Figure 33: Timing Diagram for Single-Port Block RAM Memory



Figure 34: Timing Diagram for a True Dual-Port Read/Write Block RAM Memory

# XILINX<sup>®</sup>

#### GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 42. Table 20 lists DC voltage specifications for the GTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.





Figure 42: Terminated GTL

#### Table 20: GTL Voltage Specifications

Parameter	Min	Тур	Max
V <sub>CCO</sub>	-	N/A	-
$V_{REF} = N \times V_{TT}^{(1)}$	0.74	0.8	0.86
V <sub>TT</sub>	1.14	1.2	1.26
$V_{IH} \ge V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} \leq V_{REF} - 0.05$	-	0.75	0.81
V <sub>OH</sub>	-	-	-
V <sub>OL</sub>	-	0.2	0.4
I <sub>OH</sub> at V <sub>OH</sub> (mA)	-	-	-
I <sub>OL</sub> at V <sub>OL</sub> (mA) at 0.4V	32	-	-
$I_{OL}$ at $V_{OL}$ (mA) at 0.2V	-	-	40

#### Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

#### GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 43. DC voltage specifications appear in Table 21 for the GTL+ standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.



Figure 43: Terminated GTL+

#### Table 21: GTL+ Voltage Specifications

Parameter	Min	Тур	Max
V <sub>CCO</sub>	-	-	-
$V_{REF} = N \times V_{TT}^{(1)}$	0.88	1.0	1.12
V <sub>TT</sub>	1.35	1.5	1.65
$V_{IH} \ge V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} \le V_{REF} - 0.1$	-	0.9	1.02
V <sub>OH</sub>	-	-	-
V <sub>OL</sub>	0.3	0.45	0.6
I <sub>OH</sub> at V <sub>OH</sub> (mA)	-	-	-
I <sub>OL</sub> at V <sub>OL</sub> (mA) at 0.6V	36	-	-
I <sub>OL</sub> at V <sub>OL</sub> (mA) at 0.3V	-	-	48

#### Notes:

#### HSTL Class I

A sample circuit illustrating a valid termination technique for HSTL\_I appears in Figure 44. DC voltage specifications appear in Table 22 for the HSTL\_1 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.



DS001\_44\_061.

Figure 44: Terminated HSTL Class I

#### Table 22: HSTL Class I Voltage Specification

Parameter	Min	Тур	Max
V <sub>CCO</sub>	1.40	1.50	1.60
V <sub>REF</sub>	0.68	0.75	0.90
V <sub>TT</sub>	-	$V_{CCO}  imes 0.5$	-
V <sub>IH</sub>	V <sub>REF</sub> + 0.1	-	-
V <sub>IL</sub>	-	-	$V_{REF} - 0.1$
V <sub>OH</sub>	$V_{CCO} - 0.4$	-	-
V <sub>OL</sub>			0.4
I <sub>OH</sub> at V <sub>OH</sub> (mA)	-8	-	-
I <sub>OL</sub> at V <sub>OL</sub> (mA)	8	-	-

<sup>1.</sup> N must be greater than or equal to 0.653 and less than or equal to 0.68.



# Spartan-II FPGA Family: DC and Switching Characteristics

DS001-3 (v2.8) June 13, 2008

**Product Specification** 

### **Definition of Terms**

In this document, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All limits are representative of worst-case supply voltage and junction temperature conditions. Typical numbers are based on measurements taken at a nominal  $V_{CCINT}$  level of 2.5V and a junction temperature of 25°C. The parameters included are common to popular designs and typical applications. All specifications are subject to change without notice.

### **DC Specifications**

#### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Description		Min	Max	Units
V <sub>CCINT</sub>	Supply voltage relative to GND <sup>(2)</sup>		-0.5	3.0	V
V <sub>CCO</sub>	Supply voltage relative to GND <sup>(2)</sup>		-0.5	4.0	V
V <sub>REF</sub>	Input reference voltage		-0.5	3.6	V
V <sub>IN</sub>	Input voltage relative to GND <sup>(3)</sup>	5V tolerant I/O <sup>(4)</sup>	-0.5	5.5	V
		No 5V tolerance <sup>(5)</sup>	-0.5	V <sub>CCO</sub> +0.5	V
V <sub>TS</sub>	Voltage applied to 3-state output	state output 5V tolerant I/O <sup>(4)</sup>		5.5	V
		No 5V tolerance <sup>(5)</sup>	-0.5	V <sub>CCO</sub> +0.5	V
T <sub>STG</sub>	Storage temperature (ambient)		-65	+150	°C
TJ	Junction temperature		-	+125	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

2. Power supplies may turn on in any order.

3. V<sub>IN</sub> should not exceed V<sub>CCO</sub> by more than 3.6V over extended periods of time (e.g., longer than a day).

4. Spartan<sup>®</sup>-II device I/Os are 5V Tolerant whenever the LVTTL, LVCMOS2, or PCI33\_5 signal standard has been selected. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA, and undershoot must be limited to either -0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to -2.0V or overshoot to +7.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

5. Without 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either V<sub>CCO</sub> + 0.5V or 10 mA, and undershoot must be limited to -0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to -2.0V or overshoot to V<sub>CCO</sub> + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

6. For soldering guidelines, see the <u>Packaging Information</u> on the Xilinx<sup>®</sup> web site.

© 2000-2008 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, the Brand Window, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

#### **IOB Output Switching Characteristics**

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59.

		Speed Grade				
		-6		-5		
Symbol	Description	Min	Max	Min	Max	Units
Propagation Delays	5					
T <sub>IOOP</sub>	O input to pad	-	2.9	-	3.4	ns
T <sub>IOOLP</sub>	O input to pad via transparent latch	-	3.4	-	4.0	ns
3-state Delays		1				
T <sub>IOTHZ</sub>	T input to pad high-impedance <sup>(1)</sup>	-	2.0	-	2.3	ns
T <sub>IOTON</sub>	T input to valid data on pad	-	3.0	-	3.6	ns
T <sub>IOTLPHZ</sub>	T input to pad high impedance via transparent latch <sup>(1)</sup>	-	2.5	-	2.9	ns
T <sub>IOTLPON</sub>	T input to valid data on pad via transparent latch	-	3.5	-	4.2	ns
T <sub>GTS</sub>	GTS to pad high impedance <sup>(1)</sup>	-	5.0	-	5.9	ns
Sequential Delays		1	I	1		
T <sub>IOCKP</sub>	Clock CLK to pad	-	2.9	-	3.4	ns
Т <sub>ЮСКНZ</sub>	Clock CLK to pad high impedance (synchronous) <sup>(1)</sup>	-	2.3	-	2.7	ns
T <sub>IOCKON</sub>	Clock CLK to valid data on pad (synchronous)	-	3.3	-	4.0	ns
Setup/Hold Times	with Respect to Clock CLK <sup>(2)</sup>	1	l.			
TIOOCK / TIOCKO	O input	1.1/0	-	1.3/0	-	ns
T <sub>IOOCECK</sub> /	OCE input	0.9 / 0.01	-	0.9/0.01	-	ns
TIOCKOCE						
T <sub>IOSRCKO</sub> /	SR input (OFF)	1.2/0	-	1.3 / 0	-	ns
TIOCKOSR				/ -		
TIOTCK / TIOCKT	3-state setup times, T input	0.8/0	-	0.9/0	-	ns
Т <sub>ІОТСЕСК</sub> /	3-state setup times, TCE input	1.0/0	-	1.0/0	-	ns
		11/0		10/0		
	3-state setup times, SK input (TFF)	1.170	-	1.2/0	-	ns
Set/Reset Delays						
	SR input to pad (asynchronous)	_	37	_	44	ns
	SR input to pad high impedance (asynchronous) <sup>(1)</sup>	-	3.1	-	37	ns
	SR input to valid data on pad (asynchronous)	-	4 1	-	4 Q	ns
	GSR to pad	_	9.1	_	11 7	ns
' IOGSRQ	OUN ID Pau	-	9.9	-	11.7	115

Notes:

1. Three-state turn-off delays should not be adjusted.

2. A zero hold time listing indicates no hold time or a negative hold time.

# Calculation of T<sub>IOOP</sub> as a Function of Capacitance

 $T_{\rm IOOP}$  is the propagation delay from the O Input of the IOB to the pad. The values for  $T_{\rm IOOP}$  are based on the standard capacitive load (C<sub>SL</sub>) for each I/O standard as listed in the table "Constants for Calculating TIOOP", below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay,  $T_{IOOP1}$ .

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_{L}$$

Where:

Adj is selected from "IOB Output Delay Adjustments for Different Standards", page 59, according to the I/O standard used

 $C_{\text{LOAD}}\,$  is the capacitive load for the design

F<sub>L</sub> is the capacitance scaling factor

#### **Delay Measurement Methodology**

Standard	V <sub>L</sub> (1)	V <sub>H</sub> (1)	Meas. Point	V <sub>REF</sub> Typ <sup>(2)</sup>
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_5	Pe	r PCI Spec		-
PCI33_3	Pe	r PCI Spec		-
PCI66_3	Pe	r PCI Spec		-
GTL	V <sub>REF</sub> – 0.2	V <sub>REF</sub> + 0.2	$V_{REF}$	0.80
GTL+	V <sub>REF</sub> – 0.2	V <sub>REF</sub> + 0.2	$V_{REF}$	1.0
HSTL Class I	V <sub>REF</sub> – 0.5	V <sub>REF</sub> + 0.5	$V_{REF}$	0.75
HSTL Class III	V <sub>REF</sub> – 0.5	V <sub>REF</sub> + 0.5	$V_{REF}$	0.90
HSTL Class IV	V <sub>REF</sub> – 0.5	V <sub>REF</sub> + 0.5	$V_{REF}$	0.90
SSTL3 I and II	V <sub>REF</sub> – 1.0	V <sub>REF</sub> + 1.0	$V_{REF}$	1.5
SSTL2 I and II	$V_{REF} - 0.75$	V <sub>REF</sub> + 0.75	$V_{REF}$	1.25
CTT	V <sub>REF</sub> – 0.2	V <sub>REF</sub> + 0.2	$V_{REF}$	1.5
AGP	V <sub>REF</sub> – (0.2xV <sub>CCO</sub> )	V <sub>REF</sub> + (0.2xV <sub>CCO</sub> )	V <sub>REF</sub>	Per AGP Spec

#### Notes:

- 1. Input waveform switches between V<sub>L</sub> and V<sub>H</sub>.
- 2. Measurements are made at V<sub>REF</sub> Typ, Maximum, and Minimum. Worst-case values are reported.
- I/O parameter measurements are made with the capacitance values shown in the table, "Constants for Calculating TIOOP". See Xilinx application note <u>XAPP179</u> for the appropriate terminations.
- 4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

#### Constants for Calculating T<sub>IOOP</sub>

Standard	C <sub>SL</sub> <sup>(1)</sup> (pF)	F <sub>L</sub> (ns/pF)
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.044
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.100
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.050
LVTTL Slow Slew Rate, 24 mA drive	35	0.048
LVCMOS2	35	0.041
PCI 33 MHz 5V	50	0.050
PCI 33 MHZ 3.3V	10	0.050
PCI 66 MHz 3.3V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
СТТ	20	0.035
AGP	10	0.037

#### Notes:

- 1. I/O parameter measurements are made with the capacitance values shown above. See Xilinx application note <u>XAPP179</u> for the appropriate terminations.
- 2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.



DS001-4 (v2.8) June 13, 2008

# Spartan-II FPGA Family: Pinout Tables

**Product Specification** 

# Introduction

This section describes how the various pins on a Spartan<sup>®</sup>-II FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-II FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a "G" to the middle of the package code. Except for the thermal characteristics, all

information for the standard package applies equally to the Pb-free package.

# **Pin Types**

Most pins on a Spartan-II FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-II FPGA packages, as outlined in Table 35.

#### Table 35: Pin Definitions

Pin Name	Dedicated	Direction	Description
GCK0, GCK1, GCK2, GCK3	No	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin. It is an input for slave-parallel and slave-serial modes, and output in master-serial mode.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. This pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
			In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained.
			In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
<u>CS</u>	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V <sub>CCINT</sub>	Yes	Input	Power supply pins for the internal core logic.
V <sub>CCO</sub>	Yes	Input	Power supply pins for output drivers (subject to banking rules)
V <sub>REF</sub>	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx <sup>®</sup> PCI cores. If the cores are not used, these pins are available as user I/Os.

© 2000-2008 Xilinx, Inc. All rights reserved. XILINX, the Xilinx logo, the Brand Window, and other designated brands included herein are trademarks of Xilinx, Inc. All other trademarks are the property of their respective owners.

www.xilinx.com

Package	Leads	Туре	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass <sup>(1)</sup> (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	60	0.5	16 x 16	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	92	0.5	22 x 22	1.60	1.4
CS144 / CSG144	144	Chip Scale Ball Grid Array (CSBGA)	92	0.8	12 x 12	1.20	0.3
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	140	0.5	30.6 x 30.6	3.70	5.3
FG256 / FGG256	256	Fine-pitch Ball Grid Array (FBGA)	176	1.0	17 x 17	2.00	0.9
FG456 / FGG456	456	Fine-pitch Ball Grid Array (FBGA)	284	1.0	23 x 23	2.60	2.2

#### Table 36: Spartan-II Family Package Options

#### Notes:

1. Package mass is  $\pm 10\%$ .

Note: Some early versions of Spartan-II devices, including the XC2S15 and XC2S30 ES devices and the XC2S150 with date code 0045 or earlier, included a power-down pin. For more information, see <u>Answer Record 10500</u>.

# VCCO Banks

Some of the I/O standards require specific V<sub>CCO</sub> voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3 in Module 2). Each bank has multiple V<sub>CCO</sub> pins which must be connected to the same voltage. In the smaller packages, the V<sub>CCO</sub> pins are connected between banks, effectively reducing the number of independent banks available (see Table 37). These interconnected banks are shown in the Pinout Tables with V<sub>CCO</sub> pads for multiple banks connected to the same pin.

#### Table 37: Independent VCCO Banks Available

Package	VQ100	CS144	FG256	
	PQ208	TQ144	FG456	
Independent Banks	1	4	8	

### Package Overview

Table 36 shows the six low-cost, space-saving productionpackage styles for the Spartan-II family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS144" package becomes "CSG144" when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 38. For additional package information, see <u>UG112</u>: *Device Package User Guide*.

#### **Mechanical Drawings**

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 38.

Material Declaration Data Sheets (MDDS) are also available on the <u>Xilinx web site</u> for each package.

#### Table 38: Xilinx Package Documentation

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
CS144	Package Drawing	PK149_CS144
CSG144		PK103_CSG144
PQ208	Package Drawing	PK166_PQ208
PQG208		PK123_PQG208
FG256	Package Drawing	PK151_FG256
FGG256		PK105_FGG256
FG456	Package Drawing	PK154_FG456
FGG456		PK109_FGG456

#### XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name					Bndry
Function	Bank	TQ144	PQ208	FG256	Scan
I/O	5	P99	P63	P6	326
GND	-	P98	P64	GND*	-
V <sub>CCO</sub>	5	-	P65	V <sub>CCO</sub> Bank 5*	-
V <sub>CCINT</sub>	-	P97	P66	V <sub>CCINT</sub> *	-
I/O	5	P96	P67	R6	329
I/O	5	P95	P68	M7	332
I/O	5	-	P69	N7	338
I/O	5	-	P70	T6	341
I/O	5	-	P71	P7	344
GND	-	-	P72	GND*	-
I/O, V <sub>REF</sub>	5	P94	P73	P8	347
I/O	5	-	P74	R7	350
I/O	5	-	-	T7	353
I/O	5	P93	P75	T8	356
V <sub>CCINT</sub>	-	P92	P76	V <sub>CCINT</sub> *	-
I, GCK1	5	P91	P77	R8	365
V <sub>CCO</sub>	5	P90	P78	V <sub>CCO</sub> Bank 5*	-
V <sub>CCO</sub>	4	P90	P78	V <sub>CCO</sub> Bank 4*	-
GND	-	P89	P79	GND*	-
I, GCK0	4	P88	P80	N8	366
I/O	4	P87	P81	N9	370
I/O	4	P86	P82	R9	373
I/O	4	-	-	N10	376
I/O	4	-	P83	Т9	379
I/O, V <sub>REF</sub>	4	P85	P84	P9	382
GND	-	-	P85	GND*	-
I/O	4	-	P86	M10	385
I/O	4	-	P87	R10	388
I/O	4	-	P88	P10	391
I/O	4	P84	P89	T10	397
I/O	4	P83	P90	R11	400
V <sub>CCINT</sub>	-	P82	P91	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	4	-	P92	V <sub>CCO</sub> Bank 4*	-
GND	-	P81	P93	GND*	-
I/O	4	P80	P94	M11	403
I/O	4	P79	P95	T11	406
I/O	4	P78	P96	N11	409
I/O	4	-	-	R12	412

#### XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name					Bndry
Function	Bank	TQ144	PQ208	FG256	Scan
I/O	4	-	P97	P11	415
I/O, V <sub>REF</sub>	4	P77	P98	T12	418
GND	-	-	-	GND*	-
I/O	4	-	P99	T13	421
I/O	4	-	-	N12	424
I/O	4	P76	P100	R13	427
I/O	4	-	-	P12	430
I/O	4	P75	P101	P13	433
I/O	4	P74	P102	T14	436
GND	-	P73	P103	GND*	-
DONE	3	P72	P104	R14	439
V <sub>CCO</sub>	4	P71	P105	V <sub>CCO</sub> Bank 4*	-
V <sub>CCO</sub>	3	P70	P105	V <sub>CCO</sub> Bank 3*	-
PROGRAM	-	P69	P106	P15	442
I/O (INIT)	3	P68	P107	N15	443
I/O (D7)	3	P67	P108	N14	446
I/O	3	-	-	T15	449
I/O	3	P66	P109	M13	452
I/O	3	-	-	R16	455
I/O	3	-	P110	M14	458
GND	-	-	-	GND*	-
I/O, V <sub>REF</sub>	3	P65	P111	L14	461
I/O	3	-	P112	M15	464
I/O	3	-	-	L12	467
I/O	3	P64	P113	P16	470
I/O	3	P63	P114	L13	473
I/O (D6)	3	P62	P115	N16	476
GND	-	P61	P116	GND*	-
V <sub>CCO</sub>	3	-	P117	V <sub>CCO</sub> Bank 3*	-
V <sub>CCINT</sub>	-	-	P118	V <sub>CCINT</sub> *	-
I/O (D5)	3	P60	P119	M16	479
I/O	3	P59	P120	K14	482
I/O	3	-	-	L16	485
I/O	3	-	P121	K13	488
I/O	3	-	P122	L15	491
I/O	3	-	P123	K12	494
GND	-	-	P124	GND*	-
I/O, V <sub>REF</sub>	3	P58	P125	K16	497
I/O (D4)	3	P57	P126	J16	500

#### **XC2S150 Device Pinouts**

XC2S150 Pad	Name				Bndry
Function	Bank	PQ208	FG256	FG456	Scan
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	221
I/O	7	-	-	E4	224
I/O	7	-	-	C1	227
I/O	7	-	A2	F5	230
GND	-	-	GND*	GND*	-
I/O	7	P4	B1	D2	233
I/O	7	-	-	E3	236
I/O	7	-	-	F4	239
I/O	7	-	E3	G5	242
I/O	7	P5	D2	F3	245
GND	-	-	GND*	GND*	-
V <sub>CCO</sub>	7	-	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
I/O, V <sub>REF</sub>	7	P6	C1	E2	248
I/O	7	P7	F3	E1	251
I/O	7	-	-	G4	254
I/O	7	-	-	G3	257
I/O	7	-	E2	H5	260
I/O	7	P8	E4	F2	263
I/O	7	-	-	F1	266
I/O, V <sub>REF</sub>	7	P9	D1	H4	269
I/O	7	P10	E1	G1	272
GND	-	P11	GND*	GND*	-
V <sub>CCO</sub>	7	P12	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
V <sub>CCINT</sub>	-	P13	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	7	P14	F2	H3	275
I/O	7	P15	G3	H2	278
I/O	7	-	-	H1	284
I/O	7	-	F1	J5	287
I/O	7	P16	F4	J2	290
I/O	7	-	-	J3	293
I/O	7	P17	F5	K5	299
I/O	7	P18	G2	K1	302
GND	-	P19	GND*	GND*	-
V <sub>CCO</sub>	7	-	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
I/O, V <sub>REF</sub>	7	P20	H3	K3	305
I/O	7	P21	G4	K4	308
I/O	7	-	H2	L6	311

# XC2S150 Device Pinouts (Continued)

XC2S150 Pad	Name				Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O	7	P22	G5	L1	314
I/O	7	-	-	L5	317
I/O	7	P23	H4	L4	320
I/O, IRDY <sup>(1)</sup>	7	P24	G1	L3	323
GND	-	P25	GND*	GND*	-
V <sub>CCO</sub>	7	P26	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
V <sub>CCO</sub>	6	P26	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
I/O, TRDY <sup>(1)</sup>	6	P27	J2	M1	326
V <sub>CCINT</sub>	-	P28	$V_{CCINT}^{*}$	$V_{CCINT}^{*}$	-
I/O	6	-	-	M6	332
I/O	6	P29	H1	M3	335
I/O	6	-	J4	M4	338
I/O	6	P30	J1	M5	341
I/O, V <sub>REF</sub>	6	P31	J3	N2	344
V <sub>CCO</sub>	6	-	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	347
I/O	6	P34	K2	N4	350
I/O	6	-	-	N5	356
I/O	6	P35	K1	P2	359
I/O	6	-	K3	P4	362
I/O	6	-	-	R1	365
I/O	6	P36	L1	P3	371
I/O	6	P37	L2	R2	374
V <sub>CCINT</sub>	-	P38	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	6	P39	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	377
I/O, V <sub>REF</sub>	6	P42	M1	R4	380
I/O	6	-	-	T2	383
I/O	6	P43	L4	U1	386
I/O	6	-	M2	R5	389
I/O	6	-	-	V1	392
I/O	6	-	-	T5	395
I/O	6	P44	L3	U2	398
I/O, V <sub>REF</sub>	6	P45	N1	Т3	401
V <sub>CCO</sub>	6	-	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	-	GND*	GND*	-

#### **XC2S200** Device Pinouts

XC2S200 Pad	Name				Bndry
Function	Bank	PQ208	FG256	FG456	Scan
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	257
I/O	7	-	-	E4	263
I/O	7	-	-	C1	266
I/O	7	-	A2	F5	269
GND	-	-	GND*	GND*	-
I/O, V <sub>REF</sub>	7	P4	B1	D2	272
I/O	7	-	-	E3	275
I/O	7	-	-	F4	281
GND	-	-	GND*	GND*	-
I/O	7	-	E3	G5	284
I/O	7	P5	D2	F3	287
GND	-	-	GND*	GND*	-
V <sub>CCO</sub>	7	-	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
I/O, V <sub>REF</sub>	7	P6	C1	E2	290
I/O	7	P7	F3	E1	293
I/O	7	-	-	G4	296
I/O	7	-	-	G3	299
I/O	7	-	E2	H5	302
GND	-	-	GND*	GND*	-
I/O	7	P8	E4	F2	305
I/O	7	-	-	F1	308
I/O, V <sub>REF</sub>	7	P9	D1	H4	314
I/O	7	P10	E1	G1	317
GND	-	P11	GND*	GND*	-
V <sub>CCO</sub>	7	P12	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
V <sub>CCINT</sub>	-	P13	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	7	P14	F2	H3	320
I/O	7	P15	G3	H2	323
I/O	7	-	-	J4	326
I/O	7	-	-	H1	329
I/O	7	-	F1	J5	332
GND	-	-	GND*	GND*	-
I/O	7	P16	F4	J2	335
I/O	7	-	-	J3	338
I/O	7	-	-	J1	341
I/O	7	P17	F5	K5	344
I/O	7	P18	G2	K1	347
GND	-	P19	GND*	GND*	-

#### XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
V <sub>CCO</sub>	7	-	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
I/O, V <sub>REF</sub>	7	P20	H3	K3	350
I/O	7	P21	G4	K4	353
I/O	7	-	-	K2	359
I/O	7	-	H2	L6	362
I/O	7	P22	G5	L1	365
I/O	7	-	-	L5	368
I/O	7	P23	H4	L4	374
I/O, IRDY <sup>(1)</sup>	7	P24	G1	L3	377
GND	-	P25	GND*	GND*	-
V <sub>CCO</sub>	7	P26	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
V <sub>CCO</sub>	6	P26	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
I/O, TRDY <sup>(1)</sup>	6	P27	J2	M1	380
V <sub>CCINT</sub>	-	P28	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	6	-	-	M6	389
I/O	6	P29	H1	M3	392
I/O	6	-	J4	M4	395
I/O	6	-	-	N1	398
I/O	6	P30	J1	M5	404
I/O, V <sub>REF</sub>	6	P31	J3	N2	407
V <sub>CCO</sub>	6	-	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	410
I/O	6	P34	K2	N4	413
I/O	6	-	-	P1	416
I/O	6	-	-	N5	419
I/O	6	P35	K1	P2	422
GND	-	-	GND*	GND*	-
I/O	6	-	K3	P4	425
I/O	6	-	-	R1	428
I/O	6	-	-	P5	431
I/O	6	P36	L1	P3	434
I/O	6	P37	L2	R2	437
V <sub>CCINT</sub>	-	P38	$V_{CCINT}^{*}$	$V_{CCINT}^{*}$	-
V <sub>CCO</sub>	6	P39	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	440
I/O, V <sub>REF</sub>	6	P42	M1	R4	443

#### XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
V <sub>CCO</sub>	1	P156	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
TDO	2	P157	B14	A21	-
GND	-	P158	GND*	GND*	-
TDI	-	P159	A15	B20	-
I/O ( <u>CS</u> )	1	P160	B13	C19	0
I/O (WRITE)	1	P161	C13	A20	3
I/O	1	-	-	B19	9
I/O	1	-	-	C18	12
I/O	1	-	C12	D17	15
GND	-	-	GND*	GND*	-
I/O, V <sub>REF</sub>	1	P162	A14	A19	18
I/O	1	-	-	B18	21
I/O	1	-	-	E16	27
I/O	1	-	D12	C17	30
I/O	1	P163	B12	D16	33
GND	-	-	GND*	GND*	-
V <sub>CCO</sub>	1	-	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
I/O, V <sub>REF</sub>	1	P164	C11	A18	36
I/O	1	P165	A13	B17	39
I/O	1	-	-	E15	42
I/O	1	-	-	A17	45
I/O	1	-	D11	D15	48
GND	-	-	GND*	GND*	-
I/O	1	P166	A12	C16	51
I/O	1	-	-	D14	54
I/O, V <sub>REF</sub>	1	P167	E11	E14	60
I/O	1	P168	B11	A16	63
GND	-	P169	GND*	GND*	-
V <sub>CCO</sub>	1	P170	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
V <sub>CCINT</sub>	-	P171	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	1	P172	A11	C15	66
I/O	1	P173	C10	B15	69
I/O	1	-	-	E13	72
I/O	1	-	-	A15	75
I/O	1	-	-	F12	78
GND	-	-	GND*	GND*	-
I/O	1	P174	B10	C14	81
I/O	1	-	-	B14	84
I/O	1	-	-	A14	87

#### XC2S200 Device Pinouts (Continued)

XC2S200 Pad	Name				Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O	1	P175	D10	D13	90
I/O	1	P176	A10	C13	93
GND	-	P177	GND*	GND*	-
V <sub>CCO</sub>	1	-	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
I/O, V <sub>REF</sub>	1	P178	B9	B13	96
I/O	1	P179	E10	E12	99
I/O	1	-	-	A13	105
I/O	1	-	A9	B12	108
I/O	1	P180	D9	D12	111
I/O	1	-	-	C12	114
I/O	1	P181	A8	D11	120
I, GCK2	1	P182	C9	A11	126
GND	-	P183	GND*	GND*	-
V <sub>CCO</sub>	1	P184	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
V <sub>CCO</sub>	0	P184	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
I, GCK3	0	P185	B8	C11	127
V <sub>CCINT</sub>	-	P186	$V_{CCINT}^{*}$	$V_{CCINT}^{*}$	-
I/O	0	-	-	E11	137
I/O	0	P187	A7	A10	140
I/O	0	-	D8	B10	143
I/O	0	-	-	F11	146
I/O	0	P188	A6	C10	152
I/O, V <sub>REF</sub>	0	P189	B7	A9	155
V <sub>CCO</sub>	0	-	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
GND	-	P190	GND*	GND*	-
I/O	0	P191	C8	B9	158
I/O	0	P192	D7	E10	161
I/O	0	-	-	C9	164
I/O	0	-	-	D10	167
I/O	0	P193	E7	A8	170
GND	-	-	GND*	GND*	-
I/O	0	-	-	D9	173
I/O	0	-	-	B8	176
I/O	0	-	-	C8	179
I/O	0	P194	C7	E9	182
I/O	0	P195	B6	A7	185
V <sub>CCINT</sub>	-	P196	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	0	P197	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-

#### Additional XC2S200 Package Pins (Continued)

#### 11/02/00

FG456							
V <sub>CCINT</sub> Pins							
E5	E18	F6	F17	G7	G8		
G9	G14	G15	G16	H7	H16		
J7	J16	P7	P16	R7	R16		
T7	T8	Т9	T14	T15	T16		
U6	U17	V5	V18	-	-		
V <sub>CCO</sub> Bank 0 Pins							
F7	F8	F9	F10	G10	G11		
V <sub>CCO</sub> Bank 1 Pins							
F13	F14	F15	F16	G12	G13		
V <sub>CCO</sub> Bank 2 Pins							
G17	H17	J17	K16	K17	L16		
V <sub>CCO</sub> Bank 3 Pins							
M16	N16	N17	P17	R17	T17		
V <sub>CCO</sub> Bank 4 Pins							
T12	T13	U13	U14	U15	U16		
V <sub>CCO</sub> Bank 5 Pins							
T10	T11	U7	U8	U9	U10		
V <sub>CCO</sub> Bank 6 Pins							
M7	N6	N7	P6	R6	T6		
		V <sub>CCO</sub> Ba	nk 7 Pins				

#### Additional XC2S200 Package Pins (Continued)

G6	H6	J6	K6	K7	L7		
GND Pins							
A1	A22	B2	B21	C3	C20		
J9	J10	J11	J12	J13	J14		
K9	K10	K11	K12	K13	K14		
L9	L10	L11	L12	L13	L14		
M9	M10	M11	M12	M13	M14		
N9	N10	N11	N12	N13	N14		
P9	P10	P11	P12	P13	P14		
Y3	Y20	AA2	AA21	AB1	AB22		
Not Connected Pins							
A2	A6	A12	B11	B16	C2		
D1	D4	D18	D19	E17	E19		
G2	G22	L2	L19	M2	M21		
R3	R20	U3	U18	V6	W4		
W19	Y5	Y22	AA1	AA3	AA11		
AA16	AB7	AB12	AB21	-	-		
11/02/00							

# **Revision History**

Version	Date	Description
110.	Dute	Description
2.0	09/18/00	Sectioned the Spartan-II Family data sheet into four modules. Corrected all known errors in the pinout tables.
2.1	10/04/00	Added notes requiring PWDN to be tied to V <sub>CCINT</sub> when unused.
2.2	11/02/00	Removed the Power Down feature.
2.3	03/05/01	Added notes on pinout tables for IRDY and TRDY.
2.4	04/30/01	Reinstated XC2S50 V <sub>CCO</sub> Bank 7, GND, and "not connected" pins missing in version 2.3.
2.5	09/03/03	Added caution about Not Connected Pins to XC2S30 pinout tables on page 76.
2.8	06/13/08	Added "Package Overview" section. Added notes to clarify shared V <sub>CCO</sub> banks. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.