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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	176
Number of Gates	150000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s150-5fg256i

General Overview

The Spartan-II family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-II FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master

serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes.

Spartan-II FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-II FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-II FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-II devices provide system clock rates up to 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-II FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

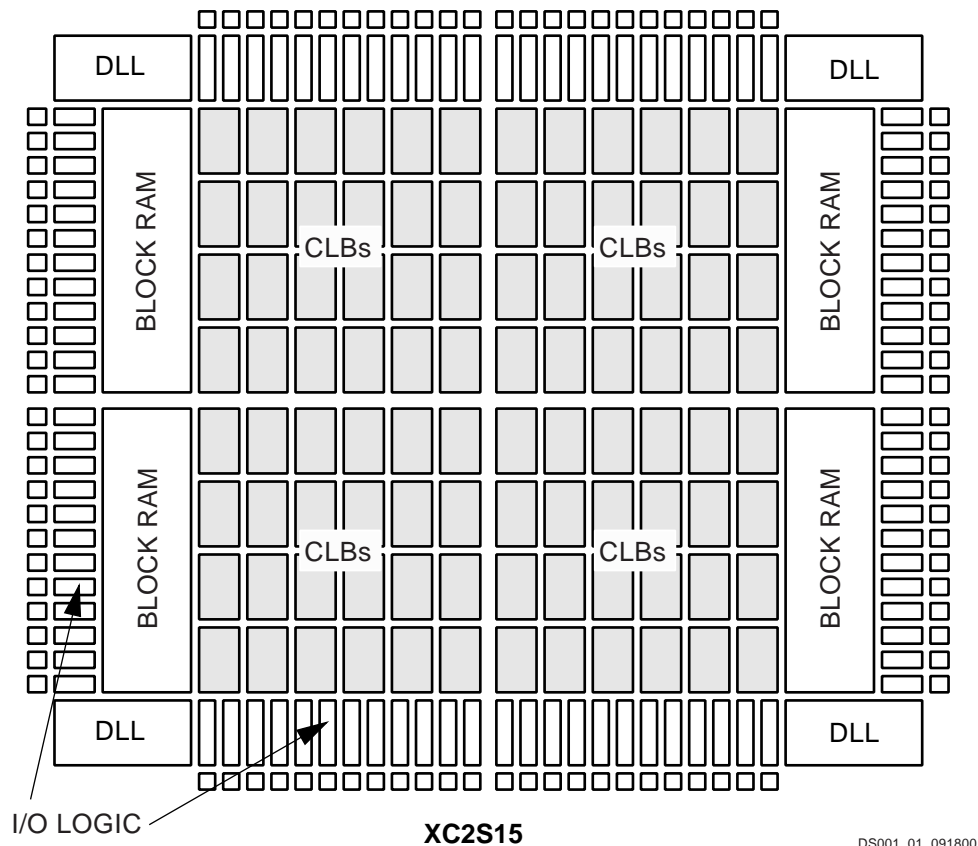
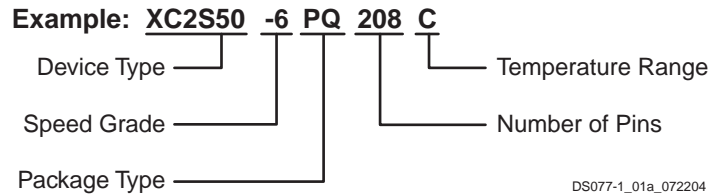


Figure 1: Basic Spartan-II Family FPGA Block Diagram

Ordering Information

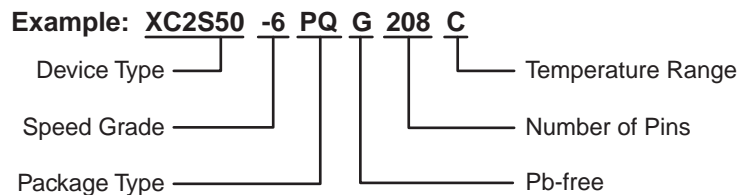
Spartan-II devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

Standard Packaging



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Pb-Free Packaging



DS077-1_01b_072204

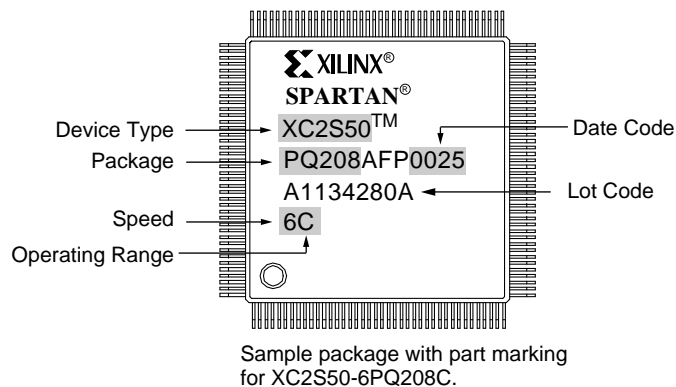
Device Ordering Options

Device	Speed Grade		Number of Pins / Package Type		Temperature Range (T _J)	
XC2S15	-5	Standard Performance	VQ(G)100	100-pin Plastic Very Thin QFP	C = Commercial	0°C to +85°C
XC2S30	-6	Higher Performance ⁽¹⁾	CS(G)144	144-ball Chip-Scale BGA	I = Industrial	-40°C to +100°C
XC2S50			TQ(G)144	144-pin Plastic Thin QFP		
XC2S100			PQ(G)208	208-pin Plastic QFP		
XC2S150			FG(G)256	256-ball Fine Pitch BGA		
XC2S200			FG(G)456	456-ball Fine Pitch BGA		

Notes:

- The -6 speed grade is exclusively available in the Commercial temperature range.

Device Part Marking



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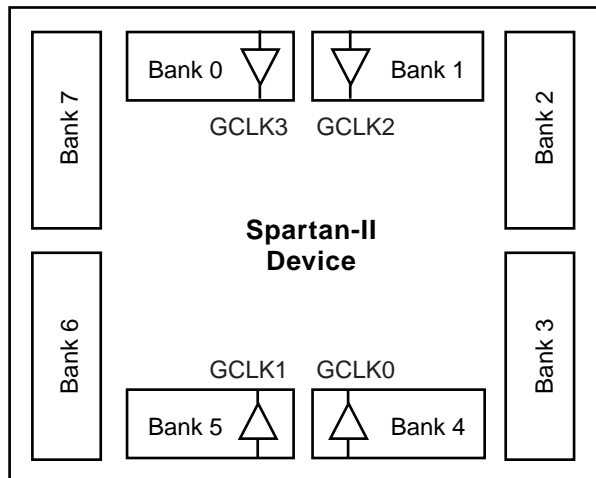
drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. Voltage is determined by the output standards in use.



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Figure 3: Spartan-II I/O Banks

Within a bank, output standards may be mixed only if they use the same V_{CCO} . Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO} .

Table 4: Compatible Output Standards

V_{CCO}	Compatible Standards
3.3V	PCI, LVTTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF} . In this case, certain user-I/O pins are

automatically configured as inputs for the V_{REF} voltage. About one in six of the I/O pins in the bank assume this role.

V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

In a bank, inputs requiring V_{REF} can be mixed with those that do not but only one V_{REF} voltage may be used within a bank. Input buffers that use V_{REF} are not 5V tolerant. LVTTTL, LVCMOS2, and PCI are 5V tolerant. The V_{CCO} and V_{REF} pins for each bank appear in the device pinout tables.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device. All V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

Independent Banks Available

Package	VQ100 PQ208	CS144 TQ144	FG256 FG456
Independent Banks	1	4	8

Configurable Logic Block

The basic building block of the Spartan-II FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. Output from the function generator in each LC drives the CLB output and the D input of the flip-flop. Each Spartan-II FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 4.

In addition to the four basic LCs, the Spartan-II FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

Look-Up Tables

Spartan-II FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-II FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-II FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-II FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing," page 12. Each Spartan-II FPGA BUFT has an independent 3-state control pin and an independent input pin.

Block RAM

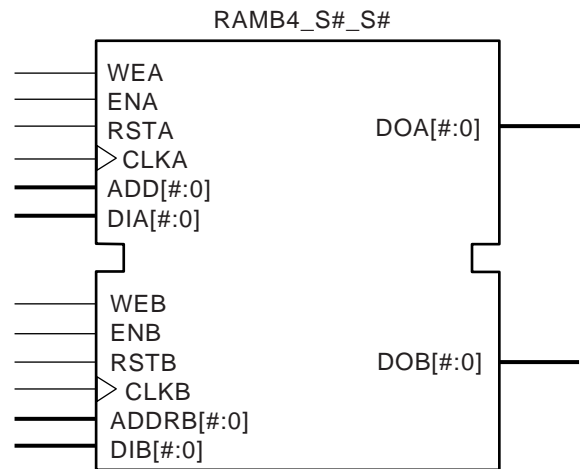
Spartan-II FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks.

Table 5: Spartan-II Block RAM Amounts

Spartan-II Device	# of Blocks	Total Block RAM Bits
XC2S15	4	16K
XC2S30	6	24K
XC2S50	8	32K
XC2S100	10	40K
XC2S150	12	48K
XC2S200	14	56K

Each block RAM cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.



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Figure 5: Dual-Port Block RAM

Table 6 shows the depth and width aspect ratios for the block RAM.

Table 6: Block RAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-II FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

Programmable Routing Matrix

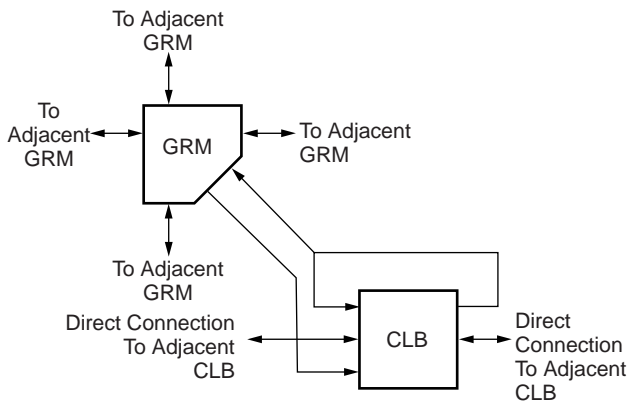
It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The local routing resources, as shown in Figure 6, provide the following three types of connections:

- Interconnections among the LUTs, flip-flops, and General Routing Matrix (GRM)
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM



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Figure 6: Spartan-II Local Routing

General Purpose Routing

Most Spartan-II FPGA signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to other GRMs six blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are unidirectional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and

efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-II devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Dedicated Routing

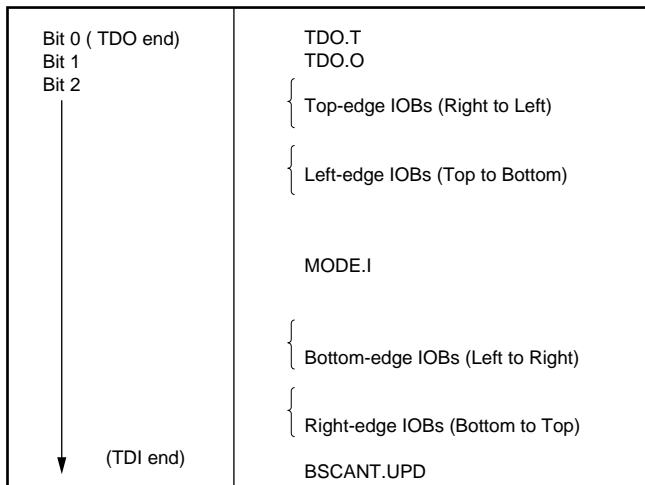
Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-II architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 7.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-II devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.



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Figure 10: Boundary Scan Bit Sequence

Development System

Spartan-II FPGAs are supported by the Xilinx ISE® development tools. The basic methodology for Spartan-II FPGA design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation, while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under a single graphical interface, providing designers with a common user interface regardless of their choice of entry and verification tools. The software simplifies the selection of implementation options with pull-down menus and on-line help.

For HDL design entry, the Xilinx FPGA development system provides interfaces to several synthesis design environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-II FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The design environment supports hierarchical design entry. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

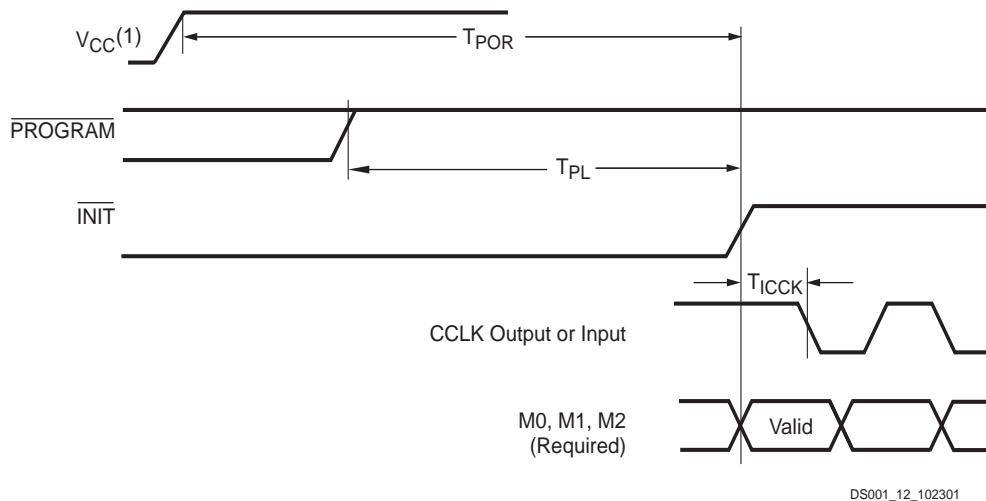
Timing requirements are entered in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, the development system includes a download cable, which connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can read back the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.



Symbol	Description	Min	Max
T_{POR}	Power-on reset	-	2 ms
T_{PL}	Program latency	-	100 μ s
T_{ICCK}	CCLK output delay (Master Serial mode only)	0.5 μ s	4 μ s
$T_{PROGRAM}$	Program pulse width	300 ns	-

Notes: (referring to waveform above:)

- Before configuration can begin, V_{CCINT} must be greater than 1.6V and V_{CCO} Bank 2 must be greater than 1.0V.

Figure 12: Configuration Timing on Power-Up

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving \overline{INIT} Low. At this time, the user can delay configuration by holding either $\overline{PROGRAM}$ or \overline{INIT} Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional \overline{INIT} line is driving a Low logic level during memory clearing. To avoid contention, use an open-drain driver to keep \overline{INIT} Low.

With no delay in force, the device indicates that the memory is completely clear by driving \overline{INIT} High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data

Once \overline{INIT} is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 14. Loading data using the Slave Parallel mode is shown in Figure 19, page 25.

CRC Error Checking

During the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values

do not match, the FPGA drives \overline{INIT} Low to indicate that a frame error has occurred and configuration is aborted.

To reconfigure the device, the $\overline{PROGRAM}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See "Clearing Configuration Memory".

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State net. This activates I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-down resistors present.
3. Negates Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

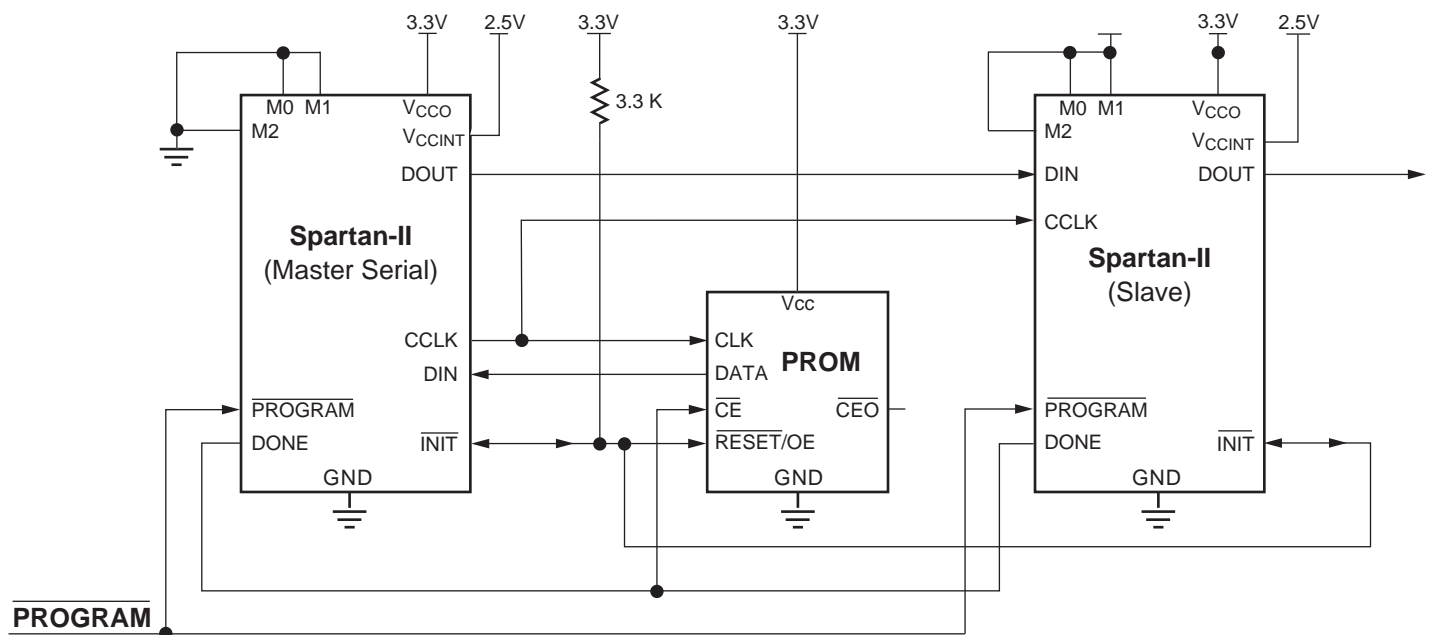
Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is $2^{20}-1$ (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until INIT pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.



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Notes:

1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 15: Master/Slave Serial Configuration Circuit Diagram

division factor N except for non-integer division in High Frequency (HF) mode. For division factor 1.5 the duty cycle in the HF mode is 33.3% High and 66.7% Low. For division factor 2.5, the duty cycle in the HF mode is 40.0% High and 60.0% Low.

1x Clock Outputs — CLK[0/90/180/270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 degree phase-shifted version. The relationship between phase shift and the corresponding period shift appears in [Table 10](#).

The timing diagrams in [Figure 26](#) illustrate the DLL clock output characteristics.

Table 10: Relationship of Phase-Shifted Output Clock to Period Shift

Phase (degrees)	Period Shift (percent)
0	0%
90	25%
180	50%
270	75%

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL primitive. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

Locked Output — LOCKED

In order to achieve lock, the DLL may need to sample several thousand clock cycles. After the DLL achieves lock the LOCKED signal activates. The ["DLL Timing Parameters"](#) section of Module 3 provides estimates for locking times.

In order to guarantee that the system clock is established prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other

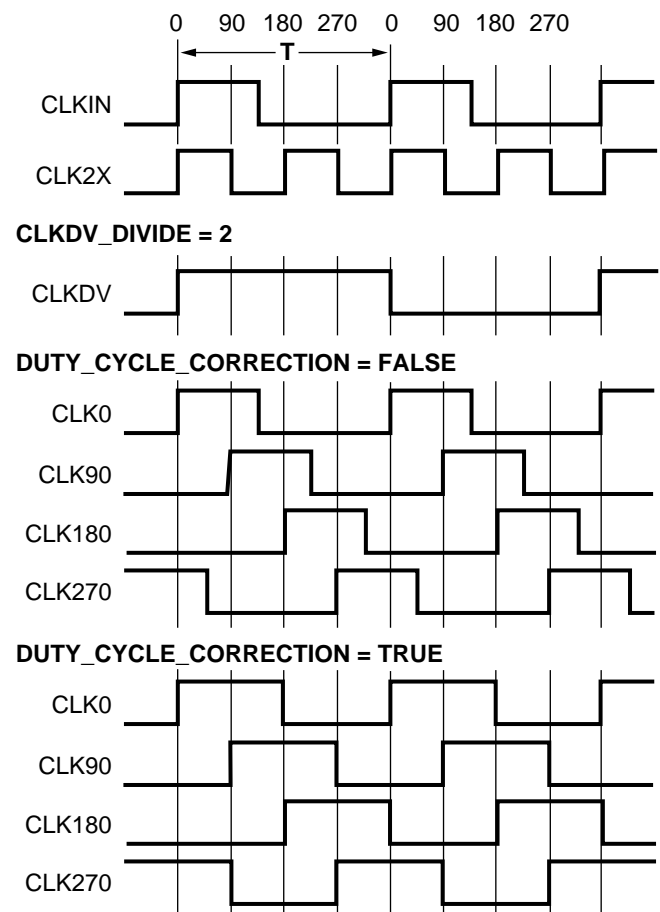
spurious movement. In particular the CLK2X output will appear as a 1x clock with a 25/75 duty cycle.

DLL Properties

Properties provide access to some of the Spartan-II family DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, such that they exhibit a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL primitive.



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Figure 26: DLL Output Characteristics

Clock Divide Property

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Using Block RAM Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block RAM memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block RAM memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Block RAM memory supports two operating modes.

- Read Through
- Write Back

Read Through (One Clock Edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (One Clock Edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

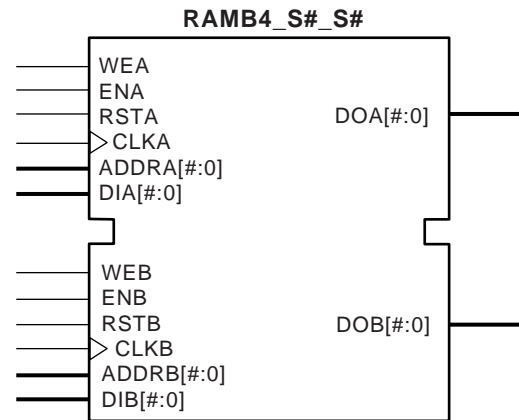
Block RAM Characteristics

1. All inputs are registered with the port clock and have a setup to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The block RAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (*i.e.*, clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

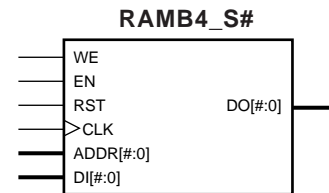
Library Primitives

Figure 31 and Figure 32 show the two generic library block RAM primitives. Table 11 describes all of the available primitives for synthesis and simulation.



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Figure 31: Dual-Port Block RAM Memory



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Figure 32: Single-Port Block RAM Memory

Table 11: Available Library Primitives

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16

property. This property could have one of the following seven values.

DRIVE=2
 DRIVE=4
 DRIVE=6
 DRIVE=8
 DRIVE=12 (Default)
 DRIVE=16
 DRIVE=24

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See [Figure 36, page 39](#) for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The V_{CCO} supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined V_{CCO} supply. The TQ144 and the CS144 packages provide four independent V_{CCO} supplies. The FG256 and the FG456 provide eight independent V_{CCO} supplies.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

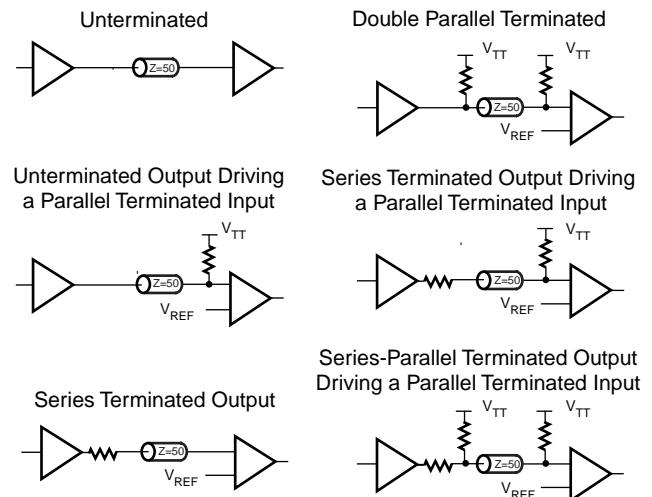
The following lists output termination techniques:

None
 Series
 Parallel (Shunt)
 Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None
 Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in [Figure 41](#).



DS001_41_032300

Figure 41: Overview of Standard Input and Output Termination Methods

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Propagation Delays						
T _{IOOP}	O input to pad	-	2.9	-	3.4	ns
T _{IOOLP}	O input to pad via transparent latch	-	3.4	-	4.0	ns
3-state Delays						
T _{IOTHZ}	T input to pad high-impedance ⁽¹⁾	-	2.0	-	2.3	ns
T _{IOTON}	T input to valid data on pad	-	3.0	-	3.6	ns
T _{IOTLPHZ}	T input to pad high impedance via transparent latch ⁽¹⁾	-	2.5	-	2.9	ns
T _{IOTLPON}	T input to valid data on pad via transparent latch	-	3.5	-	4.2	ns
T _{GTS}	GTS to pad high impedance ⁽¹⁾	-	5.0	-	5.9	ns
Sequential Delays						
T _{IOCKP}	Clock CLK to pad	-	2.9	-	3.4	ns
T _{IOCKHZ}	Clock CLK to pad high impedance (synchronous) ⁽¹⁾	-	2.3	-	2.7	ns
T _{IOCKON}	Clock CLK to valid data on pad (synchronous)	-	3.3	-	4.0	ns
Setup/Hold Times with Respect to Clock CLK ⁽²⁾						
T _{IOOCK} / T _{IOCKO}	O input	1.1 / 0	-	1.3 / 0	-	ns
T _{IOOCECK} / T _{IOCKOCE}	OCE input	0.9 / 0.01	-	0.9 / 0.01	-	ns
T _{IOSRCKO} / T _{IOCKOSR}	SR input (OFF)	1.2 / 0	-	1.3 / 0	-	ns
T _{IOTCK} / T _{IOCKT}	3-state setup times, T input	0.8 / 0	-	0.9 / 0	-	ns
T _{IOTCECK} / T _{IOCKTCE}	3-state setup times, TCE input	1.0 / 0	-	1.0 / 0	-	ns
T _{IOSRCKT} / T _{IOCKTSR}	3-state setup times, SR input (TFF)	1.1 / 0	-	1.2 / 0	-	ns
Set/Reset Delays						
T _{IOSRP}	SR input to pad (asynchronous)	-	3.7	-	4.4	ns
T _{IOSRHZ}	SR input to pad high impedance (asynchronous) ⁽¹⁾	-	3.1	-	3.7	ns
T _{IOSRON}	SR input to valid data on pad (asynchronous)	-	4.1	-	4.9	ns
T _{IOGSRQ}	GSR to pad	-	9.9	-	11.7	ns

Notes:

- Three-state turn-off delays should not be adjusted.
- A zero hold time listing indicates no hold time or a negative hold time.

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Combinatorial Delays						
T _{ILO}	4-input function: F/G inputs to X/Y outputs	-	0.6	-	0.7	ns
T _{IF5}	5-input function: F/G inputs to F5 output	-	0.7	-	0.9	ns
T _{IF5X}	5-input function: F/G inputs to X output	-	0.9	-	1.1	ns
T _{IF6Y}	6-input function: F/G inputs to Y output via F6 MUX	-	1.0	-	1.1	ns
T _{F5INY}	6-input function: F5IN input to Y output	-	0.4	-	0.4	ns
T _{IFNCTL}	Incremental delay routing through transparent latch to XQ/YQ outputs	-	0.7	-	0.9	ns
T _{BYYB}	BY input to YB output	-	0.6	-	0.7	ns
Sequential Delays						
T _{CKO}	FF clock CLK to XQ/YQ outputs	-	1.1	-	1.3	ns
T _{CKLO}	Latch clock CLK to XQ/YQ outputs	-	1.2	-	1.5	ns
Setup/Hold Times with Respect to Clock CLK ⁽¹⁾						
T _{ICK} / T _{CKI}	4-input function: F/G inputs	1.3 / 0	-	1.4 / 0	-	ns
T _{IF5CK} / T _{CKIF5}	5-input function: F/G inputs	1.6 / 0	-	1.8 / 0	-	ns
T _{F5INCK} / T _{CKF5IN}	6-input function: F5IN input	1.0 / 0	-	1.1 / 0	-	ns
T _{IF6CK} / T _{CKIF6}	6-input function: F/G inputs via F6 MUX	1.6 / 0	-	1.8 / 0	-	ns
T _{DICK} / T _{CKDI}	BX/BY inputs	0.8 / 0	-	0.8 / 0	-	ns
T _{CECK} / T _{CKCE}	CE input	0.9 / 0	-	0.9 / 0	-	ns
T _{RCK} / T _{CKR}	SR/BY inputs (synchronous)	0.8 / 0	-	0.8 / 0	-	ns
Clock CLK						
T _{CH}	Minimum pulse width, High	-	1.9	-	1.9	ns
T _{CL}	Minimum pulse width, Low	-	1.9	-	1.9	ns
Set/Reset						
T _{RPW}	Minimum pulse width, SR/BY inputs	3.1	-	3.1	-	ns
T _{RQ}	Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	-	1.1	-	1.3	ns
T _{IOGSRQ}	Delay from GSR to XQ/YQ outputs	-	9.9	-	11.7	ns
F _{TOG}	Toggle frequency (for export control)	-	263	-	263	MHz

Notes:

1. A zero hold time listing indicates no hold time or a negative hold time.

Introduction

This section describes how the various pins on a Spartan®-II FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-II FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all

information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-II FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-II FPGA packages, as outlined in [Table 35](#).

Table 35: Pin Definitions

Pin Name	Dedicated	Direction	Description
GCK0, GCK1, GCK2, GCK3	No	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin. It is an input for slave-parallel and slave-serial modes, and output in master-serial mode.
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. This pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
CS	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V _{CCINT}	Yes	Input	Power supply pins for the internal core logic.
V _{CCO}	Yes	Input	Power supply pins for output drivers (subject to banking rules)
V _{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx® PCI cores. If the cores are not used, these pins are available as user I/Os.

Table 36: Spartan-II Family Package Options

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass ⁽¹⁾ (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	60	0.5	16 x 16	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	92	0.5	22 x 22	1.60	1.4
CS144 / CSG144	144	Chip Scale Ball Grid Array (CSBGA)	92	0.8	12 x 12	1.20	0.3
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	140	0.5	30.6 x 30.6	3.70	5.3
FG256 / FGG256	256	Fine-pitch Ball Grid Array (FBGA)	176	1.0	17 x 17	2.00	0.9
FG456 / FGG456	456	Fine-pitch Ball Grid Array (FBGA)	284	1.0	23 x 23	2.60	2.2

Notes:

- Package mass is $\pm 10\%$.

Note: Some early versions of Spartan-II devices, including the XC2S15 and XC2S30 ES devices and the XC2S150 with date code 0045 or earlier, included a power-down pin. For more information, see [Answer Record 10500](#).

VCCO Banks

Some of the I/O standards require specific V_{CCO} voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Eight I/O banks result from separating each edge of the FPGA into two banks (see [Figure 3](#) in Module 2). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. In the smaller packages, the V_{CCO} pins are connected between banks, effectively reducing the number of independent banks available (see [Table 37](#)). These interconnected banks are shown in the Pinout Tables with V_{CCO} pads for multiple banks connected to the same pin.

Table 37: Independent VCCO Banks Available

Package	VQ100 PQ208	CS144 TQ144	FG256 FG456
Independent Banks	1	4	8

Package Overview

[Table 36](#) shows the six low-cost, space-saving production package styles for the Spartan-II family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra 'G' in the package style name. For example, the standard "CS144" package becomes "CSG144" when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in [Table 38](#).

For additional package information, see [UG112: Device Package User Guide](#).

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in [Table 38](#).

Material Declaration Data Sheets (MDDS) are also available on the [Xilinx web site](#) for each package.

Table 38: Xilinx Package Documentation

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
CS144	Package Drawing	PK149_CS144
CSG144		PK103_CSG144
PQ208	Package Drawing	PK166_PQ208
PQG208		PK123_PQG208
FG256	Package Drawing	PK151_FG256
FGG256		PK105_FGG256
FG456	Package Drawing	PK154_FG456
FGG456		PK109_FGG456

XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
I/O	5	P99	P63	P6	326
GND	-	P98	P64	GND*	-
V _{CCO}	5	-	P65	V _{CCO} Bank 5*	-
V _{CCINT}	-	P97	P66	V _{CCINT} *	-
I/O	5	P96	P67	R6	329
I/O	5	P95	P68	M7	332
I/O	5	-	P69	N7	338
I/O	5	-	P70	T6	341
I/O	5	-	P71	P7	344
GND	-	-	P72	GND*	-
I/O, V _{REF}	5	P94	P73	P8	347
I/O	5	-	P74	R7	350
I/O	5	-	-	T7	353
I/O	5	P93	P75	T8	356
V _{CCINT}	-	P92	P76	V _{CCINT} *	-
I, GCK1	5	P91	P77	R8	365
V _{CCO}	5	P90	P78	V _{CCO} Bank 5*	-
V _{CCO}	4	P90	P78	V _{CCO} Bank 4*	-
GND	-	P89	P79	GND*	-
I, GCK0	4	P88	P80	N8	366
I/O	4	P87	P81	N9	370
I/O	4	P86	P82	R9	373
I/O	4	-	-	N10	376
I/O	4	-	P83	T9	379
I/O, V _{REF}	4	P85	P84	P9	382
GND	-	-	P85	GND*	-
I/O	4	-	P86	M10	385
I/O	4	-	P87	R10	388
I/O	4	-	P88	P10	391
I/O	4	P84	P89	T10	397
I/O	4	P83	P90	R11	400
V _{CCINT}	-	P82	P91	V _{CCINT} *	-
V _{CCO}	4	-	P92	V _{CCO} Bank 4*	-
GND	-	P81	P93	GND*	-
I/O	4	P80	P94	M11	403
I/O	4	P79	P95	T11	406
I/O	4	P78	P96	N11	409
I/O	4	-	-	R12	412

XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
I/O	4	-	P97	P11	415
I/O, V _{REF}	4	P77	P98	T12	418
GND	-	-	-	GND*	-
I/O	4	-	P99	T13	421
I/O	4	-	-	N12	424
I/O	4	P76	P100	R13	427
I/O	4	-	-	P12	430
I/O	4	P75	P101	P13	433
I/O	4	P74	P102	T14	436
GND	-	P73	P103	GND*	-
DONE	3	P72	P104	R14	439
V _{CCO}	4	P71	P105	V _{CCO} Bank 4*	-
V _{CCO}	3	P70	P105	V _{CCO} Bank 3*	-
PROGRAM	-	P69	P106	P15	442
I/O (INIT)	3	P68	P107	N15	443
I/O (D7)	3	P67	P108	N14	446
I/O	3	-	-	T15	449
I/O	3	P66	P109	M13	452
I/O	3	-	-	R16	455
I/O	3	-	P110	M14	458
GND	-	-	-	GND*	-
I/O, V _{REF}	3	P65	P111	L14	461
I/O	3	-	P112	M15	464
I/O	3	-	-	L12	467
I/O	3	P64	P113	P16	470
I/O	3	P63	P114	L13	473
I/O (D6)	3	P62	P115	N16	476
GND	-	P61	P116	GND*	-
V _{CCO}	3	-	P117	V _{CCO} Bank 3*	-
V _{CCINT}	-	-	P118	V _{CCINT} *	-
I/O (D5)	3	P60	P119	M16	479
I/O	3	P59	P120	K14	482
I/O	3	-	-	L16	485
I/O	3	-	P121	K13	488
I/O	3	-	P122	L15	491
I/O	3	-	P123	K12	494
GND	-	-	P124	GND*	-
I/O, V _{REF}	3	P58	P125	K16	497
I/O (D4)	3	P57	P126	J16	500

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						
Function	Bank	TQ144	PQ208	FG256	FG456	Bndry Scan
I/O	0	-	P188	A6	C10	107
I/O, V _{REF}	0	P12	P189	B7	A9	110
GND	-	-	P190	GND*	GND*	-
I/O	0	-	P191	C8	B9	113
I/O	0	-	P192	D7	E10	116
I/O	0	-	P193	E7	A8	122
I/O	0	-	-	-	D9	125
I/O	0	P11	P194	C7	E9	128
I/O	0	P10	P195	B6	A7	131
V _{CCINT}	-	P9	P196	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	0	-	P197	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	P8	P198	GND*	GND*	-
I/O	0	P7	P199	A5	B7	134
I/O, V _{REF}	0	P6	P200	C6	E8	137
I/O	0	-	-	-	D8	140
I/O	0	-	P201	B5	C7	143
I/O	0	-	-	D6	D7	146
I/O	0	-	P202	A4	D6	152
I/O, V _{REF}	0	P5	P203	B4	C6	155
V _{CCO}	0	-	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	-	-	GND*	GND*	-
I/O	0	-	P204	E6	B5	158
I/O	0	-	-	D5	E7	161
I/O	0	-	-	-	E6	164
I/O	0	P4	P205	A3	B4	167
I/O	0	-	-	C5	A3	170
I/O	0	P3	P206	B3	C5	176
TCK	-	P2	P207	C4	C4	-
V _{CCO}	0	P1	P208	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
V _{CCO}	7	P144	P208	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-

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Notes:

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S150 Package Pins

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

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FG256

V _{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V _{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V _{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V _{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V _{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V _{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V _{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V _{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V _{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

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Additional XC2S150 Package Pins (Continued)

FG456

V _{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V _{CCO} Bank 0 Pins					
F7	F8	F9	F10	G10	G11
V _{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V _{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V _{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V _{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V _{CCO} Bank 5 Pins					
T10	T11	U7	U8	U9	U10
V _{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V _{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A6	A12	A13	A14	B11
B16	C2	C8	C9	D1	D4
D18	D19	E13	E17	E19	F11
G2	G22	H21	J1	J4	K2
K18	K19	L2	L19	M2	M17
M21	N1	P1	P5	P22	R3
R20	R22	U3	U18	V6	W4
W13	W15	W19	Y5	Y22	AA1
AA3	AA9	AA10	AA11	AA16	AB7
AB8	AB12	AB14	AB21	-	-

11/02/00

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	6	-	-	T2	449
I/O	6	P43	L4	U1	452
GND	-	-	GND*	GND*	-
I/O	6	-	M2	R5	455
I/O	6	-	-	V1	458
I/O	6	-	-	T5	461
I/O	6	P44	L3	U2	464
I/O, V _{REF}	6	P45	N1	T3	467
V _{CCO}	6	-	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-
I/O	6	P46	P1	T4	470
I/O	6	-	L5	W1	473
GND	-	-	GND*	GND*	-
I/O	6	-	-	V2	476
I/O	6	-	-	U4	482
I/O, V _{REF}	6	P47	N2	Y1	485
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	488
I/O	6	-	-	V3	491
I/O	6	-	-	V4	494
I/O	6	P48	R1	Y2	500
I/O	6	P49	M3	W3	503
M1	-	P50	P2	U5	506
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	507
V _{CCO}	6	P53	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
V _{CCO}	5	P53	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
M2	-	P54	R3	Y4	508
I/O	5	-	-	W5	518
I/O	5	-	-	AB3	521
I/O	5	-	N5	V7	524
GND	-	-	GND*	GND*	-
I/O, V _{REF}	5	P57	T2	Y6	527
I/O	5	-	-	AA4	530
I/O	5	-	-	AB4	536
I/O	5	-	P5	W6	539
I/O	5	P58	T3	Y7	542
GND	-	-	GND*	GND*	-

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V _{CCO}	5	-	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
I/O, V _{REF}	5	P59	T4	AA5	545
I/O	5	P60	M6	AB5	548
I/O	5	-	-	V8	551
I/O	5	-	-	AA6	554
I/O	5	-	T5	AB6	557
GND	-	-	GND*	GND*	-
I/O	5	P61	N6	AA7	560
I/O	5	-	-	W7	563
I/O, V _{REF}	5	P62	R5	W8	569
I/O	5	P63	P6	Y8	572
GND	-	P64	GND*	GND*	-
V _{CCO}	5	P65	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCINT}	-	P66	V _{CCINT} *	V _{CCINT} *	-
I/O	5	P67	R6	AA8	575
I/O	5	P68	M7	V9	578
I/O	5	-	-	AB8	581
I/O	5	-	-	W9	584
I/O	5	-	-	AB9	587
GND	-	-	GND*	GND*	-
I/O	5	P69	N7	Y9	590
I/O	5	-	-	V10	593
I/O	5	-	-	AA9	596
I/O	5	P70	T6	W10	599
I/O	5	P71	P7	AB10	602
GND	-	P72	GND*	GND*	-
V _{CCO}	5	-	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
I/O, V _{REF}	5	P73	P8	Y10	605
I/O	5	P74	R7	V11	608
I/O	5	-	-	AA10	614
I/O	5	-	T7	W11	617
I/O	5	P75	T8	AB11	620
I/O	5	-	-	U11	623
V _{CCINT}	-	P76	V _{CCINT} *	V _{CCINT} *	-
I, GCK1	5	P77	R8	Y11	635
V _{CCO}	5	P78	V _{CCO} Bank 5*	V _{CCO} Bank 5*	-
V _{CCO}	4	P78	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I, GCK0	4	P80	N8	W12	636
I/O	4	P81	N9	U12	640
I/O	4	-	-	V12	646
I/O	4	P82	R9	Y12	649
I/O	4	-	N10	AA12	652
I/O	4	-	-	W13	655
I/O	4	P83	T9	AB13	661
I/O, V _{REF}	4	P84	P9	AA13	664
V _{CCO}	4	-	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P85	GND*	GND*	-
I/O	4	P86	M10	Y13	667
I/O	4	P87	R10	V13	670
I/O	4	-	-	AB14	673
I/O	4	-	-	W14	676
I/O	4	P88	P10	AA14	679
GND	-	-	GND*	GND*	-
I/O	4	-	-	V14	682
I/O	4	-	-	Y14	685
I/O	4	-	-	W15	688
I/O	4	P89	T10	AB15	691
I/O	4	P90	R11	AA15	694
V _{CCINT}	-	P91	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	4	P92	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P93	GND*	GND*	-
I/O	4	P94	M11	Y15	697
I/O, V _{REF}	4	P95	T11	AB16	700
I/O	4	-	-	AB17	706
I/O	4	P96	N11	V15	709
GND	-	-	GND*	GND*	-
I/O	4	-	R12	Y16	712
I/O	4	-	-	AA17	715
I/O	4	-	-	W16	718
I/O	4	P97	P11	AB18	721
I/O, V _{REF}	4	P98	T12	AB19	724
V _{CCO}	4	-	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	-	GND*	GND*	-
I/O	4	P99	T13	Y17	727
I/O	4	-	N12	V16	730
I/O	4	-	-	AA18	733

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	4	-	-	W17	739
I/O, V _{REF}	4	P100	R13	AB20	742
GND	-	-	GND*	GND*	-
I/O	4	-	P12	AA19	745
I/O	4	-	-	V17	748
I/O	4	-	-	Y18	751
I/O	4	P101	P13	AA20	757
I/O	4	P102	T14	W18	760
GND	-	P103	GND*	GND*	-
DONE	3	P104	R14	Y19	763
V _{CCO}	4	P105	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
V _{CCO}	3	P105	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
PROGRAM	-	P106	P15	W20	766
I/O (INIT)	3	P107	N15	V19	767
I/O (D7)	3	P108	N14	Y21	770
I/O	3	-	-	V20	776
I/O	3	-	-	AA22	779
I/O	3	-	T15	W21	782
GND	-	-	GND*	GND*	-
I/O, V _{REF}	3	P109	M13	U20	785
I/O	3	-	-	U19	788
I/O	3	-	-	V21	794
GND	-	-	GND*	GND*	-
I/O	3	-	R16	T18	797
I/O	3	P110	M14	W22	800
GND	-	-	GND*	GND*	-
V _{CCO}	3	-	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
I/O, V _{REF}	3	P111	L14	U21	803
I/O	3	P112	M15	T20	806
I/O	3	-	-	T19	809
I/O	3	-	-	V22	812
I/O	3	-	L12	T21	815
GND	-	-	GND*	GND*	-
I/O	3	P113	P16	R18	818
I/O	3	-	-	U22	821
I/O, V _{REF}	3	P114	L13	R19	827
I/O (D6)	3	P115	N16	T22	830
GND	-	P116	GND*	GND*	-