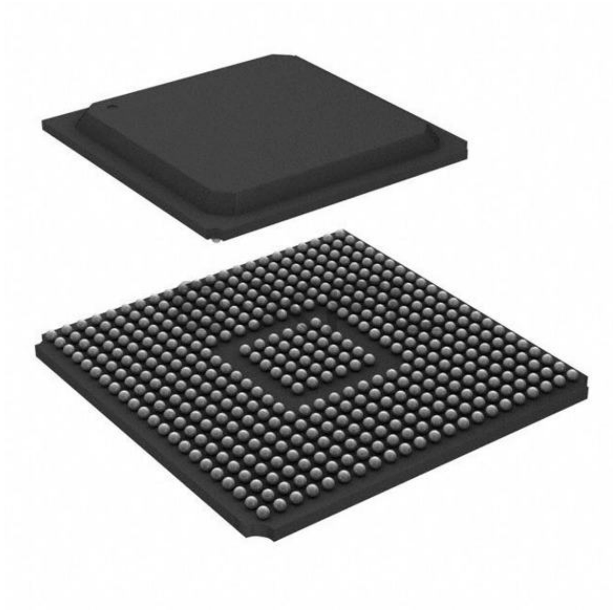
AMD Xilinx - XC2S150-5FG456I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	260
Number of Gates	150000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s150-5fg456i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

General Overview

The Spartan-II family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-II FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes.

Spartan-II FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-II FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-II FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-II devices provide system clock rates up to 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-II FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

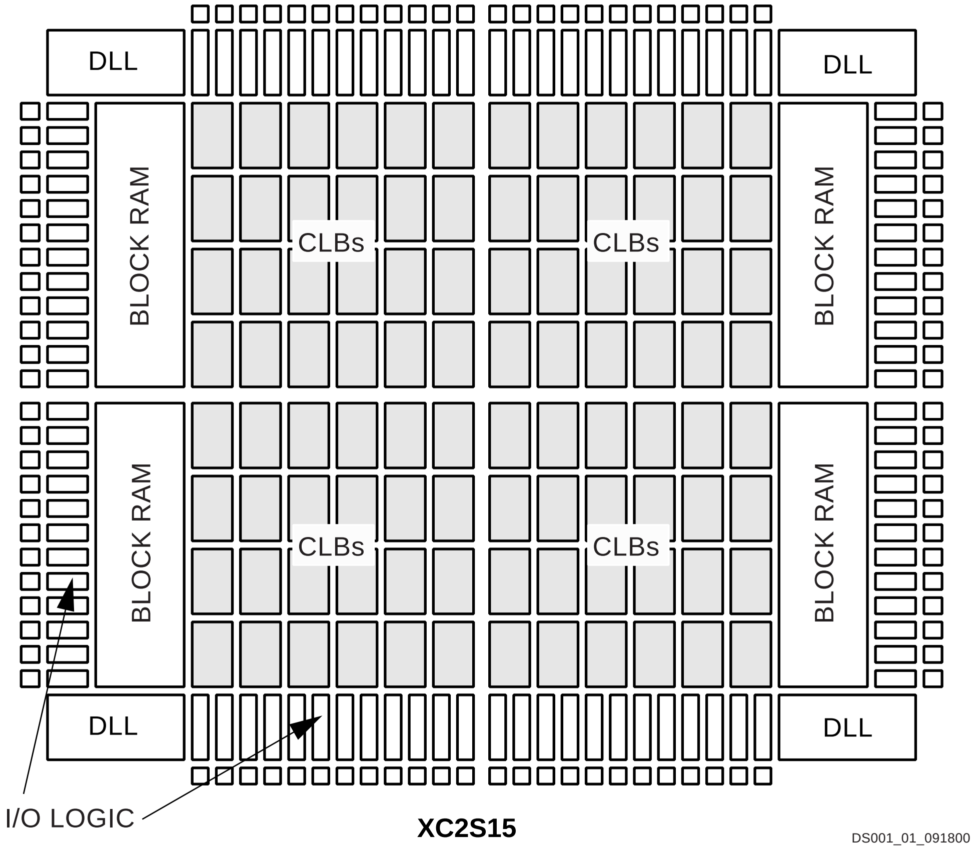


Figure 1: **Basic Spartan-II Family FPGA Block Diagram**

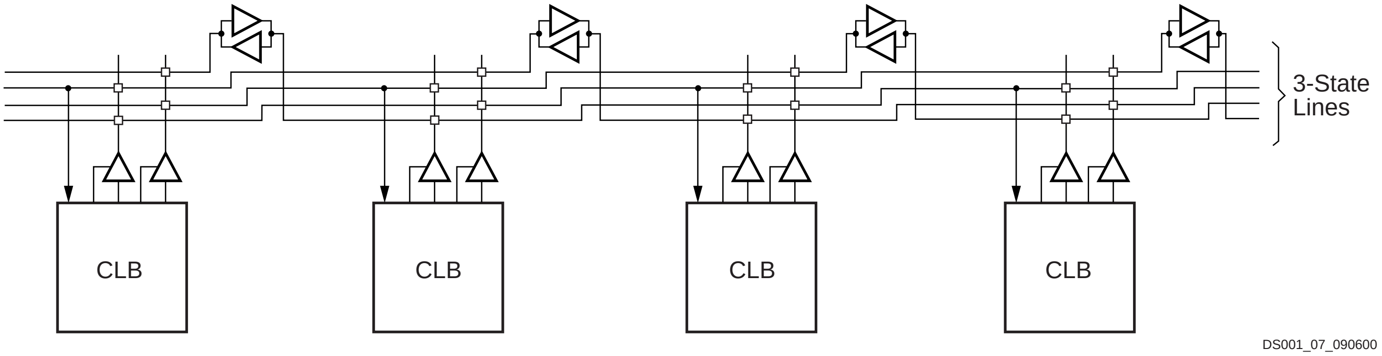


Figure 7: **BUFT Connections to Dedicated Horizontal Bus Lines**

Clock Distribution

The Spartan-II family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 8.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing. Global clock pins do not have the option for internal, weak pull-up resistors.

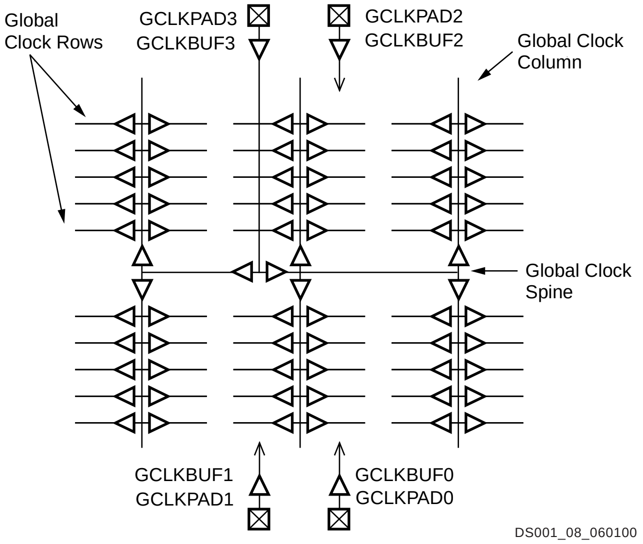


Figure 8: **Global Clock Distribution Network**

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.

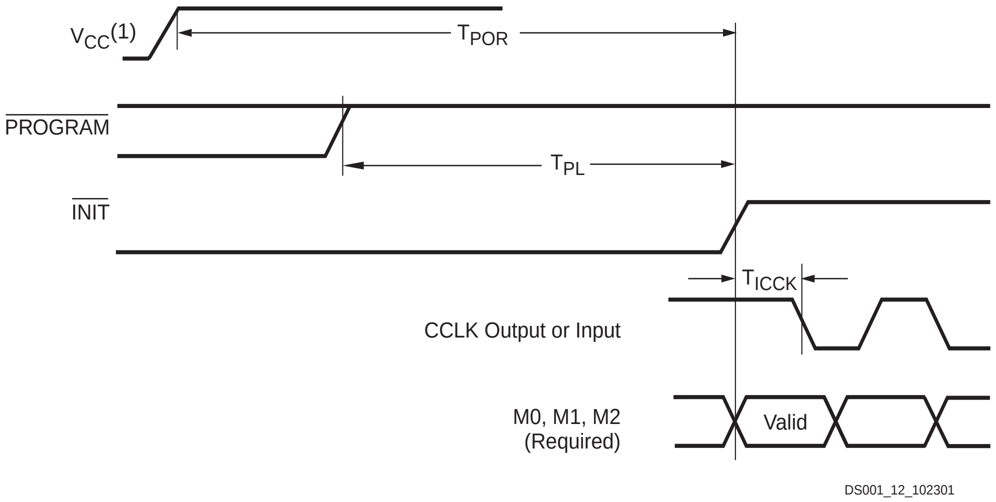
The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-II devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

Boundary Scan

Spartan-II devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}. TDI, TMS, and TCK have a default internal weak pull-up resistor, and TDO has no default resistor. Bitstream options allow setting any of the four TAP pins to have an internal pull-up, pull-down, or neither.



Symbol	Description	Min	Max
T_{POR}	Power-on reset	-	2 ms
T_{PL}	Program latency	-	100 µs
T_{ICCK}	CCLK output delay (Master Serial mode only)	0.5 µs	4 µs
$T_{PROGRAM}$	Program pulse width	300 ns	-

Notes: (referring to waveform above:)

1. Before configuration can begin, V_{CCINT} must be greater than 1.6V and V_{CCO} Bank 2 must be greater than 1.0V.

Figure 12: **Configuration Timing on Power-Up**

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving $\overline{\text{INIT}}$ Low. At this time, the user can delay configuration by holding either $\overline{\text{PROGRAM}}$ or $\overline{\text{INIT}}$ Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional $\overline{\text{INIT}}$ line is driving a Low logic level during memory clearing. To avoid contention, use an open-drain driver to keep $\overline{\text{INIT}}$ Low.

With no delay in force, the device indicates that the memory is completely clear by driving $\overline{\text{INIT}}$ High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data

Once $\overline{\text{INIT}}$ is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 14. Loading data using the Slave Parallel mode is shown in Figure 19, page 25.

CRC Error Checking

During the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives $\overline{\text{INIT}}$ Low to indicate that a frame error has occurred and configuration is aborted.

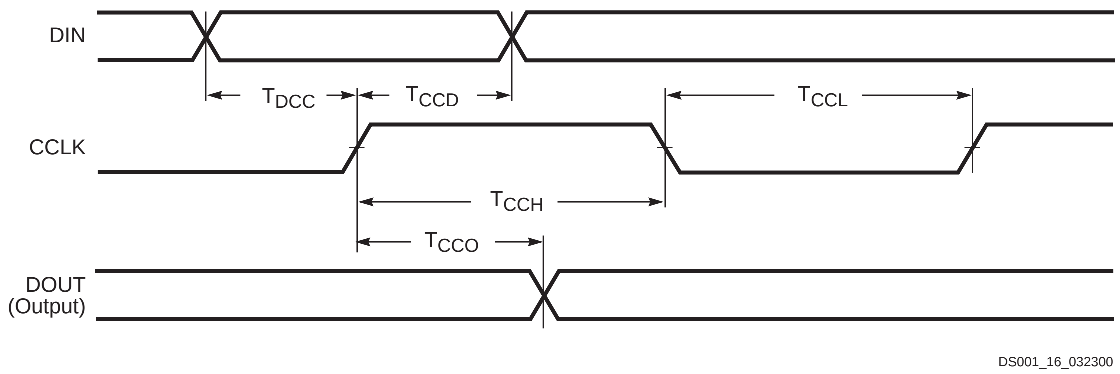
To reconfigure the device, the $\overline{\text{PROGRAM}}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See "Clearing Configuration Memory".

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

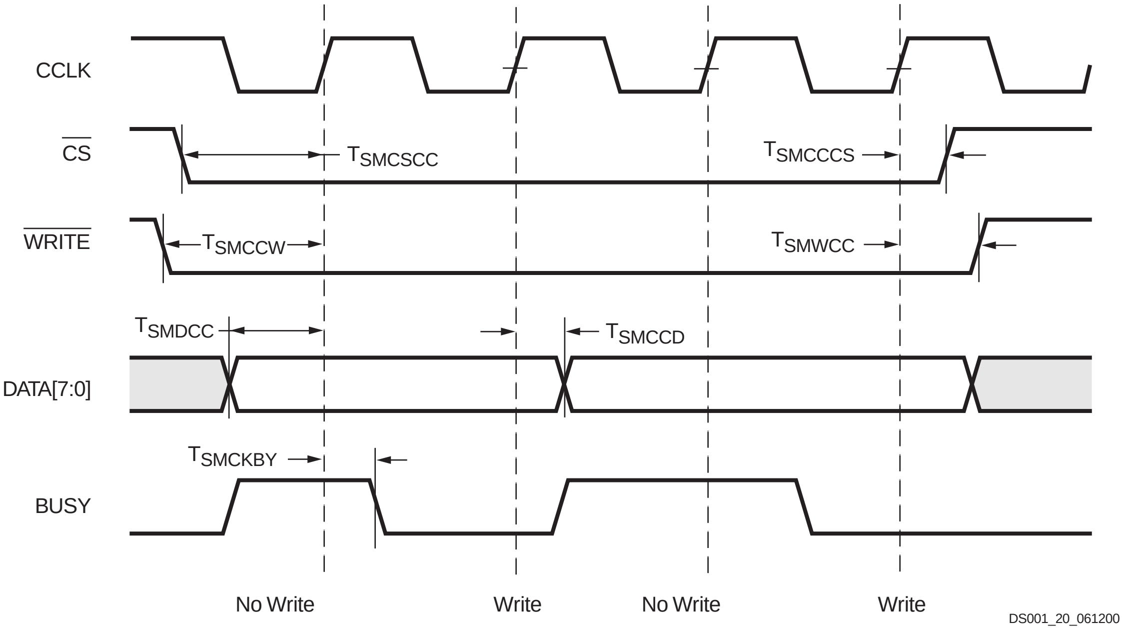
During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State net. This activates I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-down resistors present.
3. Negates Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.



Symbol		Description		Units
T_{DCC}	CCLK	DIN setup	5	ns, min
T_{CCD}		DIN hold	0	ns, min
T_{CCO}		DOUT	12	ns, max
T_{CCH}		High time	5	ns, min
T_{CCL}		Low time	5	ns, min
F_{CC}		Maximum frequency	66	MHz, max

Figure 16: **Slave Serial Mode Timing**



Symbol		Description		Units
T_{SMDCC}	CCLK	D0-D7 setup/hold	5	ns, min
T_{SMCCD}		D0-D7 hold	0	ns, min
T_{SMCSCC}		$\overline{\text{CS}}$ setup	7	ns, min
T_{SMCCCS}		$\overline{\text{CS}}$ hold	0	ns, min
T_{SMCCW}		$\overline{\text{WRITE}}$ setup	7	ns, min
T_{SMWCC}		$\overline{\text{WRITE}}$ hold	0	ns, min
T_{SMCKBY}		BUSY propagation delay	12	ns, max
F_{CC}		Maximum frequency	66	MHz, max
F_{CCNH}		Maximum frequency with no handshake	50	MHz, max

Figure 20: **Slave Parallel Write Timing**

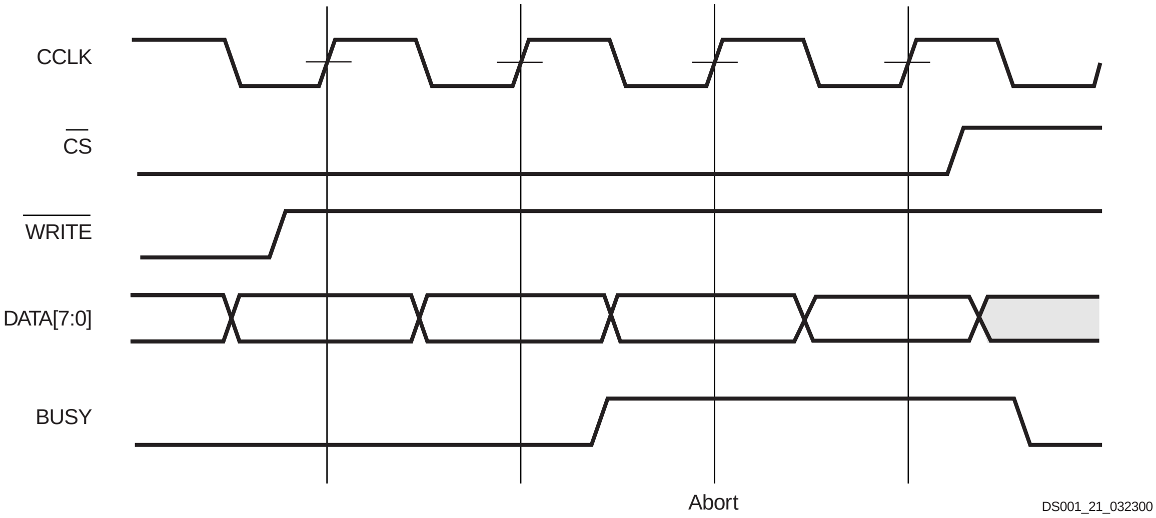


Figure 21: **Slave Parallel Write Abort Waveforms**

Design Considerations

This section contains more detailed design information on the following features:

- Delay-Locked Loop . . . see page 27
- Block RAM . . . see page 32
- Versatile I/O . . . see page 36

Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Primitives

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.

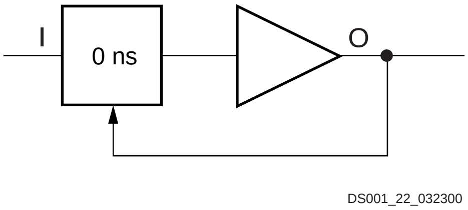


Figure 22: **Simplified DLL Macro BUFGDLL**

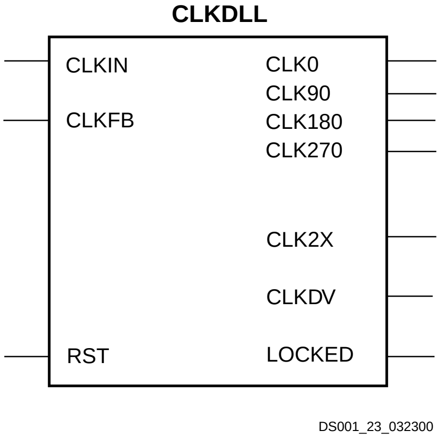


Figure 23: **Standard DLL Primitive CLKDLL**

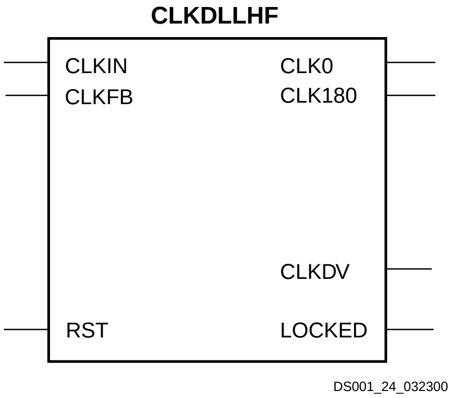


Figure 24: **High-Frequency DLL Primitive CLKDLLHF**

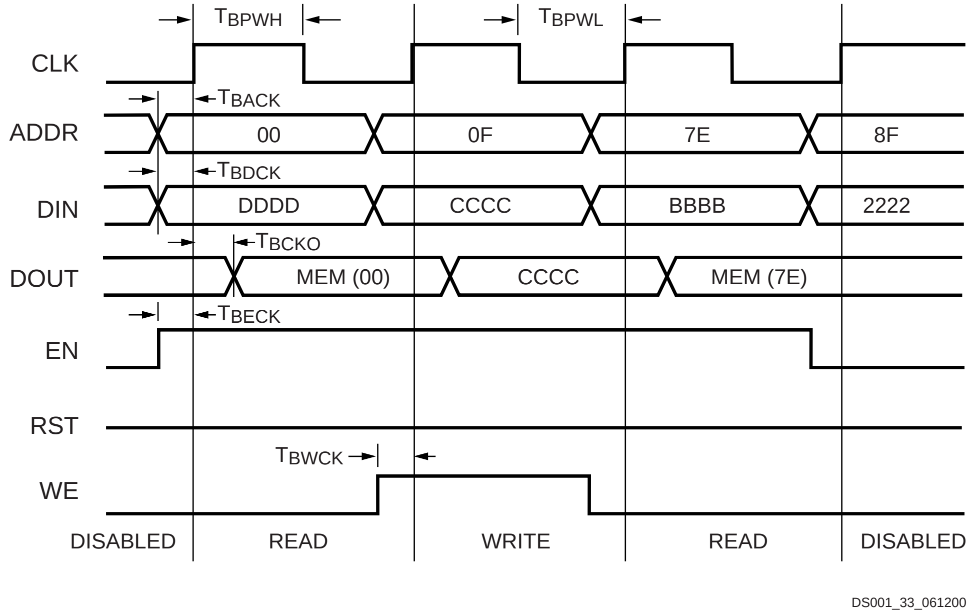


Figure 33: **Timing Diagram for Single-Port Block RAM Memory**

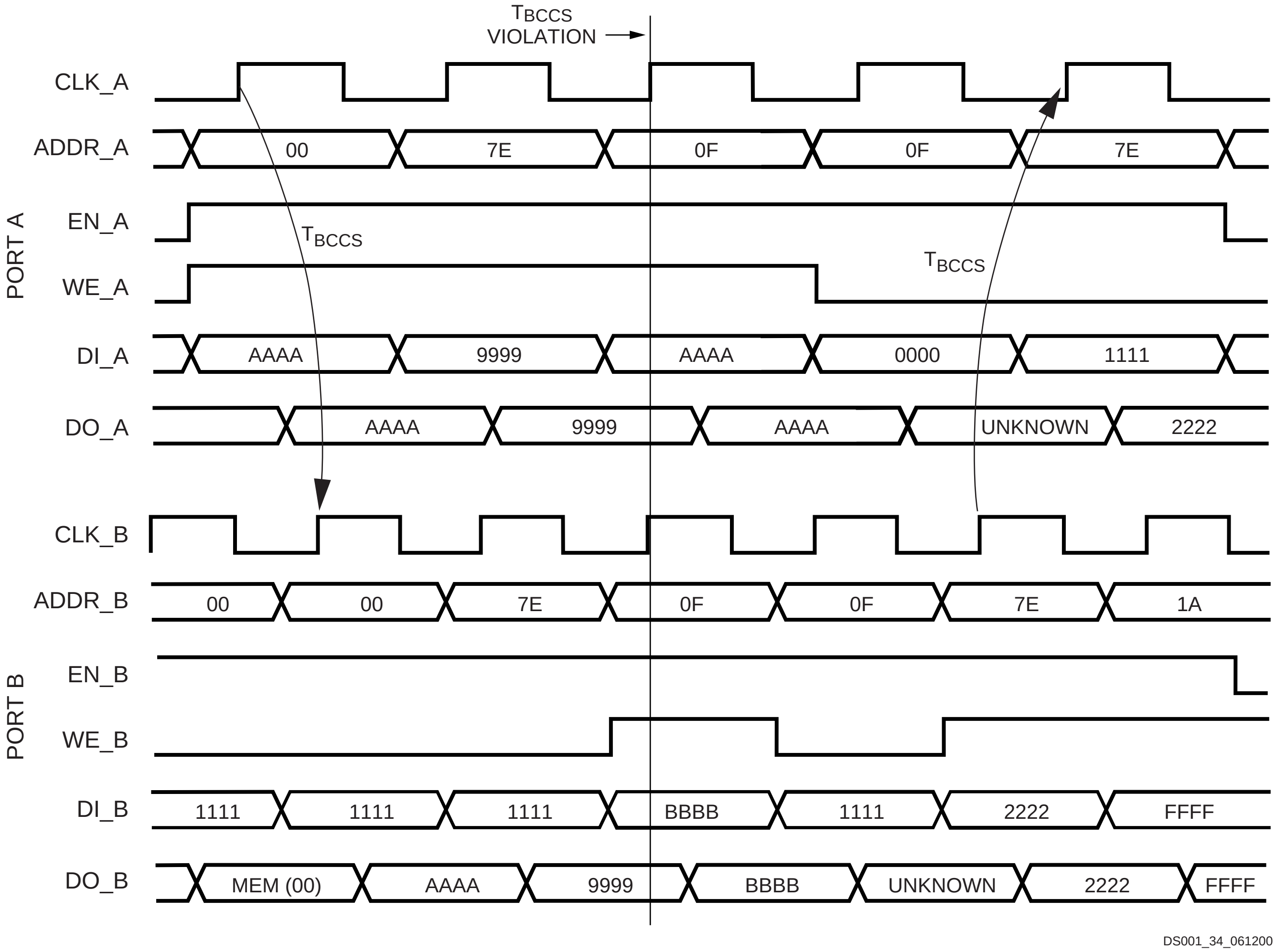


Figure 34: **Timing Diagram for a True Dual-Port Read/Write Block RAM Memory**

PCI — Peripheral Component Interface

The Peripheral Component Interface (PCI) standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a push-pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}). I/Os configured for the PCI, 33 MHz, 5V standard are also 5V-tolerant.

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic (GTL) standard is a high-speed bus standard (JESD8.3). Xilinx has implemented the terminated variation of this standard. This standard requires a differential amplifier input buffer and an open-drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus (GTL+) standard is a high-speed bus standard (JESD8.3).

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed, 1.5V bus standard (EIA/JESD 8-6). This standard has four variations or classes. Versatile I/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V (SSTL3) standard is a general purpose 3.3V memory bus standard (JESD8-8). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V (SSTL2) standard is a general purpose 2.5V memory bus standard (JESD8-9). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated (CTT) standard is a 3.3V memory bus standard (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with processors for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

Library Primitives

The Xilinx library includes an extensive list of primitives designed to provide support for the variety of Versatile I/O features. Most of these primitives represent variations of the five generic Versatile I/O primitives:

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

These primitives are available with various extensions to define the desired I/O standard. However, it is recommended that customers use a a property or attribute on the generic primitive to specify the I/O standard. See "Versatile I/O Properties".

IBUF

Signals used as inputs to the Spartan-II device must source an input buffer (IBUF) via an external input port. The generic IBUF primitive appears in Figure 35. The assumed standard is LVTTL when the generic IBUF has no specified extension or property.

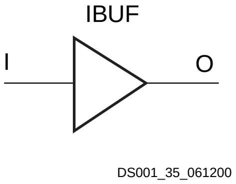


Figure 35: **Input Buffer (IBUF) Primitive**

When the IBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 16 summarizes the input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

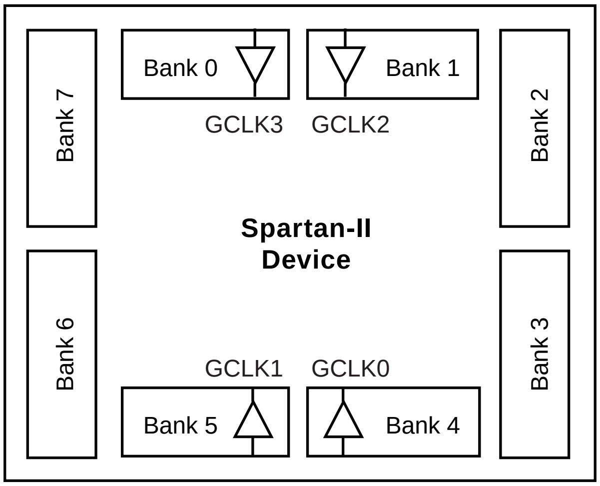


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Figure 36: **I/O Banks**

Table 16: **Xilinx Input Standards Compatibility Requirements**

Rule 1	All differential amplifier input signals within a bank are required to be of the same standard.
Rule 2	There are no placement restrictions for inputs with standards that require a single-ended input buffer.

IBUFG

Signals used as high fanout clock inputs to the Spartan-II device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG primitive can only drive a CLKDLL, CLKDLLHF, or a BUFG primitive. The generic IBUFG primitive appears in Figure 37.

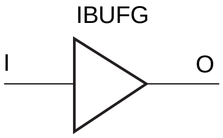

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Figure 37: **Global Clock Input Buffer (IBUFG) Primitive**

With no extension or property specified for the generic IBUFG primitive, the assumed standard is LVTTL.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP primitive represents a combination of the LVTTL IBUFG and BUFG primitives, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

The Spartan-II FPGA BUFGP primitive can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) primitive appears in Figure 38.

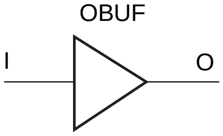

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Figure 38: **Output Buffer (OBUF) Primitive**

With no extension or property specified for the generic OBUF primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 18 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 19 for the number of effective output power/ground pairs for each Spartan-II device and package combination.

Table 18: **Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package	
	CS, FG	PQ, TQ, VQ
LVTTL Slow Slew Rate, 2 mA drive	68	36
LVTTL Slow Slew Rate, 4 mA drive	41	20
LVTTL Slow Slew Rate, 6 mA drive	29	15
LVTTL Slow Slew Rate, 8 mA drive	22	12
LVTTL Slow Slew Rate, 12 mA drive	17	9
LVTTL Slow Slew Rate, 16 mA drive	14	7
LVTTL Slow Slew Rate, 24 mA drive	9	5
LVTTL Fast Slew Rate, 2 mA drive	40	21
LVTTL Fast Slew Rate, 4 mA drive	24	12
LVTTL Fast Slew Rate, 6 mA drive	17	9
LVTTL Fast Slew Rate, 8 mA drive	13	7
LVTTL Fast Slew Rate, 12 mA drive	10	5
LVTTL Fast Slew Rate, 16 mA drive	8	4
LVTTL Fast Slew Rate, 24 mA drive	5	3
LVCMOS2	10	5
PCI	8	4
GTL	4	4
GTL+	4	4
HSTL Class I	18	9
HSTL Class III	9	5
HSTL Class IV	5	3
SSTL2 Class I	15	8
SSTL2 Class II	10	5
SSTL3 Class I	11	6
SSTL3 Class II	7	4
CTT	14	7
AGP	9	5

Notes:

1. This analysis assumes a 35 pF load for each output.

Table 19: **Effective Output Power/Ground Pairs for Spartan-II Devices**

Pkg.	Spartan-II Devices					
	XC2S 15	XC2S 30	XC2S 50	XC2S 100	XC2S 150	XC2S 200
VQ100	8	8	-	-	-	-
CS144	12	12	-	-	-	-
TQ144	12	12	12	12	-	-
PQ208	-	16	16	16	16	16
FG256	-	-	16	16	16	16
FG456	-	-	-	48	48	48

Termination Examples

Creating a design with the Versatile I/O features requires the instantiation of the desired library primitive within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the Versatile I/O features. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 45. DC voltage specifications appear in Table 23 for the HSTL_III standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

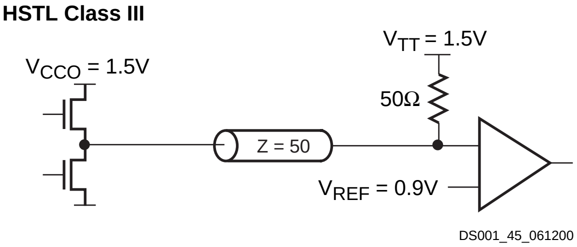

Figure 45: **Terminated HSTL Class III**

Table 23: **HSTL Class III Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Notes:

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class IV

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 46.DC voltage specifications appear in Table 23 for the HSTL_IV standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

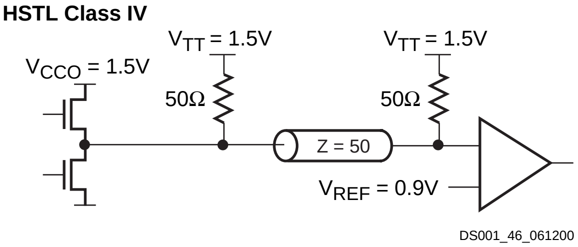

Figure 46: **Terminated HSTL Class IV**

Table 24: **HSTL Class IV Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

Notes:

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

SSTL3 Class I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 47. DC voltage specifications appear in Table 25 for the SSTL3_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

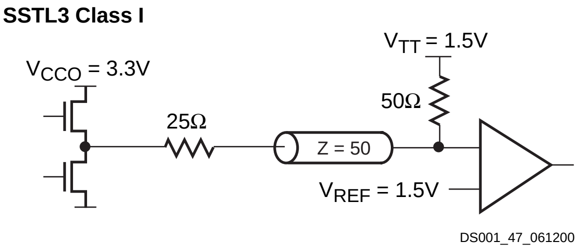

Figure 47: **Terminated SSTL3 Class I**

Table 25: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.6$	1.9	-	-
$V_{OL} \leq V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is $V_{CCO} + 0.3$.
2. V_{IL} minimum does not conform to the formula.

SSTL3 Class II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 48. DC voltage specifications appear in Table 26 for the SSTL3_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

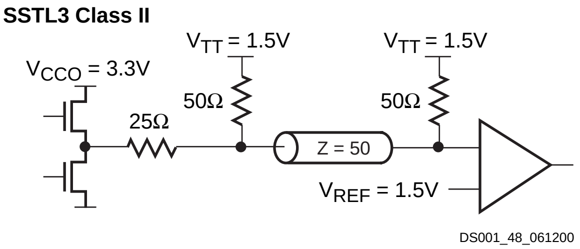

Figure 48: **Terminated SSTL3 Class II**

Table 26: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.8$	2.1	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is $V_{CCO} + 0.3$
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 49. DC voltage specifications appear in Table 27 for the SSTL2_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

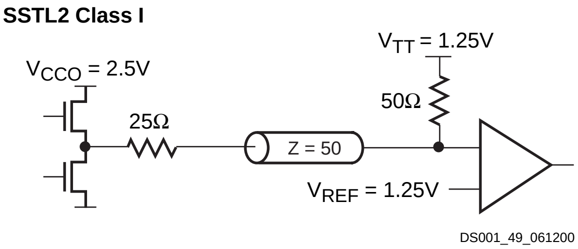

Figure 49: **Terminated SSTL2 Class I**

Table 27: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \geq V_{REF} + 0.18$	1.33	1.43	$3.0^{(2)}$
$V_{IL} \leq V_{REF} - 0.18$	$-0.3^{(3)}$	1.07	1.17
$V_{OH} \geq V_{REF} + 0.61$	1.76	-	-
$V_{OL} \leq V_{REF} - 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL} at V_{OL} (mA)	7.6	-	-

Notes:

1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

SSTL2 Class II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 50. DC voltage specifications appear in Table 28 for the SSTL2_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

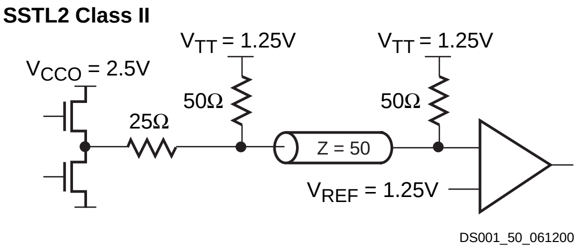

Figure 50: **Terminated SSTL2 Class II**

Table 28: **SSTL2_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \geq V_{REF} + 0.18$	1.33	1.43	$3.0^{(2)}$
$V_{IL} \leq V_{REF} - 0.18$	$-0.3^{(3)}$	1.07	1.17
$V_{OH} \geq V_{REF} + 0.8$	1.95	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:

1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

IOB Input Delay Adjustments for Different Standards(1)

Input delays associated with the pad are specified for LVTTL. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Data Input Delay Adjustments					
T_{ILVTTL}	Standard-specific data input delay adjustments	LVTTL	0	0	ns
$T_{ILVCMOS2}$		LVCMOS2	–0.04	–0.05	ns
T_{IPCI33_3}		PCI, 33 MHz, 3.3V	–0.11	–0.13	ns
T_{IPCI33_5}		PCI, 33 MHz, 5.0V	0.26	0.30	ns
T_{IPCI66_3}		PCI, 66 MHz, 3.3V	–0.11	–0.13	ns
T_{IGTL}		GTL	0.20	0.24	ns
T_{IGTLP}		GTL+	0.11	0.13	ns
T_{IHSTL}		HSTL	0.03	0.04	ns
T_{ISSTL2}		SSTL2	–0.08	–0.09	ns
T_{ISSTL3}		SSTL3	–0.04	–0.05	ns
T_{ICTT}		CTT	0.02	0.02	ns
T_{IAGP}		AGP	–0.06	–0.07	ns

Notes:

1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Propagation Delays						
T_{IOOP}	O input to pad	-	2.9	-	3.4	ns
T_{IOOLP}	O input to pad via transparent latch	-	3.4	-	4.0	ns
3-state Delays						
T_{IOTHZ}	T input to pad high-impedance(1)	-	2.0	-	2.3	ns
T_{IOTON}	T input to valid data on pad	-	3.0	-	3.6	ns
$T_{IOTLPHZ}$	T input to pad high impedance via transparent latch(1)	-	2.5	-	2.9	ns
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	-	3.5	-	4.2	ns
T_{GTS}	GTS to pad high impedance(1)	-	5.0	-	5.9	ns
Sequential Delays						
T_{IOCKP}	Clock CLK to pad	-	2.9	-	3.4	ns
T_{IOCKHZ}	Clock CLK to pad high impedance (synchronous)(1)	-	2.3	-	2.7	ns
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	-	3.3	-	4.0	ns
Setup/Hold Times with Respect to Clock CLK(2)						
T_{IOOCK} / T_{IOCKO}	O input	1.1 / 0	-	1.3 / 0	-	ns
$T_{IOOCECK}$ / $T_{IOCKOCE}$	OCE input	0.9 / 0.01	-	0.9 / 0.01	-	ns
$T_{IOSRCKO}$ / $T_{IOCKOSR}$	SR input (OFF)	1.2 / 0	-	1.3 / 0	-	ns
T_{IOTCK} / T_{IOCKT}	3-state setup times, T input	0.8 / 0	-	0.9 / 0	-	ns
$T_{IOTCECK}$ / $T_{IOCKTCE}$	3-state setup times, TCE input	1.0 / 0	-	1.0 / 0	-	ns
$T_{IOSRCKT}$ / $T_{IOCKTSR}$	3-state setup times, SR input (TFF)	1.1 / 0	-	1.2 / 0	-	ns
Set/Reset Delays						
T_{IOSRP}	SR input to pad (asynchronous)	-	3.7	-	4.4	ns
T_{IOSRHZ}	SR input to pad high impedance (asynchronous)(1)	-	3.1	-	3.7	ns
T_{IOSRON}	SR input to valid data on pad (asynchronous)	-	4.1	-	4.9	ns
T_{IOGSRQ}	GSR to pad	-	9.9	-	11.7	ns

Notes:
1. Three-state turn-off delays should not be adjusted.
2. A zero hold time listing indicates no hold time or a negative hold time.

IOB Output Delay Adjustments for Different Standards[1]

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.2	16.9	ns
T_{OLVTTL_S4}		4 mA	7.2	8.6	ns
T_{OLVTTL_S6}		6 mA	4.7	5.5	ns
T_{OLVTTL_S8}		8 mA	2.9	3.5	ns
T_{OLVTTL_S12}		12 mA	1.9	2.2	ns
T_{OLVTTL_S16}		16 mA	1.7	2.0	ns
T_{OLVTTL_S24}		24 mA	1.3	1.5	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	12.6	15.0	ns
T_{OLVTTL_F4}		4 mA	5.1	6.1	ns
T_{OLVTTL_F6}		6 mA	3.0	3.6	ns
T_{OLVTTL_F8}		8 mA	1.0	1.2	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.1	–0.1	ns
T_{OLVTTL_F24}		24 mA	–0.1	–0.2	ns
$T_{OLVCMOS2}$		LVCMOS2	0.2	0.2	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.4	2.9	ns
T_{OPCI33_5}		PCI, 33 MHz, 5.0V	2.9	3.5	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.3	–0.4	ns
T_{OGTL}		GTL	0.6	0.7	ns
T_{OGTLP}		GTL+	0.9	1.1	ns
T_{OHSTL_I}		HSTL I	–0.4	–0.5	ns
T_{OHSTL_III}		HSTL III	–0.8	–1.0	ns
T_{OHSTL_IV}		HSTL IV	–0.9	–1.1	ns
T_{OSSTL2_I}		SSTL2 I	–0.4	–0.5	ns
T_{OSSLT2_II}		SSTL2 II	–0.8	–1.0	ns
T_{OSSTL3_I}		SSTL3 I	–0.4	–0.5	ns
T_{OSSTL3_II}		SSTL3 II	–0.9	–1.1	ns
T_{OCTT}		CTT	–0.5	–0.6	ns
T_{OAGP}		AGP	–0.8	–1.0	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.

XC2S50 Device Pinouts

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
GND	-	P143	P1	GND*	-
TMS	-	P142	P2	D3	-
I/O	7	P141	P3	C2	149
I/O	7	-	-	A2	152
I/O	7	P140	P4	B1	155
I/O	7	-	-	E3	158
I/O	7	-	P5	D2	161
GND	-	-	-	GND*	-
I/O, V_{REF}	7	P139	P6	C1	164
I/O	7	-	P7	F3	167
I/O	7	-	-	E2	170
I/O	7	P138	P8	E4	173
I/O	7	P137	P9	D1	176
I/O	7	P136	P10	E1	179
GND	-	P135	P11	GND*	-
V_{CCO}	7	-	P12	V_{CCO} Bank 7*	-
V_{CCINT}	-	-	P13	V_{CCINT}*	-
I/O	7	P134	P14	F2	182
I/O	7	P133	P15	G3	185
I/O	7	-	-	F1	188
I/O	7	-	P16	F4	191
I/O	7	-	P17	F5	194
I/O	7	-	P18	G2	197
GND	-	-	P19	GND*	-
I/O, V_{REF}	7	P132	P20	H3	200
I/O	7	P131	P21	G4	203
I/O	7	-	-	H2	206
I/O	7	P130	P22	G5	209
I/O	7	-	P23	H4	212
I/O, IRDY(1)	7	P129	P24	G1	215
GND	-	P128	P25	GND*	-
V_{CCO}	7	P127	P26	V_{CCO} Bank 7*	-
V_{CCO}	6	P127	P26	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P126	P27	J2	218
V_{CCINT}	-	P125	P28	V_{CCINT}*	-
I/O	6	P124	P29	H1	224
I/O	6	-	-	J4	227
I/O	6	P123	P30	J1	230
I/O, V_{REF}	6	P122	P31	J3	233

XC2S50 Device Pinouts *(Continued)*

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
GND	-	-	P32	GND*	-
I/O	6	-	P33	K5	236
I/O	6	-	P34	K2	239
I/O	6	-	P35	K1	242
I/O	6	-	-	K3	245
I/O	6	P121	P36	L1	248
I/O	6	P120	P37	L2	251
V_{CCINT}	-	-	P38	V_{CCINT}*	-
V_{CCO}	6	-	P39	V_{CCO} Bank 6*	-
GND	-	P119	P40	GND*	-
I/O	6	P118	P41	K4	254
I/O	6	P117	P42	M1	257
I/O	6	P116	P43	L4	260
I/O	6	-	-	M2	263
I/O	6	-	P44	L3	266
I/O, V_{REF}	6	P115	P45	N1	269
GND	-	-	-	GND*	-
I/O	6	-	P46	P1	272
I/O	6	-	-	L5	275
I/O	6	P114	P47	N2	278
I/O	6	-	-	M4	281
I/O	6	P113	P48	R1	284
I/O	6	P112	P49	M3	287
M1	-	P111	P50	P2	290
GND	-	P110	P51	GND*	-
M0	-	P109	P52	N3	291
V_{CCO}	6	P108	P53	V_{CCO} Bank 6*	-
V_{CCO}	5	P107	P53	V_{CCO} Bank 5*	-
M2	-	P106	P54	R3	292
I/O	5	-	-	N5	299
I/O	5	P103	P57	T2	302
I/O	5	-	-	P5	305
I/O	5	-	P58	T3	308
GND	-	-	-	GND*	-
I/O, V_{REF}	5	P102	P59	T4	311
I/O	5	-	P60	M6	314
I/O	5	-	-	T5	317
I/O	5	P101	P61	N6	320
I/O	5	P100	P62	R5	323

Additional XC2S50 Package Pins *(Continued)*

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

11/02/00

FG256

V_{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V_{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V_{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V_{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V_{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V_{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V_{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V_{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V_{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

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XC2S100 Device Pinouts

XC2S100 Pad Name						
Function	Bank	TQ144	PQ208	FG256	FG456	Bndry Scan
GND	-	P143	P1	GND*	GND*	-
TMS	-	P142	P2	D3	D3	-
I/O	7	P141	P3	C2	B1	185
I/O	7	-	-	A2	F5	191
I/O	7	P140	P4	B1	D2	194
I/O	7	-	-	-	E3	197
I/O	7	-	-	E3	G5	200
I/O	7	-	P5	D2	F3	203
GND	-	-	-	GND*	GND*	-
V_{CCO}	7	-	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P139	P6	C1	E2	206
I/O	7	-	P7	F3	E1	209
I/O	7	-	-	E2	H5	215
I/O	7	P138	P8	E4	F2	218
I/O	7	-	-	-	F1	221
I/O, V_{REF}	7	P137	P9	D1	H4	224
I/O	7	P136	P10	E1	G1	227
GND	-	P135	P11	GND*	GND*	-
V_{CCO}	7	-	P12	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCINT}	-	-	P13	V_{CCINT}*	V_{CCINT}*	-
I/O	7	P134	P14	F2	H3	230
I/O	7	P133	P15	G3	H2	233
I/O	7	-	-	F1	J5	236
I/O	7	-	P16	F4	J2	239
I/O	7	-	P17	F5	K5	245
I/O	7	-	P18	G2	K1	248
GND	-	-	P19	GND*	GND*	-
I/O, V_{REF}	7	P132	P20	H3	K3	251
I/O	7	P131	P21	G4	K4	254
I/O	7	-	-	H2	L6	257
I/O	7	P130	P22	G5	L1	260
I/O	7	-	P23	H4	L4	266
I/O, IRDY(1)	7	P129	P24	G1	L3	269
GND	-	P128	P25	GND*	GND*	-
V_{CCO}	7	P127	P26	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCO}	6	P127	P26	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P126	P27	J2	M1	272
V_{CCINT}	-	P125	P28	V_{CCINT}*	V_{CCINT}*	-
I/O	6	P124	P29	H1	M3	281
I/O	6	-	-	J4	M4	284
I/O	6	P123	P30	J1	M5	287
I/O, V_{REF}	6	P122	P31	J3	N2	290
GND	-	-	P32	GND*	GND*	-
I/O	6	-	P33	K5	N3	293
I/O	6	-	P34	K2	N4	296
I/O	6	-	P35	K1	P2	302
I/O	6	-	-	K3	P4	305
I/O	6	P121	P36	L1	P3	308
I/O	6	P120	P37	L2	R2	311

XC2S200 Device Pinouts

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	257
I/O	7	-	-	E4	263
I/O	7	-	-	C1	266
I/O	7	-	A2	F5	269
GND	-	-	GND*	GND*	-
I/O, V_{REF}	7	P4	B1	D2	272
I/O	7	-	-	E3	275
I/O	7	-	-	F4	281
GND	-	-	GND*	GND*	-
I/O	7	-	E3	G5	284
I/O	7	P5	D2	F3	287
GND	-	-	GND*	GND*	-
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P6	C1	E2	290
I/O	7	P7	F3	E1	293
I/O	7	-	-	G4	296
I/O	7	-	-	G3	299
I/O	7	-	E2	H5	302
GND	-	-	GND*	GND*	-
I/O	7	P8	E4	F2	305
I/O	7	-	-	F1	308
I/O, V_{REF}	7	P9	D1	H4	314
I/O	7	P10	E1	G1	317
GND	-	P11	GND*	GND*	-
V_{CCO}	7	P12	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCINT}	-	P13	V_{CCINT}*	V_{CCINT}*	-
I/O	7	P14	F2	H3	320
I/O	7	P15	G3	H2	323
I/O	7	-	-	J4	326
I/O	7	-	-	H1	329
I/O	7	-	F1	J5	332
GND	-	-	GND*	GND*	-
I/O	7	P16	F4	J2	335
I/O	7	-	-	J3	338
I/O	7	-	-	J1	341
I/O	7	P17	F5	K5	344
I/O	7	P18	G2	K1	347
GND	-	P19	GND*	GND*	-

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P20	H3	K3	350
I/O	7	P21	G4	K4	353
I/O	7	-	-	K2	359
I/O	7	-	H2	L6	362
I/O	7	P22	G5	L1	365
I/O	7	-	-	L5	368
I/O	7	P23	H4	L4	374
I/O, IRDY(1)	7	P24	G1	L3	377
GND	-	P25	GND*	GND*	-
V_{CCO}	7	P26	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCO}	6	P26	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P27	J2	M1	380
V_{CCINT}	-	P28	V_{CCINT}*	V_{CCINT}*	-
I/O	6	-	-	M6	389
I/O	6	P29	H1	M3	392
I/O	6	-	J4	M4	395
I/O	6	-	-	N1	398
I/O	6	P30	J1	M5	404
I/O, V_{REF}	6	P31	J3	N2	407
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	410
I/O	6	P34	K2	N4	413
I/O	6	-	-	P1	416
I/O	6	-	-	N5	419
I/O	6	P35	K1	P2	422
GND	-	-	GND*	GND*	-
I/O	6	-	K3	P4	425
I/O	6	-	-	R1	428
I/O	6	-	-	P5	431
I/O	6	P36	L1	P3	434
I/O	6	P37	L2	R2	437
V_{CCINT}	-	P38	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	6	P39	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	440
I/O, V_{REF}	6	P42	M1	R4	443

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V_{CCO}	3	P117	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
V_{CCINT}	-	P118	V_{CCINT}*	V_{CCINT}*	-
I/O (D5)	3	P119	M16	R21	833
I/O	3	P120	K14	P18	836
I/O	3	-	-	R22	839
I/O	3	-	-	P19	842
I/O	3	-	L16	P20	845
GND	-	-	GND*	GND*	-
I/O	3	P121	K13	P21	848
I/O	3	-	-	N19	851
I/O	3	-	-	P22	854
I/O	3	P122	L15	N18	857
I/O	3	P123	K12	N20	860
GND	-	P124	GND*	GND*	-
V_{CCO}	3	-	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
I/O, V_{REF}	3	P125	K16	N21	863
I/O (D4)	3	P126	J16	N22	866
I/O	3	-	-	M17	872
I/O	3	-	J14	M19	875
I/O	3	P127	K15	M20	878
I/O	3	-	-	M18	881
V_{CCINT}	-	P128	V_{CCINT}*	V_{CCINT}*	-
I/O, TRDY(1)	3	P129	J15	M22	890
V_{CCO}	3	P130	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
V_{CCO}	2	P130	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	P131	GND*	GND*	-
I/O, IRDY(1)	2	P132	H16	L20	893
I/O	2	P133	H14	L17	896
I/O	2	-	-	L18	902
I/O	2	P134	H15	L21	905
I/O	2	-	J13	L22	908
I/O	2	-	-	K19	911
I/O (D3)	2	P135	G16	K20	917
I/O, V_{REF}	2	P136	H13	K21	920
V_{CCO}	2	-	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	P137	GND*	GND*	-
I/O	2	P138	G14	K22	923
I/O	2	P139	G15	J21	926

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	2	-	-	K18	929
I/O	2	-	-	J20	932
I/O	2	P140	G12	J18	935
GND	-	-	GND*	GND*	-
I/O	2	-	F16	J22	938
I/O	2	-	-	J19	941
I/O	2	-	-	H21	944
I/O	2	P141	G13	H19	947
I/O (D2)	2	P142	F15	H20	950
V_{CCINT}	-	P143	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	2	P144	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	P145	GND*	GND*	-
I/O (D1)	2	P146	E16	H22	953
I/O, V_{REF}	2	P147	F14	H18	956
I/O	2	-	-	G21	962
I/O	2	P148	D16	G18	965
GND	-	-	GND*	GND*	-
I/O	2	-	F12	G20	968
I/O	2	-	-	G19	971
I/O	2	-	-	F22	974
I/O	2	P149	E15	F19	977
I/O, V_{REF}	2	P150	F13	F21	980
V_{CCO}	2	-	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	-	GND*	GND*	-
I/O	2	P151	E14	F20	983
I/O	2	-	C16	F18	986
GND	-	-	GND*	GND*	-
I/O	2	-	-	E22	989
I/O	2	-	-	E21	995
I/O, V_{REF}	2	P152	E13	D22	998
GND	-	-	GND*	GND*	-
I/O	2	-	B16	E20	1001
I/O	2	-	-	D21	1004
I/O	2	-	-	C22	1007
I/O (DIN, D0)	2	P153	D14	D20	1013
I/O (DOUT, BUSY)	2	P154	C15	C21	1016
CCLK	2	P155	D15	B22	1019
V_{CCO}	2	P156	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-