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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	260
Number of Gates	150000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s150-5fgg456i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Figure 4: Spartan-II CLB Slice (two identical slices in each CLB)

Storage Elements

Storage elements in the Spartan-II FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-II FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-II FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing," page 12. Each Spartan-II FPGA BUFT has an independent 3-state control pin and an independent input pin.

Block RAM

Spartan-II FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks.

Table 5: Spartan-II Block RAM Amounts

Spartan-II Device	# of Blocks	Total Block RAM Bits
XC2S15	4	16K
XC2S30	6	24K
XC2S50	8	32K
XC2S100	10	40K
XC2S150	12	48K
XC2S200	14	56K

Each block RAM cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.



Figure 5: Dual-Port Block RAM

Table 6 shows the depth and width aspect ratios for the block RAM.

Table	6 [.]	Block	RAM	Port	Aspect	Ratios
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Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-II FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK. Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is 2²⁰-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until INIT pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.



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Notes:

1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 15: Master/Slave Serial Configuration Circuit Diagram

Design Considerations

This section contains more detailed design information on the following features:

- Delay-Locked Loop . . . see page 27
- Block RAM . . . see page 32
- Versatile I/O . . . see page 36

Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Primitives

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.



Figure 22: Simplified DLL Macro BUFGDLL



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Using Block RAM Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block RAM memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block RAM memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Block RAM memory supports two operating modes.

- Read Through
- Write Back

Read Through (One Clock Edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (One Clock Edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

Block RAM Characteristics

- 1. All inputs are registered with the port clock and have a setup to clock timing specification.
- 2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
- 3. The block RAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT cells in the CLBs are still available with this function.
- 4. The ports are completely independent from each other (*i.e.*, clocking, control, address, read/write function, and data width) without arbitration.
- 5. A write operation requires only one clock edge.
- 6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

Library Primitives

Figure 31 and Figure 32 show the two generic library block RAM primitives. Table 11 describes all of the available primitives for synthesis and simulation.



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Figure 32: Single-Port Block RAM Memory

Table 11: Available Library Primitives

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16

PCI — Peripheral Component Interface

The Peripheral Component Interface (PCI) standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a push-pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}). I/Os configured for the PCI, 33 MHz, 5V standard are also 5V-tolerant.

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic (GTL) standard is a high-speed bus standard (JESD8.3). Xilinx has implemented the terminated variation of this standard. This standard requires a differential amplifier input buffer and an open-drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus (GTL+) standard is a high-speed bus standard (JESD8.3).

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed, 1.5V bus standard (EIA/JESD 8-6). This standard has four variations or classes. Versatile I/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V (SSTL3) standard is a general purpose 3.3V memory bus standard (JESD8-8). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V (SSTL2) standard is a general purpose 2.5V memory bus standard (JESD8-9). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated (CTT) standard is a 3.3V memory bus standard (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with processors for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

Library Primitives

The Xilinx library includes an extensive list of primitives designed to provide support for the variety of Versatile I/O features. Most of these primitives represent variations of the five generic Versatile I/O primitives:

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

These primitives are available with various extensions to define the desired I/O standard. However, it is recommended that customers use a a property or attribute on the generic primitive to specify the I/O standard. See "Versatile I/O Properties".

IBUF

Signals used as inputs to the Spartan-II device must source an input buffer (IBUF) via an external input port. The generic IBUF primitive appears in Figure 35. The assumed standard is LVTTL when the generic IBUF has no specified extension or property.



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Figure 35: Input Buffer (IBUF) Primitive

When the IBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF primitive names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24). The default is slew rate limited with 12 mA drive.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. Table 17 summarizes the output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 17: Output Standards Compatibility Requirements

Rule 1	Only outputs with standards which share compatible $\rm V_{\rm CCO}$ may be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a $\rm V_{\rm CCO}$
V _{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 39, typically implements 3-state outputs or bidirectional I/O.

With no extension or property specified for the generic OBUFT primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT primitive names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).



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Figure 39: 3-State Output Buffer Primitive (OBUFT

The Versatile I/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF primitive for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 40.

With no extension or property specified for the generic IOBUF primitive, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF primitive names is as follows:

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).





When the IOBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36, page 39 for a representation of the Spartan-II FPGA I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

IOB Flip-Flop/Latch Property

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified:

map -pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each Versatile I/O primitive with the location constraint LOC attached to the Versatile I/O primitive. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

LOC=A42 LOC=P37

Output Slew Rate Property

In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

Output Drive Strength Property

For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE=

property. This property could have one of the following seven values.

DRIVE=2 DRIVE=4 DRIVE=6 DRIVE=8 DRIVE=12 (Default) DRIVE=16 DRIVE=24

Design Considerations

Reference Voltage (V_{RFF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{RFF}). Provide the V_{RFF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{RFF} banks internally. See Figure 36, page 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{RFF} input.

Within each V_{REF} bank, any input buffers that require a V_{RFF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage (V_{CCO}) . As a result each device can often have to support multiple output drive source voltages.

The V_{CCO} supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined $V_{\mbox{\scriptsize CCO}}$ supply. The TQ144 and the CS144 packages provide four independent V_{CCO} supplies. The FG256 and the FG456 provide eight independent V_{CCO} supplies.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques:

None Series Parallel (Shunt) Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 41.





Unterminated Output Driving a Parallel Terminated Input





Series Terminated Output Driving

Series-Parallel Terminated Output

Series Terminated Output



Driving a Parallel Terminated Input VTT





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Figure 41: Overview of Standard Input and Output **Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

SSTL3 Class I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 47. DC voltage specifications appear in Table 25 for the SSTL3_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

SSTL3 Class I



Figure 47: Terminated SSTL3 Class I

Table 2	25:	SSTL3_	I Voltage	Speci	fications
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Parameter	Min	Тур	Max
V _{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \ge V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} \leq V_{REF} - 0.2$	-0.3(2)	1.3	1.5
$V_{OH} \ge V_{REF} + 0.6$	1.9	-	-
$V_{OL} \le V_{REF} - 0.6$	-	-	1.1
I _{OH} at V _{OH} (mA)	-8	-	-
I _{OL} at V _{OL} (mA)	8	-	-

Notes:

1. V_{IH} maximum is V_{CCO} + 0.3.

2. V_{IL} minimum does not conform to the formula.

SSTL3 Class II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 48. DC voltage specifications appear in Table 26 for the SSTL3_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.



Figure 48: Terminated SSTL3 Class II

Table 26: SSTL3_II Voltage Specifications

Parameter	Min	Тур	Max
V _{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \ge V_{REF} + 0.2$	1.5	1.7	3.9 ⁽¹⁾
$V_{IL} \leq V_{REF} - 0.2$	-0.3 ⁽²⁾	1.3	1.5
$V_{OH} \ge V_{REF} + 0.8$	2.1	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.9
I _{OH} at V _{OH} (mA)	-16	-	-
I _{OL} at V _{OL} (mA)	16	-	-

Notes:

1. V_{IH} maximum is V_{CCO} + 0.3

2. V_{IL} minimum does not conform to the formula

Input/Output		V _{IL}	V	н	V _{OL}	V _{OH}	I _{OL}	I _{ОН}
Standard	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
CTT	-0.5	V _{REF} – 0.2	V _{REF} + 0.2	3.6	V _{REF} – 0.4	V _{REF} + 0.4	8	-8
AGP	-0.5	V _{REF} – 0.2	V _{REF} + 0.2	3.6	10% V _{CCO}	90% V _{CCO}	Note (2)	Note (2)

Notes:

1. V_{OL} and V_{OH} for lower drive currents are sample tested.

2. Tested according to the relevant specifications.

Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, with DLL (Pin-to-Pin)⁽¹⁾

			S	peed Grad	le	
			All	-6	-5	
Symbol	Description	Device	Min	Max	Max	Units
T _{ICKOFDLL}	Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, <i>with</i> DLL.	All		2.9	3.3	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

- Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
- 3. DLL output jitter is already included in the timing calculation.
- 4. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)⁽¹⁾

			All	-6	-5	
Symbol	Description	Device	Min	Max	Max	Units
T _{ICKOF}	Global clock input to output delay	XC2S15		4.5	5.4	ns
	using output flip-flop for LVTTL,	XC2S30		4.5	5.4	ns
	12 mA, fast slew rate, <i>without</i> DLL.	XC2S50		4.5	5.4	ns
		XC2S100		4.6	5.5	ns
		XC2S150		4.6	5.5	ns
		XC2S200		4.7	5.6	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

- Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
- For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59.

		-6		-5		
Symbol	Description	Min	Max	Min	Max	Units
Propagation Delays	5					
T _{IOOP}	O input to pad	-	2.9	-	3.4	ns
T _{IOOLP}	O input to pad via transparent latch	-	3.4	-	4.0	ns
3-state Delays		1				
T _{IOTHZ}	T input to pad high-impedance ⁽¹⁾	-	2.0	-	2.3	ns
T _{IOTON}	T input to valid data on pad	-	3.0	-	3.6	ns
T _{IOTLPHZ}	T input to pad high impedance via transparent latch ⁽¹⁾	-	2.5	-	2.9	ns
T _{IOTLPON}	T input to valid data on pad via transparent latch	-	3.5	-	4.2	ns
T _{GTS}	GTS to pad high impedance ⁽¹⁾	-	5.0	-	5.9	ns
Sequential Delays		1	L	I		
T _{IOCKP}	Clock CLK to pad	-	2.9	-	3.4	ns
Т _{ЮСКНZ}	Clock CLK to pad high impedance (synchronous) ⁽¹⁾	-	2.3	-	2.7	ns
T _{IOCKON}	Clock CLK to valid data on pad (synchronous)	-	3.3	-	4.0	ns
Setup/Hold Times	with Respect to Clock CLK ⁽²⁾	1	l.			
TIOOCK / TIOCKO	O input	1.1/0	-	1.3/0	-	ns
T _{IOOCECK} /	OCE input	0.9 / 0.01	-	0.9/0.01	-	ns
TIOCKOCE						
T _{IOSRCKO} /	SR input (OFF)	1.2/0	-	1.3/0	-	ns
TIOCKOSR				/ -		
TIOTCK / TIOCKT	3-state setup times, T input	0.8/0	-	0.9/0	-	ns
Т _{ІОТСЕСК} /	3-state setup times, TCE input	1.0/0	-	1.0/0	-	ns
		11/0		10/0		
	3-state setup times, SK input (TFF)	1.170	-	1.2/0	-	ns
Set/Reset Delays						
	SR input to pad (asynchronous)	_	37	_	44	ns
	SR input to pad high impedance (asynchronous) ⁽¹⁾	-	3.1	-	37	ns
	SR input to valid data on pad (asynchronous)	-	4 1	-	49	ns
	GSR to pad	_	9.1	_	11 7	ns
' IOGSRQ	OUN ID Pau	-	9.9	-	11.7	115

Notes:

1. Three-state turn-off delays should not be adjusted.

2. A zero hold time listing indicates no hold time or a negative hold time.

Clock Distribution Guidelines⁽¹⁾

		Speed Grade		
		-6	-5	
Symbol	Description	Max Max		Units
GCLK Clock Skew			·	<u>.</u>
T _{GSKEWIOB}	Global clock skew between IOB flip-flops	0.13	0.14	ns

Notes:

1. These clock distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

T_{GPIO} is specified for LVTTL levels. For other standards, adjust T_{GPIO} with the values shown in "I/O Standard Global Clock Input Adjustments".

		Speed		
		-6	-5	
Symbol	Description	Max	Max	Units
GCLK IOB and But	ifer			
T _{GPIO}	Global clock pad to output	0.7	0.8	ns
T _{GIO}	Global clock buffer I input to O output	0.7	0.8	ns

I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

			Speed Grade						
Symbol	Description	Standard	-6	-5	Units				
Data Input Delay Adjustments									
T _{GPLVTTL}	Standard-specific global clock	LVTTL	0	0	ns				
T _{GPLVCMOS2}	input delay adjustments	LVCMOS2	-0.04	-0.05	ns				
T _{GPPCI33_3}		PCI, 33 MHz, 3.3V	-0.11	-0.13	ns				
T _{GPPCI33_5}	-	PCI, 33 MHz, 5.0V	0.26	0.30	ns				
T _{GPPCI66_3}		PCI, 66 MHz, 3.3V	-0.11	-0.13	ns				
T _{GPGTL}		GTL	0.80	0.84	ns				
T _{GPGTLP}		GTL+	0.71	0.73	ns				
T _{GPHSTL}		HSTL	0.63	0.64	ns				
T _{GPSSTL2}		SSTL2	0.52	0.51	ns				
T _{GPSSTL3}		SSTL3	0.56	0.55	ns				
T _{GPCTT}		CTT	0.62	0.62	ns				
T _{GPAGP}		AGP	0.54	0.53	ns				

Notes:

1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

			Speed Grade			
			-6		·5	
Symbol	Description	Min	Max	Min	Max	Units
F _{CLKINHF}	Input clock frequency (CLKDLLHF)	60	200	60	180	MHz
F _{CLKINLF}	Input clock frequency (CLKDLL)	25	100	25	90	MHz
T _{DLLPWHF}	Input clock pulse width (CLKDLLHF)	2.0	-	2.4	-	ns
T _{DLLPWLF}	Input clock pulse width (CLKDLL)	2.5	-	3.0	-	ns

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Figure 52, page 63, provides definitions for various parameters in the table below.

			CLKE	DLLHF	CLK	DLL	
Symbol	Description		Min	Max	Min	Max	Units
T _{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T _{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T _{LOCK}	Time required for DLL to acquire lock	> 60 MHz	-	20	-	20	μs
		50-60 MHz	-	-	-	25	μs
		40-50 MHz	-	-	-	50	μs
		30-40 MHz	-	-	-	90	μs
		25-30 MHz	-	-	-	120	μs
T _{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock o	utput ⁽¹⁾	-	±60	-	±60	ps
T _{PHIO}	Phase offset between CLKIN and CLKO ⁽²⁾		-	±100	-	±100	ps
T _{PHOO}	Phase offset between clock outputs on the DLL ⁽³⁾		-	±140	-	±140	ps
T _{PHIOM}	Maximum phase difference between CLKIN and CLKO ⁽⁴⁾		-	±160	-	±160	ps
T _{PHOOM}	Maximum phase difference between clock output	uts on the DLL ⁽⁵⁾	-	±200	-	±200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.

2. Phase Offset between CLKIN and CLKO is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.

3. Phase Offset between Clock Outputs on the DLL is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.

4. Maximum Phase Difference between CLKIN an CLKO is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).

5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

Block RAM Switching Characteristics

		Speed Grade				
		-6			5	
Symbol	Description	Min	Max	Min	Max	Units
Sequential Delays		<u>.</u>	<u>.</u>	<u>.</u>	<u>.</u>	<u></u>
Т _{ВСКО}	Clock CLK to DOUT output	-	3.4	-	4.0	ns
Setup/Hold Times	with Respect to Clock CLK ⁽¹⁾					
T _{BACK} / T _{BCKA}	ADDR inputs	1.4 / 0	-	1.4 / 0	-	ns
T _{BDCK} / T _{BCKD}	DIN inputs	1.4 / 0	-	1.4 / 0	-	ns
T _{BECK} / T _{BCKE}	EN inputs	2.9 / 0	-	3.2 / 0	-	ns
T _{BRCK} / T _{BCKR}	RST input	2.7 / 0	-	2.9/0	-	ns
T _{BWCK} / T _{BCKW}	WEN input	2.6 / 0	-	2.8 / 0	-	ns
Clock CLK						
T _{BPWH}	Minimum pulse width, High	-	1.9	-	1.9	ns
T _{BPWL}	Minimum pulse width, Low	-	1.9	-	1.9	ns
T _{BCCS}	CLKA -> CLKB setup time for different ports	-	3.0	-	4.0	ns

Notes:

1. A zero hold time listing indicates no hold time or a negative hold time.

TBUF Switching Characteristics

		Speed	d Grade	
		-6	-5	-
Symbol Description		Max	Max	Units
Combinatorial Delay	rs			<u>.</u>
T _{IO}	IN input to OUT output	0	0	ns
T _{OFF}	TRI input to OUT output high impedance	0.1	0.2	ns
T _{ON}	TRI input to valid data on OUT output	0.1	0.2	ns

JTAG Test Access Port Switching Characteristics

			Speed	l Grade		
		-(6		5	
Symbol	Description	Min	Max	Min	Max	Units
Setup and Hold Time	s with Respect to TCK					
T _{TAPTCK /} T _{TCKTAP}	TMS and TDI setup and hold times	4.0/2.0	-	4.0/2.0	-	ns
Sequential Delays	-	· · ·				
T _{TCKTDO}	Output delay from clock TCK to output TDO	-	11.0	-	11.0	ns
FTCK	Maximum TCK clock frequency	-	33	-	33	MHz

Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan[®]-II device. They follow the pad locations around the die, and include Boundary Scan register locations.

XC2S15 Device Pinouts

XC2S15 Pad Name					Bndry
Function	Bank	VQ100	TQ144	CS144	Scan
GND	-	P1	P143	A1	-
TMS	-	P2	P142	B1	-
I/O	7	P3	P141	C2	77
I/O	7	-	P140	C1	80
I/O, V _{REF}	7	P4	P139	D4	83
I/O	7	P5	P137	D2	86
I/O	7	P6	P136	D1	89
GND	-	-	P135	E4	-
I/O	7	P7	P134	E3	92
I/O	7	-	P133	E2	95
I/O, V _{REF}	7	P8	P132	E1	98
I/O	7	P9	P131	F4	101
I/O	7	-	P130	F3	104
I/O, IRDY ⁽¹⁾	7	P10	P129	F2	107
GND	-	P11	P128	F1	-
V _{CCO}	7	P12	P127	G2	-
V _{CCO}	6	P12	P127	G2	-
I/O, TRDY ⁽¹⁾	6	P13	P126	G1	110
V _{CCINT}	-	P14	P125	G3	-
I/O	6	-	P124	G4	113
I/O	6	P15	P123	H1	116
I/O, V _{REF}	6	P16	P122	H2	119
I/O	6	-	P121	H3	122
I/O	6	P17	P120	H4	125
GND	-	-	P119	J1	-
I/O	6	P18	P118	J2	128
I/O	6	P19	P117	J3	131
I/O, V _{REF}	6	P20	P115	K1	134
I/O	6	-	P114	K2	137
I/O	6	P21	P113	K3	140
I/O	6	P22	P112	L1	143
M1	-	P23	P111	L2	146
GND	-	P24	P110	L3	-
M0	-	P25	P109	M1	147
V _{CCO}	6	P26	P108	M2	-
V _{CCO}	5	P26	P107	N1	-

XC2S15 Device Pinouts (Continued)

XC2S15 Pad Name					Bndry
Function	Bank	VQ100	TQ144	CS144	Scan
M2	-	P27	P106	N2	148
I/O	5	-	P103	K4	155
I/O, V _{REF}	5	P30	P102	L4	158
I/O	5	P31	P100	N4	161
I/O	5	P32	P99	K5	164
GND	-	-	P98	L5	-
V _{CCINT}	-	P33	P97	M5	-
I/O	5	-	P96	N5	167
I/O	5	-	P95	K6	170
I/O, V _{REF}	5	P34	P94	L6	173
I/O	5	-	P93	M6	176
V _{CCINT}	-	P35	P92	N6	-
I, GCK1	5	P36	P91	M7	185
V _{CCO}	5	P37	P90	N7	-
V _{CCO}	4	P37	P90	N7	-
GND	-	P38	P89	L7	-
I, GCK0	4	P39	P88	K7	186
I/O	4	P40	P87	N8	190
I/O	4	-	P86	M8	193
I/O, V _{REF}	4	P41	P85	L8	196
I/O	4	-	P84	K8	199
I/O	4	-	P83	N9	202
V _{CCINT}	-	P42	P82	M9	-
GND	-	-	P81	L9	-
I/O	4	P43	P80	K9	205
I/O	4	P44	P79	N10	208
I/O, V _{REF}	4	P45	P77	L10	211
I/O	4	-	P76	N11	214
I/O	4	P46	P75	M11	217
I/O	4	P47	P74	L11	220
GND	-	P48	P73	N12	-
DONE	3	P49	P72	M12	223
V _{CCO}	4	P50	P71	N13	-
V _{CCO}	3	P50	P70	M13	-
PROGRAM	-	P51	P69	L12	226
I/O (INIT)	3	P52	P68	L13	227
I/O (D7)	3	P53	P67	K10	230
I/O	3	-	P66	K11	233
I/O, V _{REF}	3	P54	P65	K12	236
I/O	3	P55	P63	J10	239
I/O (D6)	3	P56	P62	J11	242

XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name					Bndry
Function	Bank	TQ144	PQ208	FG256	Scan
I/O	0	-	-	D8	83
I/O	0	-	P188	A6	86
I/O, V _{REF}	0	P12	P189	B7	89
GND	-	-	P190	GND*	-
I/O	0	-	P191	C8	92
I/O	0	-	P192	D7	95
I/O	0	-	P193	E7	98
I/O	0	P11	P194	C7	104
I/O	0	P10	P195	B6	107
V _{CCINT}	-	P9	P196	V _{CCINT} *	-
V _{CCO}	0	-	P197	V _{CCO} Bank 0*	-
GND	-	P8	P198	GND*	-
I/O	0	P7	P199	A5	110
I/O	0	P6	P200	C6	113
I/O	0	-	P201	B5	116
I/O	0	-	-	D6	119
I/O	0	-	P202	A4	122
I/O, V _{REF}	0	P5	P203	B4	125
GND	-	-	-	GND*	-
I/O	0	-	P204	E6	128
I/O	0	-	-	D5	131
I/O	0	P4	P205	A3	134
I/O	0	-	-	C5	137
I/O	0	P3	P206	B3	140
TCK	-	P2	P207	C4	-
V _{CCO}	0	P1	P208	V _{CCO} Bank 0*	-
V _{CCO}	7	P144	P208	V _{CCO} Bank 7*	-

04/18/01

Notes:

- 1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
- Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
- 3. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S50 Package Pins

TQ1	44
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Not Connected Pins						
P104	P105	-	-	-	-	
11/02/00						

Additional XC2S50 Package Pins (Continued)

PQ208

Not Connected Pins						
P55	P56	-	-	-	-	
11/02/00						

FG256

V _{CCINT} Pins							
C3	C14	D4	D13	E5	E12		
M5	M12	N4	N13	P3	P14		
		V _{CCO} Ba	nk 0 Pins				
E8	F8	-	-	-	-		
		V _{CCO} Ba	nk 1 Pins				
E9	F9	-	-	-	-		
		V _{CCO} Ba	nk 2 Pins				
H11	H12	-	-	-	-		
		V _{CCO} Ba	nk 3 Pins				
J11	J12	-	-	-	-		
		V _{CCO} Ba	nk 4 Pins				
L9	M9	-	-	-	-		
		V _{CCO} Ba	nk 5 Pins				
L8	M8	-	-	-	-		
		V _{CCO} Ba	nk 6 Pins				
J5	J6	-	-	-	-		
		V _{CCO} Ba	nk 7 Pins				
H5	H6	-	-	-	-		
		GND	Pins				
A1	A16	B2	B15	F6	F7		
F10	F11	G6	G7	G8	G9		
G10	G11	H7	H8	H9	H10		
J7	J8	J9	J10	K6	K7		
K8	K9	K10	K11	L6	L7		
L10	L11	R2	R15	T1	T16		
		Not Conne	ected Pins	-			
P4	R4	-	-	-	-		
11/00/00							

11/02/00

XC2S100 Device Pinouts

XC2S100 Pad Name						Bndry
Function	Bank	TQ144	PQ208	FG256	FG456	Scan
GND	-	P143	P1	GND*	GND*	-
TMS	-	P142	P2	D3	D3	-
I/O	7	P141	P3	C2	B1	185
I/O	7	-	-	A2	F5	191
I/O	7	P140	P4	B1	D2	194
I/O	7	-	-	-	E3	197
I/O	7	-	-	E3	G5	200
I/O	7	-	P5	D2	F3	203
GND	-	-	-	GND*	GND*	-
V _{CCO}	7	-	-	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
I/O, V _{REF}	7	P139	P6	C1	E2	206

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						Pndny
Function	Bank	TQ144	PQ208	FG256	FG456	Scan
I/O	7	-	P7	F3	E1	209
I/O	7	-	-	E2	H5	215
I/O	7	P138	P8	E4	F2	218
I/O	7	-	-	-	F1	221
I/O, V _{REF}	7	P137	P9	D1	H4	224
I/O	7	P136	P10	E1	G1	227
GND	-	P135	P11	GND*	GND*	-
V _{CCO}	7	-	P12	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCINT}	-	-	P13	V _{CCINT} *	V _{CCINT} *	-
I/O	7	P134	P14	F2	H3	230
I/O	7	P133	P15	G3	H2	233
I/O	7	-	-	F1	J5	236
I/O	7	-	P16	F4	J2	239
I/O	7	-	P17	F5	K5	245
I/O	7	-	P18	G2	K1	248
GND	-	-	P19	GND*	GND*	-
I/O, V _{REF}	7	P132	P20	H3	K3	251
I/O	7	P131	P21	G4	K4	254
I/O	7	-	-	H2	L6	257
I/O	7	P130	P22	G5	L1	260
I/O	7	-	P23	H4	L4	266
I/O, IRDY ⁽¹⁾	7	P129	P24	G1	L3	269
GND	-	P128	P25	GND*	GND*	-
V _{CCO}	7	P127	P26	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCO}	6	P127	P26	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
I/O, TRDY ⁽¹⁾	6	P126	P27	J2	M1	272
V _{CCINT}	-	P125	P28	V_{CCINT}^{*}	V_{CCINT}^{*}	-
I/O	6	P124	P29	H1	М3	281
I/O	6	-	-	J4	M4	284
I/O	6	P123	P30	J1	M5	287
I/O, V _{REF}	6	P122	P31	J3	N2	290
GND	-	-	P32	GND*	GND*	-
I/O	6	-	P33	K5	N3	293
I/O	6	-	P34	K2	N4	296
I/O	6	-	P35	K1	P2	302
I/O	6	-	-	K3	P4	305
I/O	6	P121	P36	L1	P3	308
I/O	6	P120	P37	L2	R2	311

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						Bndry
Function	Bank	TQ144	PQ208	FG256	FG456	Scan
I/O	2	-	-	F12	G20	695
I/O	2	-	P149	E15	F19	701
I/O, V _{REF}	2	P41	P150	F13	F21	704
V _{CCO}	2	-	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	-	-	GND*	GND*	-
I/O	2	-	P151	E14	F20	707
I/O	2	-	-	C16	F18	710
I/O	2	-	-	-	E21	713
I/O	2	P40	P152	E13	D22	716
I/O	2	-	-	B16	E20	719
I/O (DIN, D0)	2	P39	P153	D14	D20	725
I/O (DOUT, BUSY)	2	P38	P154	C15	C21	728
CCLK	2	P37	P155	D15	B22	731
V _{CCO}	2	P36	P156	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
V _{CCO}	1	P35	P156	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
TDO	2	P34	P157	B14	A21	-
GND	-	P33	P158	GND*	GND*	-
TDI	-	P32	P159	A15	B20	-
I/O (CS)	1	P31	P160	B13	C19	0
I/O (WRITE)	1	P30	P161	C13	A20	3
I/O	1	-	-	C12	D17	9
I/O	1	P29	P162	A14	A19	12
I/O	1	-	-	-	B18	15
I/O	1	-	-	D12	C17	18
I/O	1	-	P163	B12	D16	21
GND	-	-	-	GND*	GND*	-
V _{CCO}	1	-	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P28	P164	C11	A18	24
I/O	1	-	P165	A13	B17	27
I/O	1	-	-	D11	D15	33
I/O	1	-	P166	A12	C16	36
I/O	1	-	-	-	D14	39
I/O, V _{REF}	1	P27	P167	E11	E14	42
I/O	1	P26	P168	B11	A16	45
GND	-	P25	P169	GND*	GND*	-

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						Bndrv
Function	Bank	TQ144	PQ208	FG256	FG456	Scan
V _{CCO}	1	-	P170	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCINT}	-	P24	P171	V_{CCINT}^{*}	V _{CCINT} *	-
I/O	1	P23	P172	A11	C15	48
I/O	1	P22	P173	C10	B15	51
I/O	1	-	-	-	F12	54
I/O	1	-	P174	B10	C14	57
I/O	1	-	P175	D10	D13	63
I/O	1	-	P176	A10	C13	66
GND	-	-	P177	GND*	GND*	-
I/O, V _{REF}	1	P21	P178	B9	B13	69
I/O	1	-	P179	E10	E12	72
I/O	1	-	-	A9	B12	75
I/O	1	P20	P180	D9	D12	78
I/O	1	P19	P181	A8	D11	84
I, GCK2	1	P18	P182	C9	A11	90
GND	-	P17	P183	GND*	GND*	-
V _{CCO}	1	P16	P184	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCO}	0	P16	P184	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
I, GCK3	0	P15	P185	B8	C11	91
V _{CCINT}	-	P14	P186	V _{CCINT} *	V_{CCINT}^{*}	-
I/O	0	P13	P187	A7	A10	101
I/O	0	-	-	D8	B10	104

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O, IRDY ⁽¹⁾	2	P132	H16	L20	767
I/O	2	P133	H14	L17	770
I/O	2	-	-	L18	773
I/O	2	P134	H15	L21	776
I/O	2	-	J13	L22	779
I/O (D3)	2	P135	G16	K20	782
I/O, V _{REF}	2	P136	H13	K21	785
V _{CCO}	2	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P137	GND*	GND*	-
I/O	2	P138	G14	K22	788
I/O	2	P139	G15	J21	791
I/O	2	-	-	J20	797
I/O	2	P140	G12	J18	800
I/O	2	-	F16	J22	803
I/O	2	-	-	J19	806
I/O	2	P141	G13	H19	812
I/O (D2)	2	P142	F15	H20	815
V _{CCINT}	-	P143	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	2	P144	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P145	GND*	GND*	-
I/O (D1)	2	P146	E16	H22	818
I/O, V _{REF}	2	P147	F14	H18	821
I/O	2	-	-	G21	824
I/O	2	P148	D16	G18	827
I/O	2	-	F12	G20	830
I/O	2	-	-	G19	833
I/O	2	-	-	F22	836
I/O	2	P149	E15	F19	839
I/O, V _{REF}	2	P150	F13	F21	842
V _{CCO}	2	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	-	GND*	GND*	-
I/O	2	P151	E14	F20	845
I/O	2	-	C16	F18	848
I/O	2	-	-	E22	851
I/O	2	-	-	E21	854
I/O	2	P152	E13	D22	857
GND	-	-	GND*	GND*	-
I/O	2	-	B16	E20	860
I/O	2	-	-	D21	863

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O	2	-	-	C22	866
I/O (DIN, D0)	2	P153	D14	D20	869
I/O (DOUT, BUSY)	2	P154	C15	C21	872
CCLK	2	P155	D15	B22	875
V _{CCO}	2	P156	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
V _{CCO}	1	P156	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
TDO	2	P157	B14	A21	-
GND	-	P158	GND*	GND*	-
TDI	-	P159	A15	B20	-
I/O (<u>CS</u>)	1	P160	B13	C19	0
I/O (WRITE)	1	P161	C13	A20	3
I/O	1	-	-	B19	6
I/O	1	-	-	C18	9
I/O	1	-	C12	D17	12
GND	-	-	GND*	GND*	-
I/O	1	P162	A14	A19	15
I/O	1	-	-	B18	18
I/O	1	-	-	E16	21
I/O	1	-	D12	C17	24
I/O	1	P163	B12	D16	27
GND	-	-	GND*	GND*	-
V _{CCO}	1	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P164	C11	A18	30
I/O	1	P165	A13	B17	33
I/O	1	-	-	E15	36
I/O	1	-	-	A17	39
I/O	1	-	D11	D15	42
I/O	1	P166	A12	C16	45
I/O	1	-	-	D14	48
I/O, V _{REF}	1	P167	E11	E14	51
I/O	1	P168	B11	A16	54
GND	-	P169	GND*	GND*	-
V _{CCO}	1	P170	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCINT}	-	P171	V _{CCINT} *	V _{CCINT} *	-
I/O	1	P172	A11	C15	57
I/O	1	P173	C10	B15	60
I/O	1	-	-	A15	66
I/O	1	-	-	F12	69