AMD Xilinx - XC2S150-5PQG208I Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	140
Number of Gates	150000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s150-5pqg208i

Revision History

Date	Version No.	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Added industrial temperature range information.
10/31/00	2.1	Removed Power down feature.
03/05/01	2.2	Added statement on PROMs.
11/01/01	2.3	Updated Product Availability chart. Minor text edits.
09/03/03	2.4	Added device part marking.
08/02/04	2.5	Added information on Pb-free packaging options and removed discontinued options.
06/13/08	2.8	Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.

Architectural Description

Spartan-II FPGA Array

The Spartan®-II field-programmable gate array, shown in Figure 2, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 2, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

Input/Output Block

The Spartan-II FPGA IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. Table 3 lists several of the standards which are supported along with the required reference, output and termination voltages needed to meet the standard.

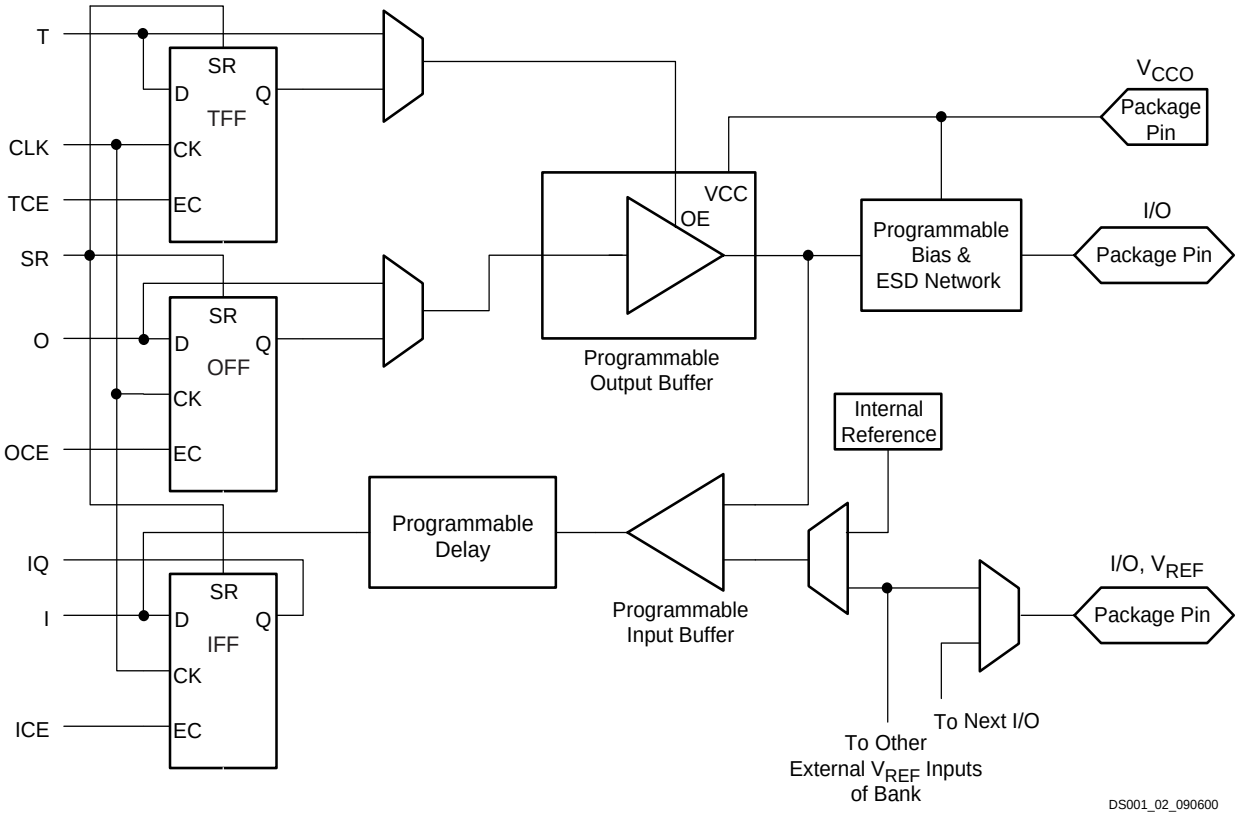


Figure 2: **Spartan-II FPGA Input/Output Block (IOB)**

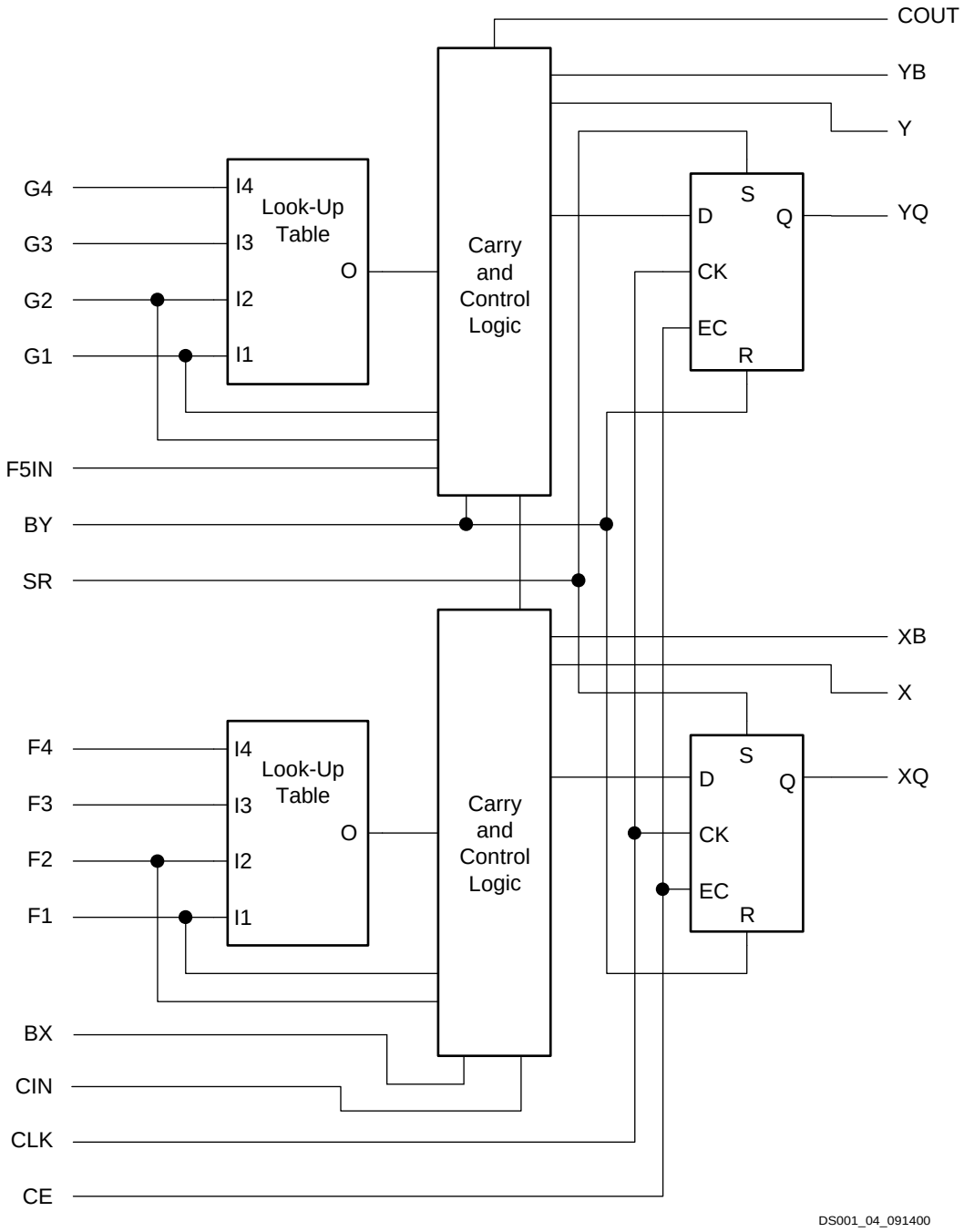


Figure 4: **Spartan-II CLB Slice** (two identical slices in each CLB)

Storage Elements

Storage elements in the Spartan-II FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-II FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-II FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing," page 12. Each Spartan-II FPGA BUFT has an independent 3-state control pin and an independent input pin.

Block RAM

Spartan-II FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks.

Table 5: **Spartan-II Block RAM Amounts**

Spartan-II Device	# of Blocks	Total Block RAM Bits
XC2S15	4	16K
XC2S30	6	24K
XC2S50	8	32K
XC2S100	10	40K
XC2S150	12	48K
XC2S200	14	56K

Each block RAM cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

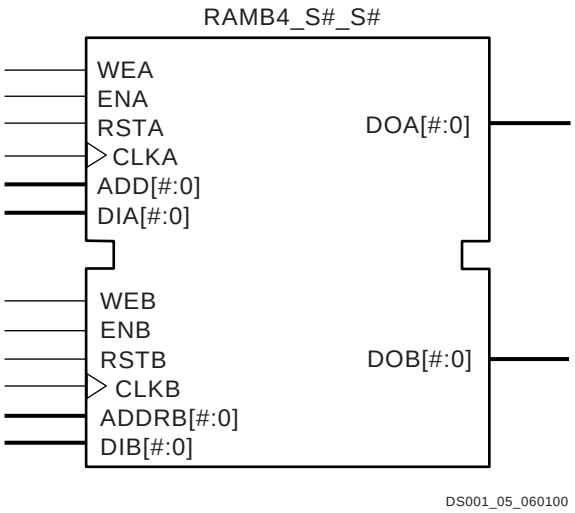


Figure 5: **Dual-Port Block RAM**

Table 6 shows the depth and width aspect ratios for the block RAM.

Table 6: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-II FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

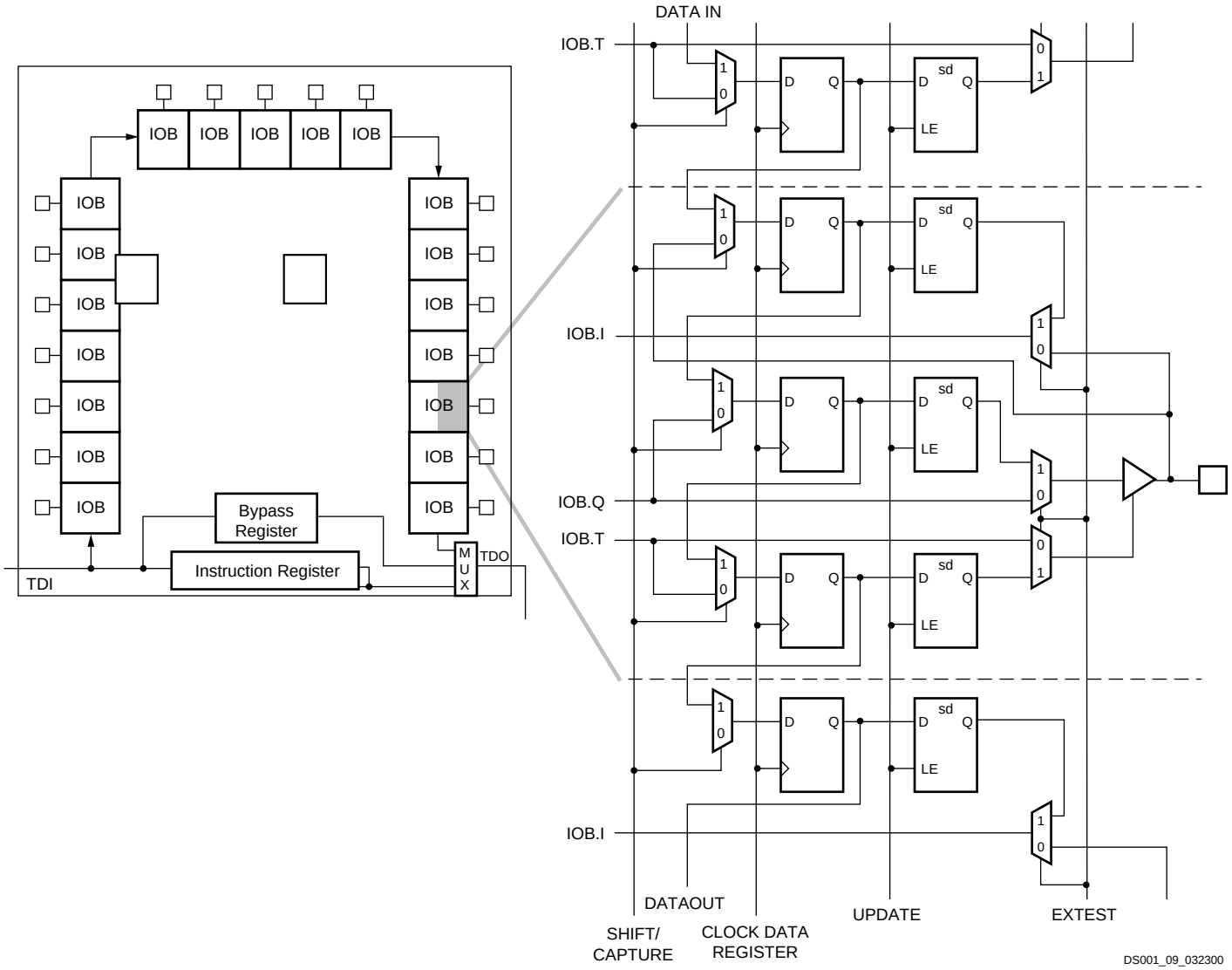


Figure 9: **Spartan-II Family Boundary Scan Logic**

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the Downloads area.

Configuration

Configuration is the process by which the bitstream of a design, as generated by the Xilinx software, is loaded into the internal configuration memory of the FPGA. Spartan-II devices support both serial configuration, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

Configuration File

Spartan-II devices are configured by sequentially loading frames of data that have been concatenated into a configuration file. Table 8 shows how much nonvolatile storage space is needed for Spartan-II devices.

It is important to note that, while a PROM is commonly used to store configuration data before loading them into the FPGA, it is by no means required. Any of a number of different kinds of under populated nonvolatile storage already available either on or off the board (i.e., hard drives, FLASH cards, etc.) can be used. For more information on configuration without a PROM, refer to XAPP098, *The Low-Cost, Efficient Serial Configuration of Spartan FPGAs*.

Table 8: **Spartan-II Configuration File Size**

Device	Configuration File Size (Bits)
XC2S15	197,696
XC2S30	336,768
XC2S50	559,200
XC2S100	781,216
XC2S150	1,040,096
XC2S200	1,335,840

Modes

Spartan-II devices support the following four configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to the end of configuration. The selection codes are listed in Table 9.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

Table 9: **Configuration Modes**

Configuration Mode	Preconfiguration Pull-ups	M0	M1	M2	CCLK Direction	Data Width	Serial D_{OUT}
Master Serial mode	No	0	0	0	Out	1	Yes
	Yes	0	0	1			
Slave Parallel mode	Yes	0	1	0	In	8	No
	No	0	1	1			
Boundary-Scan mode	Yes	1	0	0	N/A	1	No
	No	1	0	1			
Slave Serial mode	Yes	1	1	0	In	1	Yes
	No	1	1	1			

Notes:

1. During power-on and throughout configuration, the I/O drivers will be in a high-impedance state. After configuration, all unused I/Os (those not assigned signals) will remain in a high-impedance state. Pins used as outputs may pulse High at the end of configuration (see Answer 10504).
2. If the Mode pins are set for preconfiguration pull-ups, those resistors go into effect once the rising edge of INIT samples the Mode pins. They will stay in effect until GTS is released during startup, after which the UnusedPin bitstream generator option will determine whether the unused I/Os have a pull-up, pull-down, or no resistor.

Signals

There are two kinds of pins that are used to configure Spartan-II devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{PROGRAM}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see "Pinout Tables" in Module 4 and XAPP176, *Spartan-II FPGA Series Configuration and Readback*.

The Process

The sequence of steps necessary to configure Spartan-II devices are shown in Figure 11. The overall flow can be divided into three different phases.

- Initiating Configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

Initiating Configuration

There are two different ways to initiate the configuration process: applying power to the device or asserting the $\overline{\text{PROGRAM}}$ input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Figure 12, page 19. Before configuration can begin, V_{CCO} Bank 2 must be greater than 1.0V. Furthermore, all V_{CCINT} power pins must be connected to a 2.5V supply. For more information on delaying configuration, see "Clearing Configuration Memory," page 19.

Once in user operation, the device can be re-configured simply by pulling the $\overline{\text{PROGRAM}}$ pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase.

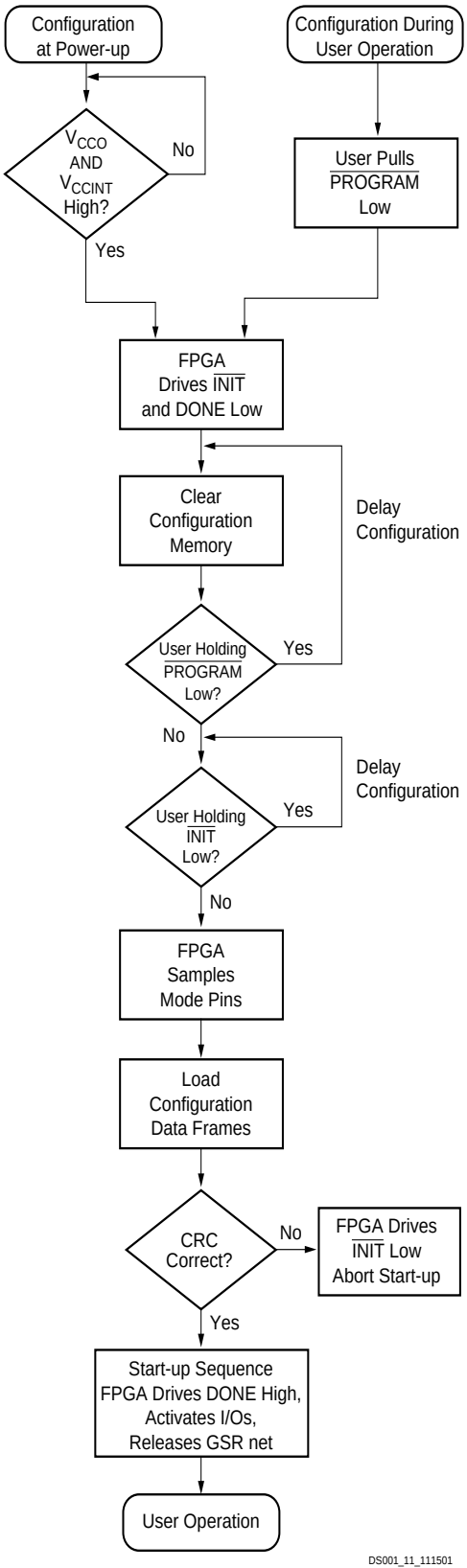


Figure 11: **Configuration Flow Diagram**

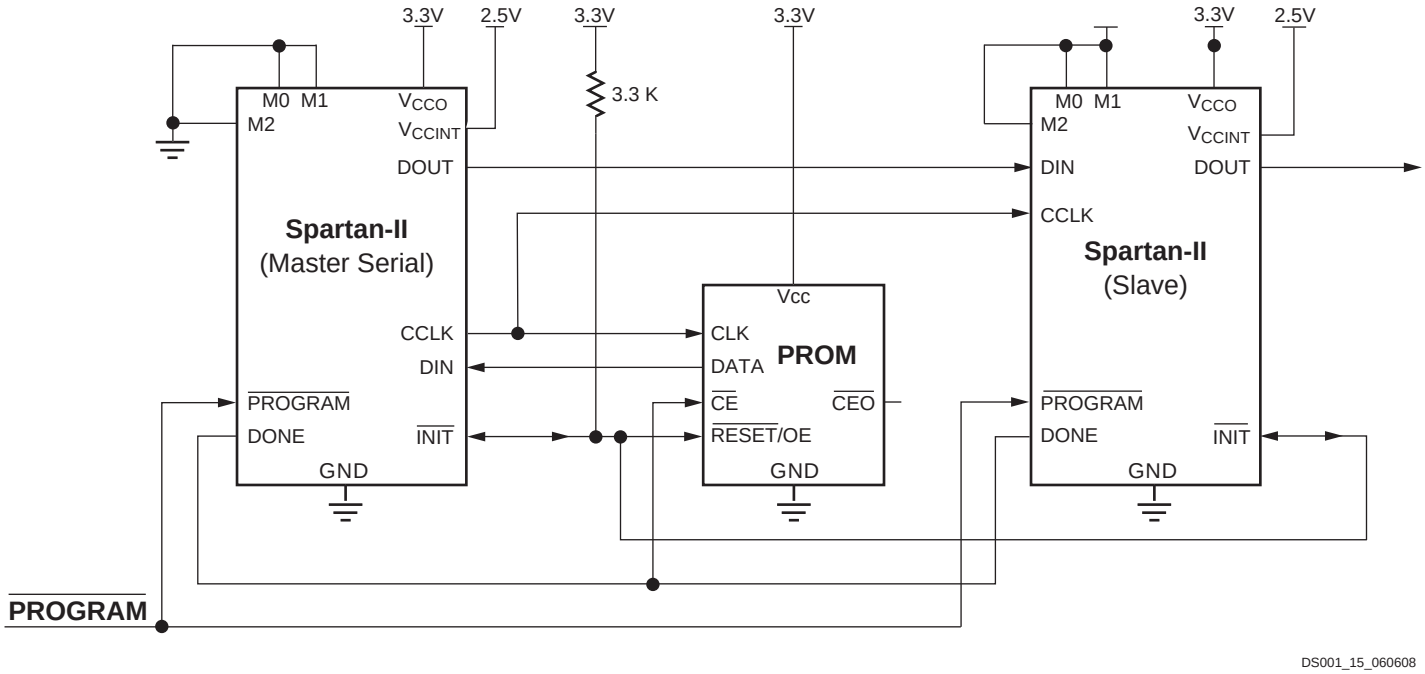
Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

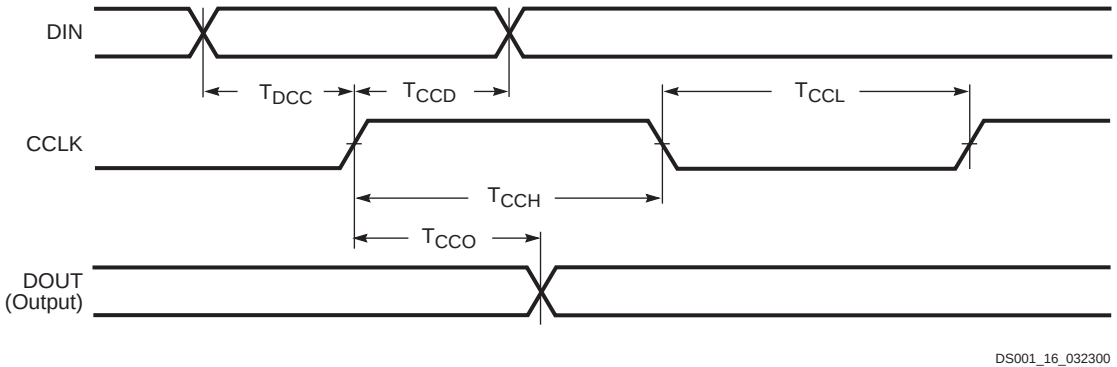
Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.



Notes:
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 15: **Master/Slave Serial Configuration Circuit Diagram**



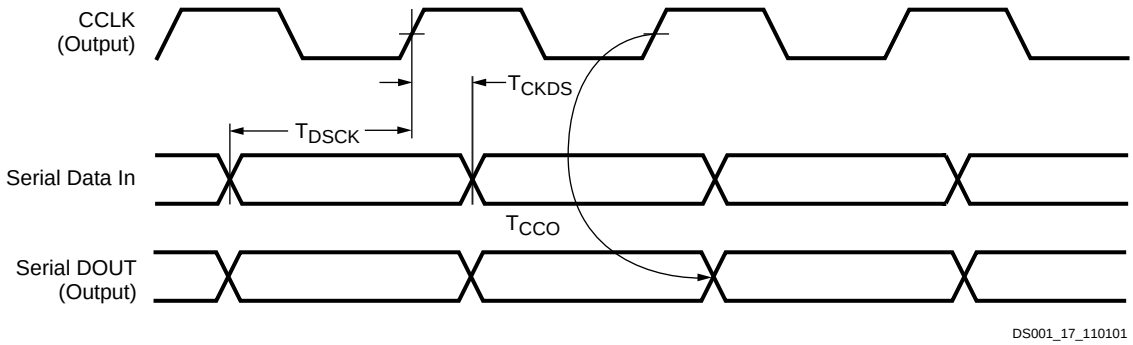
Symbol		Description		Units
T_{DCC}	CCLK	DIN setup	5	ns, min
T_{CCD}		DIN hold	0	ns, min
T_{CCO}		DOUT	12	ns, max
T_{CCH}		High time	5	ns, min
T_{CCL}		Low time	5	ns, min
F_{CC}		Maximum frequency	66	MHz, max

Figure 16: **Slave Serial Mode Timing**

Master Serial Mode

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 15 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by $\overline{\text{INIT}}$, and CE input is driven by DONE. The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx software. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point, the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The frequency of the CCLK signal created by the internal oscillator has a variance of +45%, –30% from the specified value.

Figure 17 shows the timing for Master Serial configuration. The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.



Symbol		Description		Units
T_{DSCK}	CCLK	DIN setup	5.0	ns, min
T_{CKDS}		DIN hold	0.0	ns, min
		Frequency tolerance with respect to nominal	+45%, –30%	-

Figure 17: **Master Serial Mode Timing**

Slave Parallel Mode

The Slave Parallel mode is the fastest configuration option. Byte-wide data is written into the FPGA. A BUSY flag is provided for controlling the flow of data at a clock frequency F_{CCNH} above 50 MHz.

Figure 18, page 24 shows the connections for two Spartan-II devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

If a configuration file of the format .bit, .rbt, or non-swapped HEX is used for parallel programming, then the most significant bit (i.e. the left-most bit of each configuration byte, as displayed in a text editor) must be routed to the D0 input on the FPGA.

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by de-asserting $\overline{\text{WRITE}}$. See "Readback," page 25.

support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features, system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 15, each buffer type can support a variety of voltage requirements.

Table 15: **Versatile I/O Supported Standards (Typical Values)**

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL (2-24 mA)	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	1.5
HSTL Class IV	0.9	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance JEDEC website at http://www.jedec.org. For more details on the I/O standards and termination application examples, see XAPP179, "*Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs.*"

LVTTL — Low-Voltage TTL

The Low-Voltage TTL (LVTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5V

The Low-Voltage CMOS for 2.5V or lower (LVCMOS2) standard is an extension of the LVCMOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

the LOC property is described below. Table 16 summarizes the input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

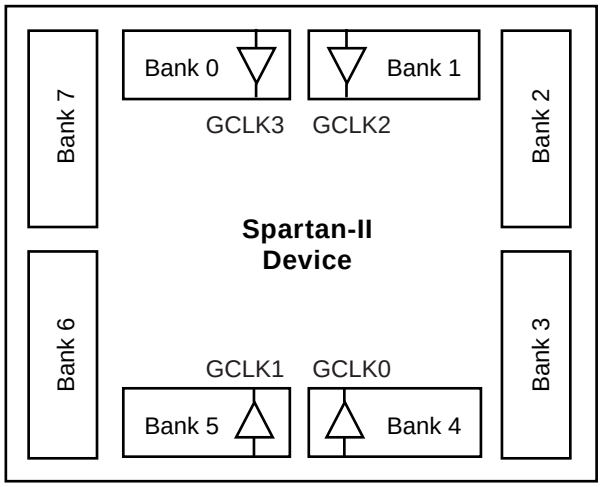


Figure 36: **I/O Banks**

Table 16: **Xilinx Input Standards Compatibility Requirements**

Rule 1	All differential amplifier input signals within a bank are required to be of the same standard.
Rule 2	There are no placement restrictions for inputs with standards that require a single-ended input buffer.

IBUFG

Signals used as high fanout clock inputs to the Spartan-II device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG primitive can only drive a CLKDLL, CLKDLLHF, or a BUFG primitive. The generic IBUFG primitive appears in Figure 37.

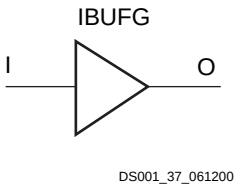


Figure 37: **Global Clock Input Buffer (IBUFG) Primitive**

With no extension or property specified for the generic IBUFG primitive, the assumed standard is LVTTL.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP primitive represents a combination of the LVTTL IBUFG and BUFG primitives, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

The Spartan-II FPGA BUFGP primitive can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) primitive appears in Figure 38.

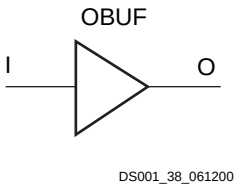


Figure 38: **Output Buffer (OBUF) Primitive**

With no extension or property specified for the generic OBUF primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 32 for the LVTTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 32: **LVTTL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	2.0	-	5.5
V_{IL}	–0.5	-	0.8
V_{OH}	2.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–24	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Notes:
1. V_{OL} and V_{OH} for lower drive currents sample tested.

LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 33 for the LVCMOS2 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 33: **LVCMOS2 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.7	-	5.5
V_{IL}	–0.5	-	0.7
V_{OH}	1.9	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–12	-	-
I_{OL} at V_{OL} (mA)	12	-	-

AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 34 for the AGP-2X standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 34: **AGP-2X Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}$ (1)	1.17	1.32	1.48
V_{TT}	-	-	-
$V_{IH} \geq V_{REF} + 0.2$	1.37	1.52	-
$V_{IL} \leq V_{REF} - 0.2$	-	1.12	1.28
$V_{OH} \geq 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} \leq 0.1 \times V_{CCO}$	-	0.33	0.36
I_{OH} at V_{OH} (mA)	Note 2	-	-
I_{OL} at V_{OL} (mA)	Note 2	-	-

Notes:
1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

For design examples and more information on using the I/O, see XAPP179, *Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs*.

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Delay Adjustments for Different Standards," page 57.

Symbol	Description	Device	Speed Grade				Units
			-6		-5		
			Min	Max	Min	Max	
Propagation Delays							
T_{IOPI}	Pad to I output, no delay	All	-	0.8	-	1.0	ns
T_{IOPID}	Pad to I output, with delay	All	-	1.5	-	1.8	ns
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	-	1.7	-	2.0	ns
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S15	-	3.8	-	4.5	ns
		XC2S30	-	3.8	-	4.5	ns
		XC2S50	-	3.8	-	4.5	ns
		XC2S100	-	3.8	-	4.5	ns
		XC2S150	-	4.0	-	4.7	ns
		XC2S200	-	4.0	-	4.7	ns
Sequential Delays							
T_{IOCKIQ}	Clock CLK to output IQ	All	-	0.7	-	0.8	ns
Setup/Hold Times with Respect to Clock CLK(2)							
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	1.7 / 0	-	1.9 / 0	-	ns
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay(1)	XC2S15	3.8 / 0	-	4.4 / 0	-	ns
		XC2S30	3.8 / 0	-	4.4 / 0	-	ns
		XC2S50	3.8 / 0	-	4.4 / 0	-	ns
		XC2S100	3.8 / 0	-	4.4 / 0	-	ns
		XC2S150	3.9 / 0	-	4.6 / 0	-	ns
		XC2S200	3.9 / 0	-	4.6 / 0	-	ns
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	0.9 / 0.01	-	0.9 / 0.01	-	ns
Set/Reset Delays							
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All	-	1.1	-	1.2	ns
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	-	1.5	-	1.7	ns
T_{GSRQ}	GSR to output IQ	All	-	9.9	-	11.7	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.
2. A zero hold time listing indicates no hold time or a negative hold time.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	60	200	60	180	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	25	100	25	90	MHz
$T_{DLLPWHF}$	Input clock pulse width (CLKDLLHF)	2.0	-	2.4	-	ns
$T_{DLLPWLF}$	Input clock pulse width (CLKDLL)	2.5	-	3.0	-	ns

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Figure 52, page 63, provides definitions for various parameters in the table below.

Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(1)		-	±60	-	±60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(2)		-	±100	-	±100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(3)		-	±140	-	±140	ps
T_{PHIOM}	Maximum phase difference between CLKIN and CLKO(4)		-	±160	-	±160	ps
T_{PHOOM}	Maximum phase difference between clock outputs on the DLL(5)		-	±200	-	±200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

Revision History

Date	Version No.	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Updated timing to reflect the latest speed files. Added current supply numbers and XC2S200 -5 timing numbers. Approved -5 timing numbers as preliminary information with exceptions as noted.
11/02/00	2.1	Removed Power Down feature.
01/19/01	2.2	DC and timing numbers updated to Preliminary for the XC2S50 and XC2S100. Industrial power-on current specifications and -6 DLL timing numbers added. Power-on specification clarified.
03/09/01	2.3	Added note on power sequencing. Clarified power-on current requirement.
08/28/01	2.4	Added -6 preliminary timing. Added typical and industrial standby current numbers. Specified min. power-on current by junction temperature instead of by device type (Commercial vs. Industrial). Eliminated minimum V_{CCINT} ramp time requirement. Removed footnote limiting DLL operation to the Commercial temperature range.
07/26/02	2.5	Clarified that I/O leakage current is specified over the Recommended Operating Conditions for V_{CCINT} and V_{CCO}.
08/26/02	2.6	Added references for XAPP450 to Power-On Current Specification.
09/03/03	2.7	Added relaxed minimum power-on current (I_{CCPO}) requirements to page 53. On page 64, moved T_{RPW} values from maximum to minimum column.
06/13/08	2.8	Updated I/O measurement thresholds. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.

Table 36: **Spartan-II Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass[1] (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	60	0.5	16 x 16	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	92	0.5	22 x 22	1.60	1.4
CS144 / CSG144	144	Chip Scale Ball Grid Array (CSBGA)	92	0.8	12 x 12	1.20	0.3
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	140	0.5	30.6 x 30.6	3.70	5.3
FG256 / FGG256	256	Fine-pitch Ball Grid Array (FBGA)	176	1.0	17 x 17	2.00	0.9
FG456 / FGG456	456	Fine-pitch Ball Grid Array (FBGA)	284	1.0	23 x 23	2.60	2.2

Notes:

1. Package mass is ±10%.

Note: Some early versions of Spartan-II devices, including the XC2S15 and XC2S30 ES devices and the XC2S150 with date code 0045 or earlier, included a power-down pin. For more information, see Answer Record 10500.

VCCO Banks

Some of the I/O standards require specific V_{CCO} voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3 in Module 2). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. In the smaller packages, the V_{CCO} pins are connected between banks, effectively reducing the number of independent banks available (see Table 37). These interconnected banks are shown in the Pinout Tables with V_{CCO} pads for multiple banks connected to the same pin.

Table 37: **Independent VCCO Banks Available**

Package	VQ100 PQ208	CS144 TQ144	FG256 FG456
Independent Banks	1	4	8

Package Overview

Table 36 shows the six low-cost, space-saving production package styles for the Spartan-II family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra ‘G’ in the package style name. For example, the standard “CS144” package becomes “CSG144” when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 38.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 38.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

Table 38: **Xilinx Package Documentation**

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
CS144	Package Drawing	PK149_CS144
CSG144		PK103_CSG144
PQ208	Package Drawing	PK166_PQ208
PQG208		PK123_PQG208
FG256	Package Drawing	PK151_FG256
FGG256		PK105_FGG256
FG456	Package Drawing	PK154_FG456
FGG456		PK109_FGG456

XC2S30 Device Pinouts *(Continued)*

XC2S30 Pad Name						
Function	Bank	VQ100	TQ144	CS144	PQ208	Bndry Scan
I/O	4	-	-	-	P87	295
I/O	4	-	-	-	P88	298
I/O	4	-	P84	K8	P89	301
I/O	4	-	P83	N9	P90	304
V_{CCINT}	-	P42	P82	M9	P91	-
V_{CCO}	4	-	-	-	P92	-
GND	-	-	P81	L9	P93	-
I/O	4	P43	P80	K9	P94	307
I/O	4	P44	P79	N10	P95	310
I/O	4	-	P78	M10	P96	313
I/O, V_{REF}	4	P45	P77	L10	P98	316
I/O	4	-	-	-	P99	319
I/O	4	-	P76	N11	P100	322
I/O	4	P46	P75	M11	P101	325
I/O	4	P47	P74	L11	P102	328
GND	-	P48	P73	N12	P103	-
DONE	3	P49	P72	M12	P104	331
V_{CCO}	4	P50	P71	N13	P105	-
V_{CCO}	3	P50	P70	M13	P105	-
$\overline{PROGRAM}$	-	P51	P69	L12	P106	334
I/O ($\overline{INIT}$)	3	P52	P68	L13	P107	335
I/O (D7)	3	P53	P67	K10	P108	338
I/O	3	-	P66	K11	P109	341
I/O	3	-	-	-	P110	344
I/O, V_{REF}	3	P54	P65	K12	P111	347
I/O	3	-	P64	K13	P113	350
I/O	3	P55	P63	J10	P114	353
I/O (D6)	3	P56	P62	J11	P115	356
GND	-	-	P61	J12	P116	-
V_{CCO}	3	-	-	-	P117	-
I/O (D5)	3	P57	P60	J13	P119	359
I/O	3	P58	P59	H10	P120	362
I/O	3	-	-	-	P121	365
I/O	3	-	-	-	P122	368
I/O	3	-	-	-	P123	371
GND	-	-	-	-	P124	-
I/O, V_{REF}	3	P59	P58	H11	P125	374
I/O (D4)	3	P60	P57	H12	P126	377
I/O	3	-	P56	H13	P127	380
V_{CCINT}	-	P61	P55	G12	P128	-
I/O, TRDY(1)	3	P62	P54	G13	P129	386

XC2S30 Device Pinouts *(Continued)*

XC2S30 Pad Name						
Function	Bank	VQ100	TQ144	CS144	PQ208	Bndry Scan
V_{CCO}	3	P63	P53	G11	P130	-
V_{CCO}	2	P63	P53	G11	P130	-
GND	-	P64	P52	G10	P131	-
I/O, IRDY(1)	2	P65	P51	F13	P132	389
I/O	2	-	-	-	P133	392
I/O	2	-	P50	F12	P134	395
I/O (D3)	2	P66	P49	F11	P135	398
I/O, V_{REF}	2	P67	P48	F10	P136	401
GND	-	-	-	-	P137	-
I/O	2	-	-	-	P138	404
I/O	2	-	-	-	P139	407
I/O	2	-	-	-	P140	410
I/O	2	P68	P47	E13	P141	413
I/O (D2)	2	P69	P46	E12	P142	416
V_{CCO}	2	-	-	-	P144	-
GND	-	-	P45	E11	P145	-
I/O (D1)	2	P70	P44	E10	P146	419
I/O	2	P71	P43	D13	P147	422
I/O	2	-	P42	D12	P148	425
I/O, V_{REF}	2	P72	P41	D11	P150	428
I/O	2	-	-	-	P151	431
I/O	2	-	P40	C13	P152	434
I/O (DIN, D0)	2	P73	P39	C12	P153	437
I/O (DOUT, BUSY)	2	P74	P38	C11	P154	440
CCLK	2	P75	P37	B13	P155	443
V_{CCO}	2	P76	P36	B12	P156	-
V_{CCO}	1	P76	P35	A13	P156	-
TDO	2	P77	P34	A12	P157	-
GND	-	P78	P33	B11	P158	-
TDI	-	P79	P32	A11	P159	-
I/O ($\overline{CS}$)	1	P80	P31	D10	P160	0
I/O ($\overline{WRITE}$)	1	P81	P30	C10	P161	3
I/O	1	-	P29	B10	P162	6
I/O	1	-	-	-	P163	9
I/O, V_{REF}	1	P82	P28	A10	P164	12
I/O	1	-	-	-	P166	15
I/O	1	P83	P27	D9	P167	18
I/O	1	P84	P26	C9	P168	21
GND	-	-	P25	B9	P169	-
V_{CCO}	1	-	-	-	P170	-

XC2S50 Device Pinouts

XC2S50 Pad Name					
Function	Bank	TQ144	PQ208	FG256	Bndry Scan
GND	-	P143	P1	GND*	-
TMS	-	P142	P2	D3	-
I/O	7	P141	P3	C2	149
I/O	7	-	-	A2	152
I/O	7	P140	P4	B1	155
I/O	7	-	-	E3	158
I/O	7	-	P5	D2	161
GND	-	-	-	GND*	-
I/O, V_{REF}	7	P139	P6	C1	164
I/O	7	-	P7	F3	167
I/O	7	-	-	E2	170
I/O	7	P138	P8	E4	173
I/O	7	P137	P9	D1	176
I/O	7	P136	P10	E1	179
GND	-	P135	P11	GND*	-
V_{CCO}	7	-	P12	V_{CCO} Bank 7*	-
V_{CCINT}	-	-	P13	V_{CCINT}*	-
I/O	7	P134	P14	F2	182
I/O	7	P133	P15	G3	185
I/O	7	-	-	F1	188
I/O	7	-	P16	F4	191
I/O	7	-	P17	F5	194
I/O	7	-	P18	G2	197
GND	-	-	P19	GND*	-
I/O, V_{REF}	7	P132	P20	H3	200
I/O	7	P131	P21	G4	203
I/O	7	-	-	H2	206
I/O	7	P130	P22	G5	209
I/O	7	-	P23	H4	212
I/O, IRDY(1)	7	P129	P24	G1	215
GND	-	P128	P25	GND*	-
V_{CCO}	7	P127	P26	V_{CCO} Bank 7*	-
V_{CCO}	6	P127	P26	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P126	P27	J2	218
V_{CCINT}	-	P125	P28	V_{CCINT}*	-
I/O	6	P124	P29	H1	224
I/O	6	-	-	J4	227
I/O	6	P123	P30	J1	230
I/O, V_{REF}	6	P122	P31	J3	233

XC2S50 Device Pinouts *(Continued)*

XC2S50 Pad Name					
Function	Bank	TQ144	PQ208	FG256	Bndry Scan
GND	-	-	P32	GND*	-
I/O	6	-	P33	K5	236
I/O	6	-	P34	K2	239
I/O	6	-	P35	K1	242
I/O	6	-	-	K3	245
I/O	6	P121	P36	L1	248
I/O	6	P120	P37	L2	251
V_{CCINT}	-	-	P38	V_{CCINT}*	-
V_{CCO}	6	-	P39	V_{CCO} Bank 6*	-
GND	-	P119	P40	GND*	-
I/O	6	P118	P41	K4	254
I/O	6	P117	P42	M1	257
I/O	6	P116	P43	L4	260
I/O	6	-	-	M2	263
I/O	6	-	P44	L3	266
I/O, V_{REF}	6	P115	P45	N1	269
GND	-	-	-	GND*	-
I/O	6	-	P46	P1	272
I/O	6	-	-	L5	275
I/O	6	P114	P47	N2	278
I/O	6	-	-	M4	281
I/O	6	P113	P48	R1	284
I/O	6	P112	P49	M3	287
M1	-	P111	P50	P2	290
GND	-	P110	P51	GND*	-
M0	-	P109	P52	N3	291
V_{CCO}	6	P108	P53	V_{CCO} Bank 6*	-
V_{CCO}	5	P107	P53	V_{CCO} Bank 5*	-
M2	-	P106	P54	R3	292
I/O	5	-	-	N5	299
I/O	5	P103	P57	T2	302
I/O	5	-	-	P5	305
I/O	5	-	P58	T3	308
GND	-	-	-	GND*	-
I/O, V_{REF}	5	P102	P59	T4	311
I/O	5	-	P60	M6	314
I/O	5	-	-	T5	317
I/O	5	P101	P61	N6	320
I/O	5	P100	P62	R5	323

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	6	-	-	T2	449
I/O	6	P43	L4	U1	452
GND	-	-	GND*	GND*	-
I/O	6	-	M2	R5	455
I/O	6	-	-	V1	458
I/O	6	-	-	T5	461
I/O	6	P44	L3	U2	464
I/O, V_{REF}	6	P45	N1	T3	467
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-
I/O	6	P46	P1	T4	470
I/O	6	-	L5	W1	473
GND	-	-	GND*	GND*	-
I/O	6	-	-	V2	476
I/O	6	-	-	U4	482
I/O, V_{REF}	6	P47	N2	Y1	485
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	488
I/O	6	-	-	V3	491
I/O	6	-	-	V4	494
I/O	6	P48	R1	Y2	500
I/O	6	P49	M3	W3	503
M1	-	P50	P2	U5	506
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	507
V_{CCO}	6	P53	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
V_{CCO}	5	P53	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
M2	-	P54	R3	Y4	508
I/O	5	-	-	W5	518
I/O	5	-	-	AB3	521
I/O	5	-	N5	V7	524
GND	-	-	GND*	GND*	-
I/O, V_{REF}	5	P57	T2	Y6	527
I/O	5	-	-	AA4	530
I/O	5	-	-	AB4	536
I/O	5	-	P5	W6	539
I/O	5	P58	T3	Y7	542
GND	-	-	GND*	GND*	-

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P59	T4	AA5	545
I/O	5	P60	M6	AB5	548
I/O	5	-	-	V8	551
I/O	5	-	-	AA6	554
I/O	5	-	T5	AB6	557
GND	-	-	GND*	GND*	-
I/O	5	P61	N6	AA7	560
I/O	5	-	-	W7	563
I/O, V_{REF}	5	P62	R5	W8	569
I/O	5	P63	P6	Y8	572
GND	-	P64	GND*	GND*	-
V_{CCO}	5	P65	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCINT}	-	P66	V_{CCINT}*	V_{CCINT}*	-
I/O	5	P67	R6	AA8	575
I/O	5	P68	M7	V9	578
I/O	5	-	-	AB8	581
I/O	5	-	-	W9	584
I/O	5	-	-	AB9	587
GND	-	-	GND*	GND*	-
I/O	5	P69	N7	Y9	590
I/O	5	-	-	V10	593
I/O	5	-	-	AA9	596
I/O	5	P70	T6	W10	599
I/O	5	P71	P7	AB10	602
GND	-	P72	GND*	GND*	-
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P73	P8	Y10	605
I/O	5	P74	R7	V11	608
I/O	5	-	-	AA10	614
I/O	5	-	T7	W11	617
I/O	5	P75	T8	AB11	620
I/O	5	-	-	U11	623
V_{CCINT}	-	P76	V_{CCINT}*	V_{CCINT}*	-
I, GCK1	5	P77	R8	Y11	635
V_{CCO}	5	P78	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCO}	4	P78	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-