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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	260
Number of Gates	150000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	456-BBGA
Supplier Device Package	456-FBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/xilinx/xc2s150-6fg456c">https://www.e-xfl.com/product-detail/xilinx/xc2s150-6fg456c</a>

## Introduction

The Spartan®-II Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The six-member family offers densities ranging from 15,000 to 200,000 system gates, as shown in [Table 1](#). System performance is supported up to 200 MHz. Features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards, and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-II family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

## Features

- Second generation ASIC replacement technology
  - Densities as high as 5,292 logic cells with up to 200,000 system gates
  - Streamlined features based on Virtex® FPGA architecture
  - Unlimited reprogrammability
  - Very low cost
  - Cost-effective 0.18 micron process
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K bit block RAM
    - Fast interfaces to external RAM
  - Fully PCI compliant
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 16 high-performance interface standards
  - Hot swap Compact PCI friendly
  - Zero hold time simplifies system timing
- Core logic powered at 2.5V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing

**Table 1: Spartan-II FPGA Family Members**

Device	Logic Cells	System Gates (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O <sup>(1)</sup>	Total Distributed RAM Bits	Total Block RAM Bits
XC2S15	432	15,000	8 x 12	96	86	6,144	16K
XC2S30	972	30,000	12 x 18	216	92	13,824	24K
XC2S50	1,728	50,000	16 x 24	384	176	24,576	32K
XC2S100	2,700	100,000	20 x 30	600	176	38,400	40K
XC2S150	3,888	150,000	24 x 36	864	260	55,296	48K
XC2S200	5,292	200,000	28 x 42	1,176	284	75,264	56K

### Notes:

1. All user I/O counts do not include the four global clock/user input pins. See details in [Table 2, page 4](#).

## Architectural Description

### Spartan-II FPGA Array

The Spartan®-II field-programmable gate array, shown in [Figure 2](#), is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in [Figure 2](#), the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and

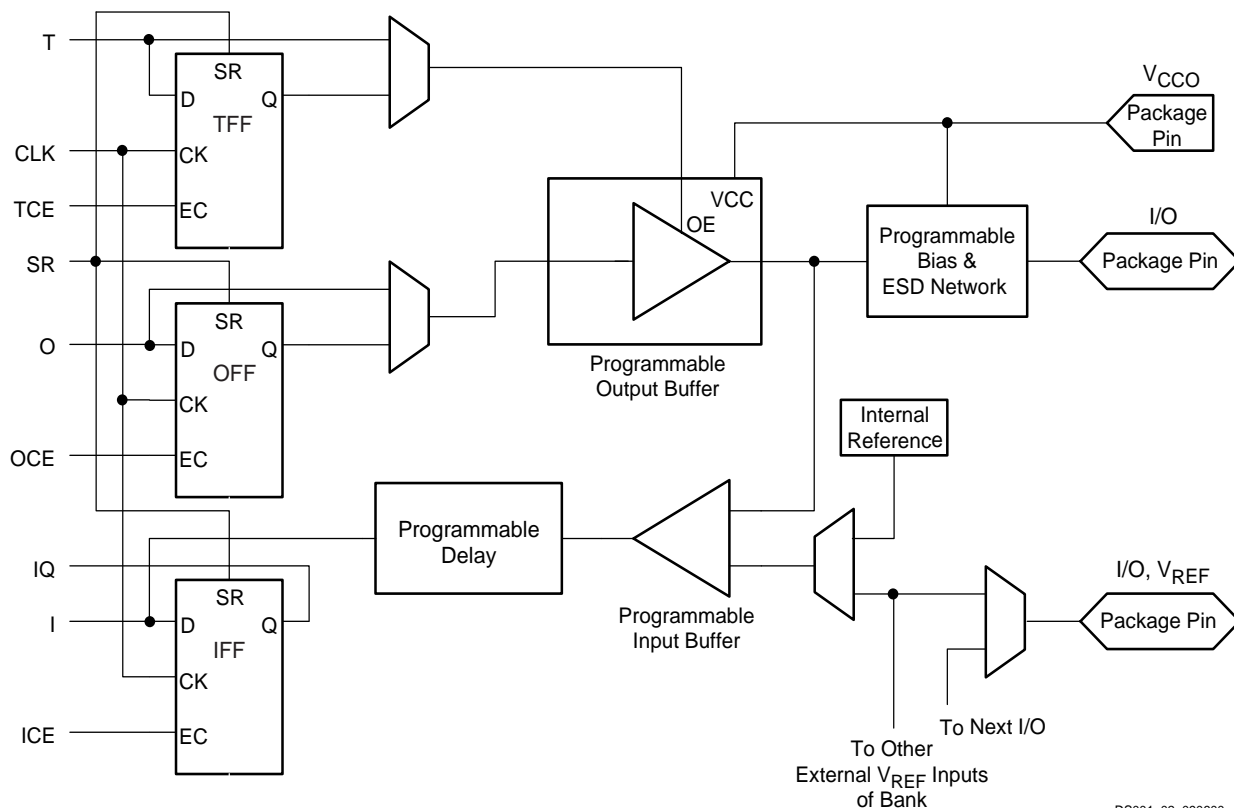
memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

### Input/Output Block

The Spartan-II FPGA IOB, as seen in [Figure 2](#), features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. [Table 3](#) lists several of the standards which are supported along with the required reference, output and termination voltages needed to meet the standard.



**Figure 2: Spartan-II FPGA Input/Output Block (IOB)**

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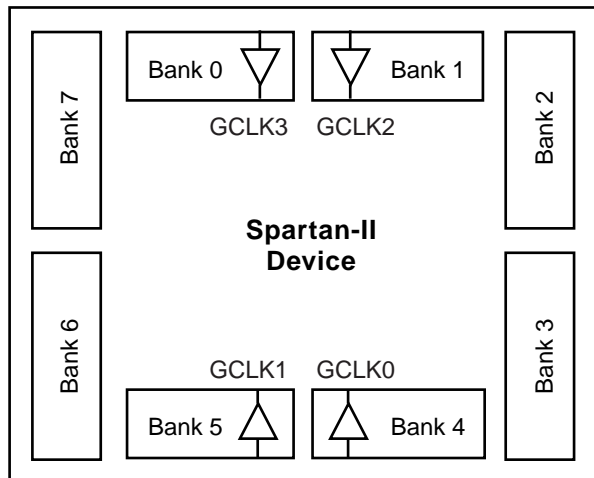
drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate  $V_{REF}$  voltage must be provided if the signaling standard requires one. The provision of this voltage must comply with the I/O banking rules.

### I/O Banking

Some of the I/O standards described above require  $V_{CCO}$  and/or  $V_{REF}$  voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3). Each bank has multiple  $V_{CCO}$  pins which must be connected to the same voltage. Voltage is determined by the output standards in use.



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Figure 3: Spartan-II I/O Banks

Within a bank, output standards may be mixed only if they use the same  $V_{CCO}$ . Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on  $V_{CCO}$ .

Table 4: Compatible Output Standards

$V_{CCO}$	Compatible Standards
3.3V	PCI, LVTTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage,  $V_{REF}$ . In this case, certain user-I/O pins are

automatically configured as inputs for the  $V_{REF}$  voltage. About one in six of the I/O pins in the bank assume this role.

$V_{REF}$  pins within a bank are interconnected internally and consequently only one  $V_{REF}$  voltage can be used within each bank. All  $V_{REF}$  pins in the bank, however, must be connected to the external voltage source for correct operation.

In a bank, inputs requiring  $V_{REF}$  can be mixed with those that do not but only one  $V_{REF}$  voltage may be used within a bank. Input buffers that use  $V_{REF}$  are not 5V tolerant. LVTTTL, LVCMOS2, and PCI are 5V tolerant. The  $V_{CCO}$  and  $V_{REF}$  pins for each bank appear in the device pinout tables.

Within a given package, the number of  $V_{REF}$  and  $V_{CCO}$  pins can vary depending on the size of device. In larger devices, more I/O pins convert to  $V_{REF}$  pins. Since these are always a superset of the  $V_{REF}$  pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device. All  $V_{REF}$  pins for the largest device anticipated must be connected to the  $V_{REF}$  voltage, and not used for I/O.

### Independent Banks Available

Package	VQ100 PQ208	CS144 TQ144	FG256 FG456
Independent Banks	1	4	8

### Configurable Logic Block

The basic building block of the Spartan-II FPGA CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and storage element. Output from the function generator in each LC drives the CLB output and the D input of the flip-flop. Each Spartan-II FPGA CLB contains four LCs, organized in two similar slices; a single slice is shown in Figure 4.

In addition to the four basic LCs, the Spartan-II FPGA CLB contains logic that combines function generators to provide functions of five or six inputs.

### Look-Up Tables

Spartan-II FPGA function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-II FPGA LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

## Signals

There are two kinds of pins that are used to configure Spartan-II devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the **PROGRAM** pin, the **DONE** pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a  $V_{CCO}$  of 3.3V to drive an LVTTTL signal or 2.5V to drive an LVC MOS signal. All the relevant pins fall in banks 2 or 3. The **CS** and **WRITE** pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see "Pinout Tables" in Module 4 and [XAPP176](#), *Spartan-II FPGA Series Configuration and Readback*.

## The Process

The sequence of steps necessary to configure Spartan-II devices are shown in [Figure 11](#). The overall flow can be divided into three different phases.

- Initiating Configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

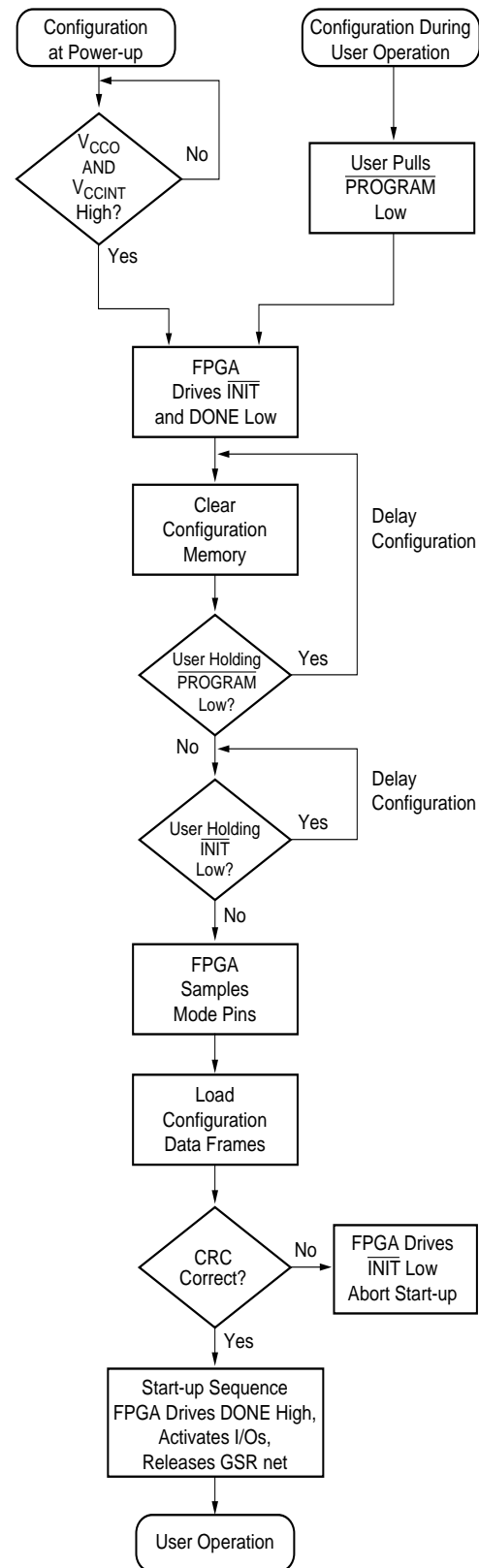
### Initiating Configuration

There are two different ways to initiate the configuration process: applying power to the device or asserting the **PROGRAM** input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in [Figure 12](#), page 19. Before configuration can begin,  $V_{CCO}$  Bank 2 must be greater than 1.0V. Furthermore, all  $V_{CCINT}$  power pins must be connected to a 2.5V supply. For more information on delaying configuration, see "Clearing Configuration Memory," page 19.

Once in user operation, the device can be re-configured simply by pulling the **PROGRAM** pin Low. The device acknowledges the beginning of the configuration process

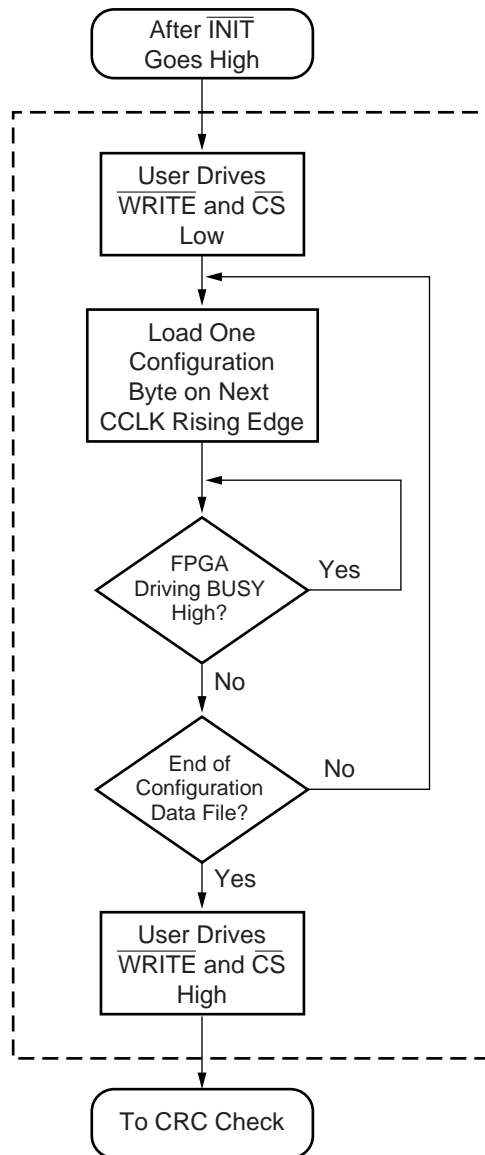
by driving **DONE** Low, then enters the memory-clearing phase.



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Figure 11: Configuration Flow Diagram

If CCLK is slower than  $F_{CCNH}$ , the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.



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Figure 19: Loading Configuration Data for the Slave Parallel Mode

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of  $\overline{CS}$ .

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the  $\overline{CS}$  signal may be de-asserted until the next byte is valid on D0-D7. While  $\overline{CS}$  is High, the Slave Parallel

interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration,  $\overline{WRITE}$  must continue to be asserted while  $\overline{CS}$  is asserted.

### Abort

To abort configuration during a write sequence, de-assert  $\overline{WRITE}$  while holding  $\overline{CS}$  Low. The abort operation is initiated at the rising edge of CCLK, as shown in Figure 21, page 26. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

### Boundary-Scan Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG\_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG\_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2).

### Readback

The configuration data stored in the Spartan-II FPGA configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see [XAPP176](#), *Spartan-II FPGA Family Configuration and Readback*.



## Startup Delay Property

This property, `STARTUP_WAIT`, takes on a value of `TRUE` or `FALSE` (the default value). When `TRUE` the Startup Sequence following device configuration is paused at a user-specified point until the DLL locks. [XAPP176: Configuration and Readback of the Spartan-II and Spartan-IIe Families](#) explains how this can result in delaying the assertion of the `DONE` pin until the DLL locks.

## DLL Location Constraints

The DLLs are distributed such that there is one DLL in each corner of the device. The location constraint `LOC`, attached to the DLL primitive with the numeric identifier 0, 1, 2, or 3, controls DLL location. The orientation of the four DLLs and their corresponding clock resources appears in [Figure 27](#).

The `LOC` property uses the following form.

`LOC = DLL2`

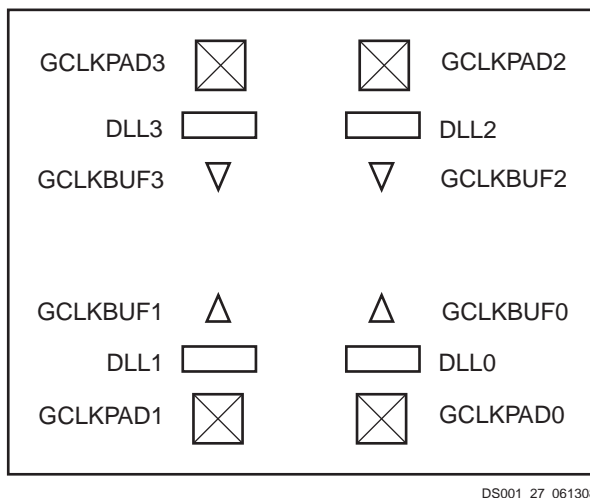


Figure 27: Orientation of DLLs

## Design Considerations

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

### Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the ["DLL Timing Parameters"](#) section of the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the

clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

### Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the `CLKDLL`. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock in a way that has little impact to the DLL. Stopping the clock should be limited to less than approximately 100  $\mu$ s to keep device cooling to a minimum and maintain the validity of the current tap setting. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time `LOCKED` will stay High and remain High when the clock is restored. If these conditions may not be met in the design, apply a manual reset to the DLL after re-starting the input clock, even if the `LOCKED` signal has not changed.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the `CLKDLL` control.

### Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an `OBUF`, a global clock buffer `BUFG`, or route directly to destination clock pins. The only `BUFGs` that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). One DLL output can drive more than one `OBUF`; however, this adds skew.

Do not use the DLL output clock signals until after activation of the `LOCKED` signal. Prior to the activation of the `LOCKED` signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 18 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 19 for the number of effective output power/ground pairs for each Spartan-II device and package combination.

**Table 18: Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package	
	CS, FG	PQ, TQ, VQ
LVTTL Slow Slew Rate, 2 mA drive	68	36
LVTTL Slow Slew Rate, 4 mA drive	41	20
LVTTL Slow Slew Rate, 6 mA drive	29	15
LVTTL Slow Slew Rate, 8 mA drive	22	12
LVTTL Slow Slew Rate, 12 mA drive	17	9
LVTTL Slow Slew Rate, 16 mA drive	14	7
LVTTL Slow Slew Rate, 24 mA drive	9	5
LVTTL Fast Slew Rate, 2 mA drive	40	21
LVTTL Fast Slew Rate, 4 mA drive	24	12
LVTTL Fast Slew Rate, 6 mA drive	17	9
LVTTL Fast Slew Rate, 8 mA drive	13	7
LVTTL Fast Slew Rate, 12 mA drive	10	5
LVTTL Fast Slew Rate, 16 mA drive	8	4
LVTTL Fast Slew Rate, 24 mA drive	5	3
LVC MOS2	10	5
PCI	8	4
GTL	4	4
GTL+	4	4
HSTL Class I	18	9
HSTL Class III	9	5
HSTL Class IV	5	3
SSTL2 Class I	15	8

**Table 18: Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package	
	CS, FG	PQ, TQ, VQ
SSTL2 Class II	10	5
SSTL3 Class I	11	6
SSTL3 Class II	7	4
CTT	14	7
AGP	9	5

**Notes:**

1. This analysis assumes a 35 pF load for each output.

**Table 19: Effective Output Power/Ground Pairs for Spartan-II Devices**

Pkg.	Spartan-II Devices					
	XC2S 15	XC2S 30	XC2S 50	XC2S 100	XC2S 150	XC2S 200
VQ100	8	8	-	-	-	-
CS144	12	12	-	-	-	-
TQ144	12	12	12	12	-	-
PQ208	-	16	16	16	16	16
FG256	-	-	16	16	16	16
FG456	-	-	-	48	48	48

## Termination Examples

Creating a design with the Versatile I/O features requires the instantiation of the desired library primitive within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the Versatile I/O features. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.



## Revision History

Date	Version	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Corrected banking description.
03/05/01	2.1	Clarified guidelines for applying power to $V_{CCINT}$ and $V_{CCO}$
09/03/03	2.2	<p>The following changes were made:</p> <ul style="list-style-type: none"> <li>"Serial Modes," page 20 cautions about toggling <math>\overline{WRITE}</math> during serial configuration.</li> <li>Maximum <math>V_{IH}</math> values in Table 32 and Table 33 changed to 5.5V.</li> <li>In "Boundary Scan," page 13, removed sentence about lack of INTEST support.</li> <li>In Table 9, page 17, added note about the state of I/Os after power-on.</li> <li>In "Slave Parallel Mode," page 23, explained configuration bit alignment to SelectMap port.</li> </ul>
06/13/08	2.8	Added note that TDI, TMS, and TCK have a default pull-up resistor. Added note on maximum daisy chain limit. Updated Figure 15 and Figure 18 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated DLL section. Recommended using property or attribute instead of primitive to define I/O properties. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.

## Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All limits are representative of worst-case supply voltage and junction temperature conditions. Typical numbers are based on measurements taken at a nominal  $V_{CCINT}$  level of 2.5V and a junction temperature of 25°C. The parameters included are common to popular designs and typical applications. **All specifications are subject to change without notice.**

## DC Specifications

### Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Description	Min	Max	Units
$V_{CCINT}$	Supply voltage relative to GND <sup>(2)</sup>	-0.5	3.0	V
$V_{CCO}$	Supply voltage relative to GND <sup>(2)</sup>	-0.5	4.0	V
$V_{REF}$	Input reference voltage	-0.5	3.6	V
$V_{IN}$	Input voltage relative to GND <sup>(3)</sup>			
	5V tolerant I/O <sup>(4)</sup>	-0.5	5.5	V
$V_{TS}$	Input voltage relative to GND <sup>(3)</sup>			
	No 5V tolerance <sup>(5)</sup>	-0.5	$V_{CCO} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output			
	5V tolerant I/O <sup>(4)</sup>	-0.5	5.5	V
$V_{TS}$	Voltage applied to 3-state output			
	No 5V tolerance <sup>(5)</sup>	-0.5	$V_{CCO} + 0.5$	V
$T_{STG}$	Storage temperature (ambient)	-65	+150	°C
$T_J$	Junction temperature	-	+125	°C

#### Notes:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
- Power supplies may turn on in any order.
- $V_{IN}$  should not exceed  $V_{CCO}$  by more than 3.6V over extended periods of time (e.g., longer than a day).
- Spartan®-II device I/Os are 5V Tolerant whenever the LVTTTL, LVCMOS2, or PCI33\_5 signal standard has been selected. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA, and undershoot must be limited to either -0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to -2.0V or overshoot to +7.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- Without 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either  $V_{CCO} + 0.5V$  or 10 mA, and undershoot must be limited to -0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to -2.0V or overshoot to  $V_{CCO} + 2.0V$ , provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
- For soldering guidelines, see the [Packaging Information](#) on the Xilinx® web site.

## IOB Input Switching Characteristics<sup>(1)</sup>

Input delays associated with the pad are specified for LVTTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Delay Adjustments for Different Standards," page 57.

Symbol	Description	Device	Speed Grade				Units
			-6		-5		
			Min	Max	Min	Max	
Propagation Delays							
T <sub>IOPI</sub>	Pad to I output, no delay	All	-	0.8	-	1.0	ns
T <sub>IOPID</sub>	Pad to I output, with delay	All	-	1.5	-	1.8	ns
T <sub>IOPLI</sub>	Pad to output IQ via transparent latch, no delay	All	-	1.7	-	2.0	ns
T <sub>IOPLID</sub>	Pad to output IQ via transparent latch, with delay	XC2S15	-	3.8	-	4.5	ns
		XC2S30	-	3.8	-	4.5	ns
		XC2S50	-	3.8	-	4.5	ns
		XC2S100	-	3.8	-	4.5	ns
		XC2S150	-	4.0	-	4.7	ns
		XC2S200	-	4.0	-	4.7	ns
Sequential Delays							
T <sub>IOCKIQ</sub>	Clock CLK to output IQ	All	-	0.7	-	0.8	ns
Setup/Hold Times with Respect to Clock CLK <sup>(2)</sup>							
T <sub>IOPICK</sub> / T <sub>IOICKP</sub>	Pad, no delay	All	1.7 / 0	-	1.9 / 0	-	ns
T <sub>IOPICKD</sub> / T <sub>IOICKPD</sub>	Pad, with delay <sup>(1)</sup>	XC2S15	3.8 / 0	-	4.4 / 0	-	ns
		XC2S30	3.8 / 0	-	4.4 / 0	-	ns
		XC2S50	3.8 / 0	-	4.4 / 0	-	ns
		XC2S100	3.8 / 0	-	4.4 / 0	-	ns
		XC2S150	3.9 / 0	-	4.6 / 0	-	ns
		XC2S200	3.9 / 0	-	4.6 / 0	-	ns
T <sub>IOICECK</sub> / T <sub>IOICKICE</sub>	ICE input	All	0.9 / 0.01	-	0.9 / 0.01	-	ns
Set/Reset Delays							
T <sub>IOSRCKI</sub>	SR input (IFF, synchronous)	All	-	1.1	-	1.2	ns
T <sub>IOSRIQ</sub>	SR input to IQ (asynchronous)	All	-	1.5	-	1.7	ns
T <sub>GSRQ</sub>	GSR to output IQ	All	-	9.9	-	11.7	ns

### Notes:

- Input timing for LVTTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.
- A zero hold time listing indicates no hold time or a negative hold time.

## Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Sequential Delays						
T <sub>BCKO</sub>	Clock CLK to DOUT output	-	3.4	-	4.0	ns
Setup/Hold Times with Respect to Clock CLK <sup>(1)</sup>						
T <sub>BACK</sub> / T <sub>BCKA</sub>	ADDR inputs	1.4 / 0	-	1.4 / 0	-	ns
T <sub>BDCK</sub> / T <sub>BCKD</sub>	DIN inputs	1.4 / 0	-	1.4 / 0	-	ns
T <sub>BECK</sub> / T <sub>BCKE</sub>	EN inputs	2.9 / 0	-	3.2 / 0	-	ns
T <sub>BRCK</sub> / T <sub>BCKR</sub>	RST input	2.7 / 0	-	2.9 / 0	-	ns
T <sub>BWCK</sub> / T <sub>BCKW</sub>	WEN input	2.6 / 0	-	2.8 / 0	-	ns
Clock CLK						
T <sub>BPWH</sub>	Minimum pulse width, High	-	1.9	-	1.9	ns
T <sub>BPWL</sub>	Minimum pulse width, Low	-	1.9	-	1.9	ns
T <sub>BCCS</sub>	CLKA -> CLKB setup time for different ports	-	3.0	-	4.0	ns

**Notes:**

1. A zero hold time listing indicates no hold time or a negative hold time.

## TBUF Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
Combinatorial Delays				
T <sub>IO</sub>	IN input to OUT output	0	0	ns
T <sub>OFF</sub>	TRI input to OUT output high impedance	0.1	0.2	ns
T <sub>ON</sub>	TRI input to valid data on OUT output	0.1	0.2	ns

## JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Setup and Hold Times with Respect to TCK						
T <sub>TAPTCK</sub> / T <sub>TCKTAP</sub>	TMS and TDI setup and hold times	4.0 / 2.0	-	4.0 / 2.0	-	ns
Sequential Delays						
T <sub>TCKTDO</sub>	Output delay from clock TCK to output TDO	-	11.0	-	11.0	ns
f <sub>TCK</sub>	Maximum TCK clock frequency	-	33	-	33	MHz

## Package Thermal Characteristics

Table 39 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on [www.xilinx.com](http://www.xilinx.com/cgi-bin/thermal/thermal.pl) ([www.xilinx.com/cgi-bin/thermal/thermal.pl](http://www.xilinx.com/cgi-bin/thermal/thermal.pl)).

The junction-to-case thermal resistance ( $\theta_{JC}$ ) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board ( $\theta_{JB}$ )

value similarly reports the difference between the board and junction temperature. The junction-to-ambient ( $\theta_{JA}$ ) value reports the temperature difference between the ambient environment and the junction temperature. The  $\theta_{JA}$  value is reported at different air velocities, measured in linear feet per minute (LFM). The “Still Air (0 LFM)” column shows the  $\theta_{JA}$  value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 39: Spartan-II Package Thermal Characteristics

Package	Device	Junction-to-Case ( $\theta_{JC}$ )	Junction-to-Board ( $\theta_{JB}$ )	Junction-to-Ambient ( $\theta_{JA}$ ) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
VQ100 VQG100	XC2S15	11.3	N/A	44.1	36.7	34.2	33.3	°C/Watt
	XC2S30	10.1	N/A	40.7	33.9	31.5	30.8	°C/Watt
TQ144 TQG144	XC2S15	7.3	N/A	38.6	30.0	25.7	24.1	°C/Watt
	XC2S30	6.7	N/A	34.7	27.0	23.1	21.7	°C/Watt
	XC2S50	5.8	N/A	32.2	25.1	21.4	20.1	°C/Watt
	XC2S100	5.3	N/A	31.4	24.4	20.9	19.6	°C/Watt
CS144 CSG144	XC2S30	2.8	N/A	34.0	26.0	23.9	23.2	°C/Watt
PQ208 PQG208	XC2S50	6.7	N/A	25.2	18.6	16.4	15.2	°C/Watt
	XC2S100	5.9	N/A	24.6	18.1	16.0	14.9	°C/Watt
	XC2S150	5.0	N/A	23.8	17.6	15.6	14.4	°C/Watt
	XC2S200	4.1	N/A	23.0	17.0	15.0	13.9	°C/Watt
FG256 FGG256	XC2S50	7.1	17.6	27.2	21.4	20.3	19.8	°C/Watt
	XC2S100	5.8	15.1	25.1	19.5	18.3	17.8	°C/Watt
	XC2S150	4.6	12.7	23.0	17.6	16.3	15.8	°C/Watt
	XC2S200	3.5	10.7	21.4	16.1	14.7	14.2	°C/Watt
FG456 FGG456	XC2S150	2.0	N/A	21.9	17.3	15.8	15.2	°C/Watt
	XC2S200	2.0	N/A	21.0	16.6	15.1	14.5	°C/Watt

## XC2S15 Device Pinouts (Continued)

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
GND	-	-	P61	J12	-
I/O (D5)	3	P57	P60	J13	245
I/O	3	P58	P59	H10	248
I/O, V <sub>REF</sub>	3	P59	P58	H11	251
I/O (D4)	3	P60	P57	H12	254
I/O	3	-	P56	H13	257
V <sub>CCINT</sub>	-	P61	P55	G12	-
I/O, TRDY <sup>(1)</sup>	3	P62	P54	G13	260
V <sub>CCO</sub>	3	P63	P53	G11	-
V <sub>CCO</sub>	2	P63	P53	G11	-
GND	-	P64	P52	G10	-
I/O, IRDY <sup>(1)</sup>	2	P65	P51	F13	263
I/O	2	-	P50	F12	266
I/O (D3)	2	P66	P49	F11	269
I/O, V <sub>REF</sub>	2	P67	P48	F10	272
I/O	2	P68	P47	E13	275
I/O (D2)	2	P69	P46	E12	278
GND	-	-	P45	E11	-
I/O (D1)	2	P70	P44	E10	281
I/O	2	P71	P43	D13	284
I/O, V <sub>REF</sub>	2	P72	P41	D11	287
I/O	2	-	P40	C13	290
I/O (DIN, D0)	2	P73	P39	C12	293
I/O (DOUT, BUSY)	2	P74	P38	C11	296
CCLK	2	P75	P37	B13	299
V <sub>CCO</sub>	2	P76	P36	B12	-
V <sub>CCO</sub>	1	P76	P35	A13	-
TDO	2	P77	P34	A12	-
GND	-	P78	P33	B11	-
TDI	-	P79	P32	A11	-
I/O ( $\overline{\text{CS}}$ )	1	P80	P31	D10	0
I/O ( $\overline{\text{WRITE}}$ )	1	P81	P30	C10	3
I/O	1	-	P29	B10	6
I/O, V <sub>REF</sub>	1	P82	P28	A10	9
I/O	1	P83	P27	D9	12
I/O	1	P84	P26	C9	15
GND	-	-	P25	B9	-
V <sub>CCINT</sub>	-	P85	P24	A9	-
I/O	1	-	P23	D8	18
I/O	1	-	P22	C8	21

## XC2S15 Device Pinouts (Continued)

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
I/O, V <sub>REF</sub>	1	P86	P21	B8	24
I/O	1	-	P20	A8	27
I/O	1	P87	P19	B7	30
I, GCK2	1	P88	P18	A7	36
GND	-	P89	P17	C7	-
V <sub>CCO</sub>	1	P90	P16	D7	-
V <sub>CCO</sub>	0	P90	P16	D7	-
I, GCK3	0	P91	P15	A6	37
V <sub>CCINT</sub>	-	P92	P14	B6	-
I/O	0	-	P13	C6	44
I/O, V <sub>REF</sub>	0	P93	P12	D6	47
I/O	0	-	P11	A5	50
I/O	0	-	P10	B5	53
V <sub>CCINT</sub>	-	P94	P9	C5	-
GND	-	-	P8	D5	-
I/O	0	P95	P7	A4	56
I/O	0	P96	P6	B4	59
I/O, V <sub>REF</sub>	0	P97	P5	C4	62
I/O	0	-	P4	A3	65
I/O	0	P98	P3	B3	68
TCK	-	P99	P2	C3	-
V <sub>CCO</sub>	0	P100	P1	A2	-
V <sub>CCO</sub>	7	P100	P144	B2	-

04/18/01

### Notes:

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on V<sub>CCO</sub> banking.

## Additional XC2S15 Package Pins

### VQ100

Not Connected Pins					
P28	P29	-	-	-	-

11/02/00

### TQ144

Not Connected Pins					
P42	P64	P78	P101	P104	P105
P116	P138	-	-	-	-

11/02/00

### CS144

Not Connected Pins					
D3	D12	J4	K13	M3	M4
M10	N3	-	-	-	-

11/02/00



## XC2S30 Device Pinouts

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
GND	-	P1	P143	A1	P1	-
TMS	-	P2	P142	B1	P2	-
I/O	7	P3	P141	C2	P3	113
I/O	7	-	P140	C1	P4	116
I/O	7	-	-	-	P5	119
I/O, V <sub>REF</sub>	7	P4	P139	D4	P6	122
I/O	7	-	P138	D3	P8	125
I/O	7	P5	P137	D2	P9	128
I/O	7	P6	P136	D1	P10	131
GND	-	-	P135	E4	P11	-
V <sub>CCO</sub>	7	-	-	-	P12	-
I/O	7	P7	P134	E3	P14	134
I/O	7	-	P133	E2	P15	137
I/O	7	-	-	-	P16	140
I/O	7	-	-	-	P17	143
I/O	7	-	-	-	P18	146
GND	-	-	-	-	P19	-
I/O, V <sub>REF</sub>	7	P8	P132	E1	P20	149
I/O	7	P9	P131	F4	P21	152
I/O	7	-	P130	F3	P22	155
I/O	7	-	-	-	P23	158
I/O, IRDY <sup>(1)</sup>	7	P10	P129	F2	P24	161
GND	-	P11	P128	F1	P25	-
V <sub>CCO</sub>	7	P12	P127	G2	P26	-
V <sub>CCO</sub>	6	P12	P127	G2	P26	-
I/O, TRDY <sup>(1)</sup>	6	P13	P126	G1	P27	164
V <sub>CCINT</sub>	-	P14	P125	G3	P28	-
I/O	6	-	P124	G4	P29	170
I/O	6	P15	P123	H1	P30	173
I/O, V <sub>REF</sub>	6	P16	P122	H2	P31	176
GND	-	-	-	-	P32	-
I/O	6	-	-	-	P33	179
I/O	6	-	-	-	P34	182
I/O	6	-	-	-	P35	185
I/O	6	-	P121	H3	P36	188
I/O	6	P17	P120	H4	P37	191
V <sub>CCO</sub>	6	-	-	-	P39	-
GND	-	-	P119	J1	P40	-
I/O	6	P18	P118	J2	P41	194
I/O	6	P19	P117	J3	P42	197
I/O	6	-	P116	J4	P43	200

## XC2S30 Device Pinouts (Continued)

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
I/O, V <sub>REF</sub>	6	P20	P115	K1	P45	203
I/O	6	-	-	-	P46	206
I/O	6	-	P114	K2	P47	209
I/O	6	P21	P113	K3	P48	212
I/O	6	P22	P112	L1	P49	215
M1	-	P23	P111	L2	P50	218
GND	-	P24	P110	L3	P51	-
M0	-	P25	P109	M1	P52	219
V <sub>CCO</sub>	6	P26	P108	M2	P53	-
V <sub>CCO</sub>	5	P26	P107	N1	P53	-
M2	-	P27	P106	N2	P54	220
I/O	5	-	P103	K4	P57	227
I/O	5	-	-	-	P58	230
I/O, V <sub>REF</sub>	5	P30	P102	L4	P59	233
I/O	5	-	P101	M4	P61	236
I/O	5	P31	P100	N4	P62	239
I/O	5	P32	P99	K5	P63	242
GND	-	-	P98	L5	P64	-
V <sub>CCO</sub>	5	-	-	-	P65	-
V <sub>CCINT</sub>	-	P33	P97	M5	P66	-
I/O	5	-	P96	N5	P67	245
I/O	5	-	P95	K6	P68	248
I/O	5	-	-	-	P69	251
I/O	5	-	-	-	P70	254
I/O	5	-	-	-	P71	257
GND	-	-	-	-	P72	-
I/O, V <sub>REF</sub>	5	P34	P94	L6	P73	260
I/O	5	-	-	-	P74	263
I/O	5	-	P93	M6	P75	266
V <sub>CCINT</sub>	-	P35	P92	N6	P76	-
I, GCK1	5	P36	P91	M7	P77	275
V <sub>CCO</sub>	5	P37	P90	N7	P78	-
V <sub>CCO</sub>	4	P37	P90	N7	P78	-
GND	-	P38	P89	L7	P79	-
I, GCK0	4	P39	P88	K7	P80	276
I/O	4	P40	P87	N8	P81	280
I/O	4	-	P86	M8	P82	283
I/O	4	-	-	-	P83	286
I/O, V <sub>REF</sub>	4	P41	P85	L8	P84	289
GND	-	-	-	-	P85	-
I/O	4	-	-	-	P86	292

## XC2S50 Device Pinouts

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
GND	-	P143	P1	GND*	-
TMS	-	P142	P2	D3	-
I/O	7	P141	P3	C2	149
I/O	7	-	-	A2	152
I/O	7	P140	P4	B1	155
I/O	7	-	-	E3	158
I/O	7	-	P5	D2	161
GND	-	-	-	GND*	-
I/O, V <sub>REF</sub>	7	P139	P6	C1	164
I/O	7	-	P7	F3	167
I/O	7	-	-	E2	170
I/O	7	P138	P8	E4	173
I/O	7	P137	P9	D1	176
I/O	7	P136	P10	E1	179
GND	-	P135	P11	GND*	-
V <sub>CCO</sub>	7	-	P12	V <sub>CCO</sub> Bank 7*	-
V <sub>CCINT</sub>	-	-	P13	V <sub>CCINT</sub> *	-
I/O	7	P134	P14	F2	182
I/O	7	P133	P15	G3	185
I/O	7	-	-	F1	188
I/O	7	-	P16	F4	191
I/O	7	-	P17	F5	194
I/O	7	-	P18	G2	197
GND	-	-	P19	GND*	-
I/O, V <sub>REF</sub>	7	P132	P20	H3	200
I/O	7	P131	P21	G4	203
I/O	7	-	-	H2	206
I/O	7	P130	P22	G5	209
I/O	7	-	P23	H4	212
I/O, IRDY <sup>(1)</sup>	7	P129	P24	G1	215
GND	-	P128	P25	GND*	-
V <sub>CCO</sub>	7	P127	P26	V <sub>CCO</sub> Bank 7*	-
V <sub>CCO</sub>	6	P127	P26	V <sub>CCO</sub> Bank 6*	-
I/O, TRDY <sup>(1)</sup>	6	P126	P27	J2	218
V <sub>CCINT</sub>	-	P125	P28	V <sub>CCINT</sub> *	-
I/O	6	P124	P29	H1	224
I/O	6	-	-	J4	227
I/O	6	P123	P30	J1	230
I/O, V <sub>REF</sub>	6	P122	P31	J3	233

## XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name		TQ144	PQ208	FG256	Bndry Scan
Function	Bank				
GND	-	-	P32	GND*	-
I/O	6	-	P33	K5	236
I/O	6	-	P34	K2	239
I/O	6	-	P35	K1	242
I/O	6	-	-	K3	245
I/O	6	P121	P36	L1	248
I/O	6	P120	P37	L2	251
V <sub>CCINT</sub>	-	-	P38	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	6	-	P39	V <sub>CCO</sub> Bank 6*	-
GND	-	P119	P40	GND*	-
I/O	6	P118	P41	K4	254
I/O	6	P117	P42	M1	257
I/O	6	P116	P43	L4	260
I/O	6	-	-	M2	263
I/O	6	-	P44	L3	266
I/O, V <sub>REF</sub>	6	P115	P45	N1	269
GND	-	-	-	GND*	-
I/O	6	-	P46	P1	272
I/O	6	-	-	L5	275
I/O	6	P114	P47	N2	278
I/O	6	-	-	M4	281
I/O	6	P113	P48	R1	284
I/O	6	P112	P49	M3	287
M1	-	P111	P50	P2	290
GND	-	P110	P51	GND*	-
M0	-	P109	P52	N3	291
V <sub>CCO</sub>	6	P108	P53	V <sub>CCO</sub> Bank 6*	-
V <sub>CCO</sub>	5	P107	P53	V <sub>CCO</sub> Bank 5*	-
M2	-	P106	P54	R3	292
I/O	5	-	-	N5	299
I/O	5	P103	P57	T2	302
I/O	5	-	-	P5	305
I/O	5	-	P58	T3	308
GND	-	-	-	GND*	-
I/O, V <sub>REF</sub>	5	P102	P59	T4	311
I/O	5	-	P60	M6	314
I/O	5	-	-	T5	317
I/O	5	P101	P61	N6	320
I/O	5	P100	P62	R5	323

## XC2S150 Device Pinouts

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	221
I/O	7	-	-	E4	224
I/O	7	-	-	C1	227
I/O	7	-	A2	F5	230
GND	-	-	GND*	GND*	-
I/O	7	P4	B1	D2	233
I/O	7	-	-	E3	236
I/O	7	-	-	F4	239
I/O	7	-	E3	G5	242
I/O	7	P5	D2	F3	245
GND	-	-	GND*	GND*	-
V <sub>CCO</sub>	7	-	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
I/O, V <sub>REF</sub>	7	P6	C1	E2	248
I/O	7	P7	F3	E1	251
I/O	7	-	-	G4	254
I/O	7	-	-	G3	257
I/O	7	-	E2	H5	260
I/O	7	P8	E4	F2	263
I/O	7	-	-	F1	266
I/O, V <sub>REF</sub>	7	P9	D1	H4	269
I/O	7	P10	E1	G1	272
GND	-	P11	GND*	GND*	-
V <sub>CCO</sub>	7	P12	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
V <sub>CCINT</sub>	-	P13	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	7	P14	F2	H3	275
I/O	7	P15	G3	H2	278
I/O	7	-	-	H1	284
I/O	7	-	F1	J5	287
I/O	7	P16	F4	J2	290
I/O	7	-	-	J3	293
I/O	7	P17	F5	K5	299
I/O	7	P18	G2	K1	302
GND	-	P19	GND*	GND*	-
V <sub>CCO</sub>	7	-	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
I/O, V <sub>REF</sub>	7	P20	H3	K3	305
I/O	7	P21	G4	K4	308
I/O	7	-	H2	L6	311

## XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	7	P22	G5	L1	314
I/O	7	-	-	L5	317
I/O	7	P23	H4	L4	320
I/O, IRDY <sup>(1)</sup>	7	P24	G1	L3	323
GND	-	P25	GND*	GND*	-
V <sub>CCO</sub>	7	P26	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-
V <sub>CCO</sub>	6	P26	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
I/O, TRDY <sup>(1)</sup>	6	P27	J2	M1	326
V <sub>CCINT</sub>	-	P28	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	6	-	-	M6	332
I/O	6	P29	H1	M3	335
I/O	6	-	J4	M4	338
I/O	6	P30	J1	M5	341
I/O, V <sub>REF</sub>	6	P31	J3	N2	344
V <sub>CCO</sub>	6	-	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	347
I/O	6	P34	K2	N4	350
I/O	6	-	-	N5	356
I/O	6	P35	K1	P2	359
I/O	6	-	K3	P4	362
I/O	6	-	-	R1	365
I/O	6	P36	L1	P3	371
I/O	6	P37	L2	R2	374
V <sub>CCINT</sub>	-	P38	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	6	P39	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	377
I/O, V <sub>REF</sub>	6	P42	M1	R4	380
I/O	6	-	-	T2	383
I/O	6	P43	L4	U1	386
I/O	6	-	M2	R5	389
I/O	6	-	-	V1	392
I/O	6	-	-	T5	395
I/O	6	P44	L3	U2	398
I/O, V <sub>REF</sub>	6	P45	N1	T3	401
V <sub>CCO</sub>	6	-	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
GND	-	-	GND*	GND*	-

## XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	6	P46	P1	T4	404
I/O	6	-	L5	W1	407
I/O	6	-	-	V2	410
I/O	6	-	-	U4	413
I/O	6	P47	N2	Y1	416
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	419
I/O	6	-	-	V3	422
I/O	6	-	-	V4	425
I/O	6	P48	R1	Y2	428
I/O	6	P49	M3	W3	431
M1	-	P50	P2	U5	434
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	435
V <sub>CCO</sub>	6	P53	V <sub>CCO</sub> Bank 6*	V <sub>CCO</sub> Bank 6*	-
V <sub>CCO</sub>	5	P53	V <sub>CCO</sub> Bank 5*	V <sub>CCO</sub> Bank 5*	-
M2	-	P54	R3	Y4	436
I/O	5	-	-	W5	443
I/O	5	-	-	AB3	446
I/O	5	-	N5	V7	449
GND	-	-	GND*	GND*	-
I/O	5	P57	T2	Y6	452
I/O	5	-	-	AA4	455
I/O	5	-	-	AB4	458
I/O	5	-	P5	W6	461
I/O	5	P58	T3	Y7	464
GND	-	-	GND*	GND*	-
V <sub>CCO</sub>	5	-	V <sub>CCO</sub> Bank 5*	V <sub>CCO</sub> Bank 5*	-
I/O, V <sub>REF</sub>	5	P59	T4	AA5	467
I/O	5	P60	M6	AB5	470
I/O	5	-	-	V8	473
I/O	5	-	-	AA6	476
I/O	5	-	T5	AB6	479
I/O	5	P61	N6	AA7	482
I/O	5	-	-	W7	485
I/O, V <sub>REF</sub>	5	P62	R5	W8	488
I/O	5	P63	P6	Y8	491
GND	-	P64	GND*	GND*	-

## XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V <sub>CCO</sub>	5	P65	V <sub>CCO</sub> Bank 5*	V <sub>CCO</sub> Bank 5*	-
V <sub>CCINT</sub>	-	P66	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	5	P67	R6	AA8	494
I/O	5	P68	M7	V9	497
I/O	5	-	-	W9	503
I/O	5	-	-	AB9	506
I/O	5	P69	N7	Y9	509
I/O	5	-	-	V10	512
I/O	5	P70	T6	W10	518
I/O	5	P71	P7	AB10	521
GND	-	P72	GND*	GND*	-
V <sub>CCO</sub>	5	-	V <sub>CCO</sub> Bank 5*	V <sub>CCO</sub> Bank 5*	-
I/O, V <sub>REF</sub>	5	P73	P8	Y10	524
I/O	5	P74	R7	V11	527
I/O	5	-	T7	W11	530
I/O	5	P75	T8	AB11	533
I/O	5	-	-	U11	536
V <sub>CCINT</sub>	-	P76	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I, GCK1	5	P77	R8	Y11	545
V <sub>CCO</sub>	5	P78	V <sub>CCO</sub> Bank 5*	V <sub>CCO</sub> Bank 5*	-
V <sub>CCO</sub>	4	P78	V <sub>CCO</sub> Bank 4*	V <sub>CCO</sub> Bank 4*	-
GND	-	P79	GND*	GND*	-
I, GCK0	4	P80	N8	W12	546
I/O	4	P81	N9	U12	550
I/O	4	-	-	V12	553
I/O	4	P82	R9	Y12	556
I/O	4	-	N10	AA12	559
I/O	4	P83	T9	AB13	562
I/O, V <sub>REF</sub>	4	P84	P9	AA13	565
V <sub>CCO</sub>	4	-	V <sub>CCO</sub> Bank 4*	V <sub>CCO</sub> Bank 4*	-
GND	-	P85	GND*	GND*	-
I/O	4	P86	M10	Y13	568
I/O	4	P87	R10	V13	571
I/O	4	-	-	W14	577
I/O	4	P88	P10	AA14	580
I/O	4	-	-	V14	583
I/O	4	-	-	Y14	586
I/O	4	P89	T10	AB15	592

## XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O, IRDY <sup>(1)</sup>	2	P132	H16	L20	767
I/O	2	P133	H14	L17	770
I/O	2	-	-	L18	773
I/O	2	P134	H15	L21	776
I/O	2	-	J13	L22	779
I/O (D3)	2	P135	G16	K20	782
I/O, V <sub>REF</sub>	2	P136	H13	K21	785
V <sub>CCO</sub>	2	-	V <sub>CCO</sub> Bank 2*	V <sub>CCO</sub> Bank 2*	-
GND	-	P137	GND*	GND*	-
I/O	2	P138	G14	K22	788
I/O	2	P139	G15	J21	791
I/O	2	-	-	J20	797
I/O	2	P140	G12	J18	800
I/O	2	-	F16	J22	803
I/O	2	-	-	J19	806
I/O	2	P141	G13	H19	812
I/O (D2)	2	P142	F15	H20	815
V <sub>CCINT</sub>	-	P143	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	2	P144	V <sub>CCO</sub> Bank 2*	V <sub>CCO</sub> Bank 2*	-
GND	-	P145	GND*	GND*	-
I/O (D1)	2	P146	E16	H22	818
I/O, V <sub>REF</sub>	2	P147	F14	H18	821
I/O	2	-	-	G21	824
I/O	2	P148	D16	G18	827
I/O	2	-	F12	G20	830
I/O	2	-	-	G19	833
I/O	2	-	-	F22	836
I/O	2	P149	E15	F19	839
I/O, V <sub>REF</sub>	2	P150	F13	F21	842
V <sub>CCO</sub>	2	-	V <sub>CCO</sub> Bank 2*	V <sub>CCO</sub> Bank 2*	-
GND	-	-	GND*	GND*	-
I/O	2	P151	E14	F20	845
I/O	2	-	C16	F18	848
I/O	2	-	-	E22	851
I/O	2	-	-	E21	854
I/O	2	P152	E13	D22	857
GND	-	-	GND*	GND*	-
I/O	2	-	B16	E20	860
I/O	2	-	-	D21	863

## XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	2	-	-	C22	866
I/O (DIN, D0)	2	P153	D14	D20	869
I/O (DOUT, BUSY)	2	P154	C15	C21	872
CCLK	2	P155	D15	B22	875
V <sub>CCO</sub>	2	P156	V <sub>CCO</sub> Bank 2*	V <sub>CCO</sub> Bank 2*	-
V <sub>CCO</sub>	1	P156	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
TDO	2	P157	B14	A21	-
GND	-	P158	GND*	GND*	-
TDI	-	P159	A15	B20	-
I/O ( $\overline{\text{CS}}$ )	1	P160	B13	C19	0
I/O ( $\overline{\text{WRITE}}$ )	1	P161	C13	A20	3
I/O	1	-	-	B19	6
I/O	1	-	-	C18	9
I/O	1	-	C12	D17	12
GND	-	-	GND*	GND*	-
I/O	1	P162	A14	A19	15
I/O	1	-	-	B18	18
I/O	1	-	-	E16	21
I/O	1	-	D12	C17	24
I/O	1	P163	B12	D16	27
GND	-	-	GND*	GND*	-
V <sub>CCO</sub>	1	-	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
I/O, V <sub>REF</sub>	1	P164	C11	A18	30
I/O	1	P165	A13	B17	33
I/O	1	-	-	E15	36
I/O	1	-	-	A17	39
I/O	1	-	D11	D15	42
I/O	1	P166	A12	C16	45
I/O	1	-	-	D14	48
I/O, V <sub>REF</sub>	1	P167	E11	E14	51
I/O	1	P168	B11	A16	54
GND	-	P169	GND*	GND*	-
V <sub>CCO</sub>	1	P170	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
V <sub>CCINT</sub>	-	P171	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	1	P172	A11	C15	57
I/O	1	P173	C10	B15	60
I/O	1	-	-	A15	66
I/O	1	-	-	F12	69

## XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	1	P174	B10	C14	72
I/O	1	-	-	B14	75
I/O	1	P175	D10	D13	81
I/O	1	P176	A10	C13	84
GND	-	P177	GND*	GND*	-
V <sub>CCO</sub>	1	-	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
I/O, V <sub>REF</sub>	1	P178	B9	B13	87
I/O	1	P179	E10	E12	90
I/O	1	-	A9	B12	93
I/O	1	P180	D9	D12	96
I/O	1	-	-	C12	99
I/O	1	P181	A8	D11	102
I, GCK2	1	P182	C9	A11	108
GND	-	P183	GND*	GND*	-
V <sub>CCO</sub>	1	P184	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
V <sub>CCO</sub>	0	P184	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
I, GCK3	0	P185	B8	C11	109
V <sub>CCINT</sub>	-	P186	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	0	-	-	E11	116
I/O	0	P187	A7	A10	119
I/O	0	-	D8	B10	122
I/O	0	P188	A6	C10	125
I/O, V <sub>REF</sub>	0	P189	B7	A9	128
V <sub>CCO</sub>	0	-	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
GND	-	P190	GND*	GND*	-
I/O	0	P191	C8	B9	131
I/O	0	P192	D7	E10	134
I/O	0	-	-	D10	140
I/O	0	P193	E7	A8	143
I/O	0	-	-	D9	146
I/O	0	-	-	B8	149
I/O	0	P194	C7	E9	155
I/O	0	P195	B6	A7	158

## XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V <sub>CCINT</sub>	-	P196	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	0	P197	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
GND	-	P198	GND*	GND*	-
I/O	0	P199	A5	B7	161
I/O, V <sub>REF</sub>	0	P200	C6	E8	164
I/O	0	-	-	D8	167
I/O	0	P201	B5	C7	170
I/O	0	-	D6	D7	173
I/O	0	-	-	B6	176
I/O	0	-	-	A5	179
I/O	0	P202	A4	D6	182
I/O, V <sub>REF</sub>	0	P203	B4	C6	185
V <sub>CCO</sub>	0	-	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
GND	-	-	GND*	GND*	-
I/O	0	P204	E6	B5	188
I/O	0	-	D5	E7	191
I/O	0	-	-	A4	194
I/O	0	-	-	E6	197
I/O	0	P205	A3	B4	200
GND	-	-	GND*	GND*	-
I/O	0	-	C5	A3	203
I/O	0	-	-	B3	206
I/O	0	-	-	D5	209
I/O	0	P206	B3	C5	212
TCK	-	P207	C4	C4	-
V <sub>CCO</sub>	0	P208	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
V <sub>CCO</sub>	7	P208	V <sub>CCO</sub> Bank 7*	V <sub>CCO</sub> Bank 7*	-

04/18/01

### Notes:

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND\*, V<sub>CCINT</sub>\*, V<sub>CCO</sub> Bank 0\*, V<sub>CCO</sub> Bank 1\*, V<sub>CCO</sub> Bank 2\*, V<sub>CCO</sub> Bank 3\*, V<sub>CCO</sub> Bank 4\*, V<sub>CCO</sub> Bank 5\*, V<sub>CCO</sub> Bank 6\*, V<sub>CCO</sub> Bank 7\* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on V<sub>CCO</sub> banking.



## XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V <sub>CCO</sub>	1	P156	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
TDO	2	P157	B14	A21	-
GND	-	P158	GND*	GND*	-
TDI	-	P159	A15	B20	-
I/O ( $\overline{\text{CS}}$ )	1	P160	B13	C19	0
I/O ( $\overline{\text{WRITE}}$ )	1	P161	C13	A20	3
I/O	1	-	-	B19	9
I/O	1	-	-	C18	12
I/O	1	-	C12	D17	15
GND	-	-	GND*	GND*	-
I/O, V <sub>REF</sub>	1	P162	A14	A19	18
I/O	1	-	-	B18	21
I/O	1	-	-	E16	27
I/O	1	-	D12	C17	30
I/O	1	P163	B12	D16	33
GND	-	-	GND*	GND*	-
V <sub>CCO</sub>	1	-	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
I/O, V <sub>REF</sub>	1	P164	C11	A18	36
I/O	1	P165	A13	B17	39
I/O	1	-	-	E15	42
I/O	1	-	-	A17	45
I/O	1	-	D11	D15	48
GND	-	-	GND*	GND*	-
I/O	1	P166	A12	C16	51
I/O	1	-	-	D14	54
I/O, V <sub>REF</sub>	1	P167	E11	E14	60
I/O	1	P168	B11	A16	63
GND	-	P169	GND*	GND*	-
V <sub>CCO</sub>	1	P170	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
V <sub>CCINT</sub>	-	P171	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	1	P172	A11	C15	66
I/O	1	P173	C10	B15	69
I/O	1	-	-	E13	72
I/O	1	-	-	A15	75
I/O	1	-	-	F12	78
GND	-	-	GND*	GND*	-
I/O	1	P174	B10	C14	81
I/O	1	-	-	B14	84
I/O	1	-	-	A14	87

## XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	1	P175	D10	D13	90
I/O	1	P176	A10	C13	93
GND	-	P177	GND*	GND*	-
V <sub>CCO</sub>	1	-	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
I/O, V <sub>REF</sub>	1	P178	B9	B13	96
I/O	1	P179	E10	E12	99
I/O	1	-	-	A13	105
I/O	1	-	A9	B12	108
I/O	1	P180	D9	D12	111
I/O	1	-	-	C12	114
I/O	1	P181	A8	D11	120
I, GCK2	1	P182	C9	A11	126
GND	-	P183	GND*	GND*	-
V <sub>CCO</sub>	1	P184	V <sub>CCO</sub> Bank 1*	V <sub>CCO</sub> Bank 1*	-
V <sub>CCO</sub>	0	P184	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
I, GCK3	0	P185	B8	C11	127
V <sub>CCINT</sub>	-	P186	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
I/O	0	-	-	E11	137
I/O	0	P187	A7	A10	140
I/O	0	-	D8	B10	143
I/O	0	-	-	F11	146
I/O	0	P188	A6	C10	152
I/O, V <sub>REF</sub>	0	P189	B7	A9	155
V <sub>CCO</sub>	0	-	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-
GND	-	P190	GND*	GND*	-
I/O	0	P191	C8	B9	158
I/O	0	P192	D7	E10	161
I/O	0	-	-	C9	164
I/O	0	-	-	D10	167
I/O	0	P193	E7	A8	170
GND	-	-	GND*	GND*	-
I/O	0	-	-	D9	173
I/O	0	-	-	B8	176
I/O	0	-	-	C8	179
I/O	0	P194	C7	E9	182
I/O	0	P195	B6	A7	185
V <sub>CCINT</sub>	-	P196	V <sub>CCINT</sub> *	V <sub>CCINT</sub> *	-
V <sub>CCO</sub>	0	P197	V <sub>CCO</sub> Bank 0*	V <sub>CCO</sub> Bank 0*	-