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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	864
Number of Logic Elements/Cells	3888
Total RAM Bits	49152
Number of I/O	140
Number of Gates	150000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s150-6pqg208c

The three IOB registers function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three registers and independent Clock Enable (CE) signals for each register. In addition to the CLK and CE control signals, the three registers share a Set/Reset (SR). For each register, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

A feature not shown in the block diagram, but controlled by the software, is polarity control. The input and output buffers and all of the IOB control signals have independent polarity controls.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up.

Table 3: **Standards Supported by I/O (Typical Values)**

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL (2-24 mA)	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	1.5
HSTL Class IV	0.9	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5V compliance, and one that does not. For 5V compliance, a zener-like structure connected to ground turns on when the output rises to approximately 6.5V. When 5V compliance is not required, a conventional clamp diode may be connected to the output supply voltage, V_{CCO}. The type of over-voltage protection can be selected independently for each pad.

All Spartan-II FPGA IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer In the Spartan-II FPGA IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signaling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See "I/O Banking," page 9.

There are optional pull-up and pull-down resistors at each input for use after configuration.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signaling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signaling standards, the output high voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See "I/O Banking".

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

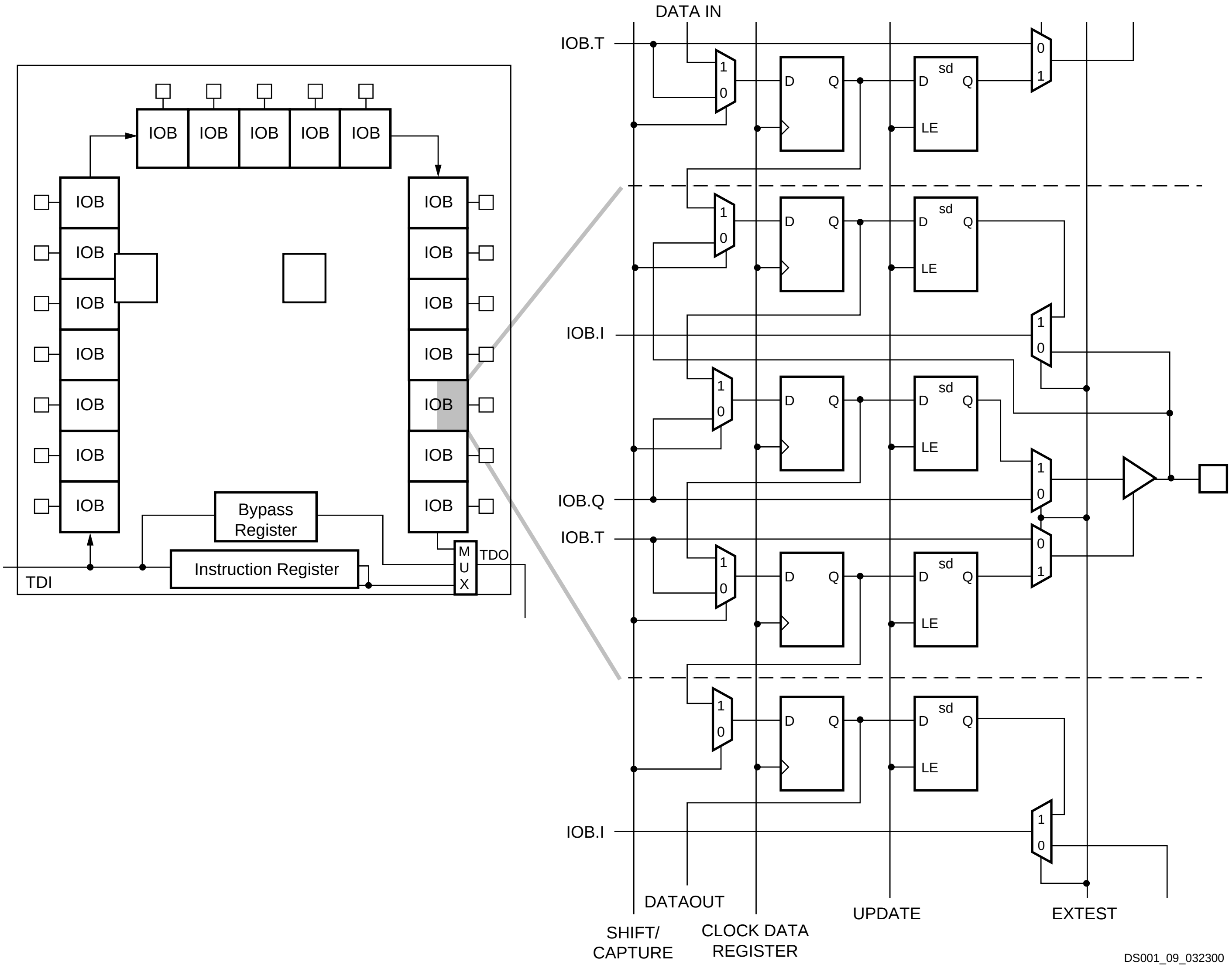


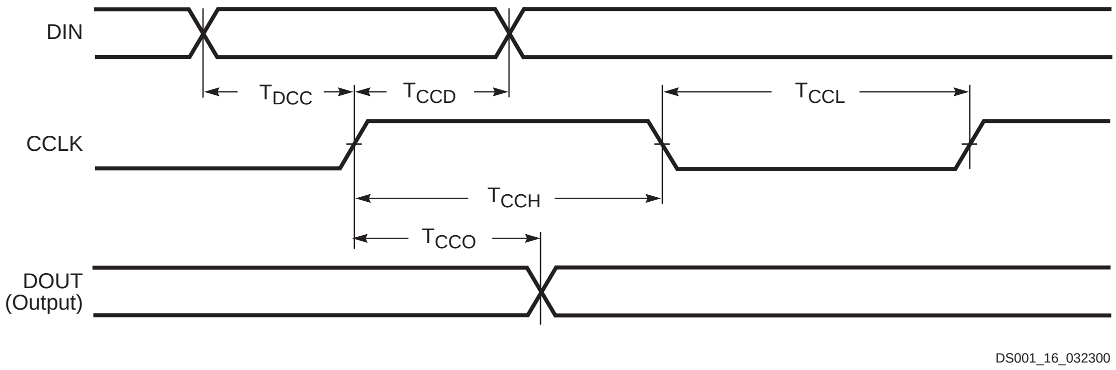
Figure 9: **Spartan-II Family Boundary Scan Logic**

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the Downloads area.



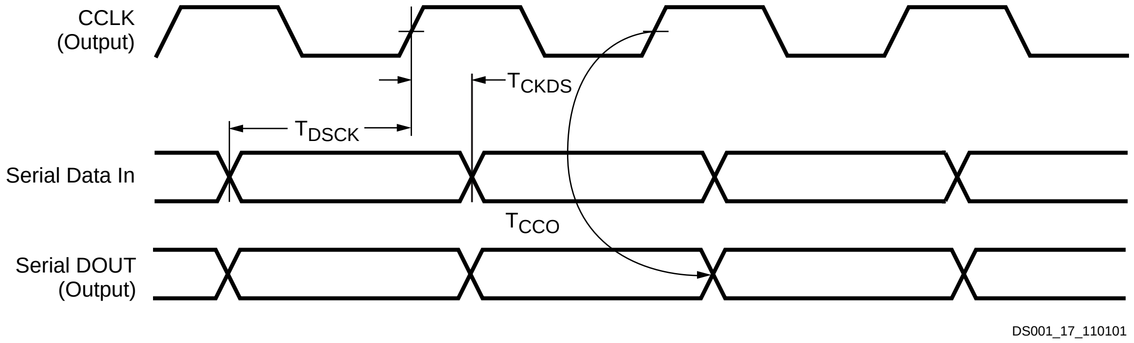
Symbol		Description		Units
T_{DCC}	CCLK	DIN setup	5	ns, min
T_{CCD}		DIN hold	0	ns, min
T_{CCO}		DOUT	12	ns, max
T_{CCH}		High time	5	ns, min
T_{CCL}		Low time	5	ns, min
F_{CC}		Maximum frequency	66	MHz, max

Figure 16: **Slave Serial Mode Timing**

Master Serial Mode

In Master Serial mode, the CCLK output of the FPGA drives a Xilinx PROM which feeds a serial stream of configuration data to the FPGA's DIN input. Figure 15 shows a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in Master Serial mode should be connected as shown for the device on the left side. Master Serial mode is selected by a <00x> on the mode pins (M0, M1, M2). The PROM RESET pin is driven by INIT, and CE input is driven by DONE. The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in the Xilinx software. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point, the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The frequency of the CCLK signal created by the internal oscillator has a variance of +45%, –30% from the specified value.

Figure 17 shows the timing for Master Serial configuration. The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.



Symbol		Description		Units
T_{DSCK}	CCLK	DIN setup	5.0	ns, min
T_{CKDS}		DIN hold	0.0	ns, min
		Frequency tolerance with respect to nominal	+45%, –30%	-

Figure 17: **Master Serial Mode Timing**

Slave Parallel Mode

The Slave Parallel mode is the fastest configuration option. Byte-wide data is written into the FPGA. A BUSY flag is provided for controlling the flow of data at a clock frequency F_{CCNH} above 50 MHz.

Figure 18, page 24 shows the connections for two Spartan-II devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

If a configuration file of the format .bit, .rbt, or non-swapped HEX is used for parallel programming, then the most significant bit (i.e. the left-most bit of each configuration byte, as displayed in a text editor) must be routed to the D0 input on the FPGA.

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by de-asserting WRITE. See "Readback," page 25.

Creating Larger RAM Structures

The block RAM columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

Location Constraints

Block RAM instances can have LOC properties attached to them to constrain the placement. The block RAM placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form:

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

Conflict Resolution

The block RAM memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
  - The write succeeds
  - The data out on the writing port accurately reflects the data written.
  - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

Single Port Timing

Figure 33 shows a timing diagram for a single port of a block RAM memory. The block RAM AC switching characteristics are specified in the data sheet. The block RAM memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the block RAM memory is now disabled. The DO bus retains the last value.

Dual Port Timing

Figure 34 shows a timing diagram for a true dual-port read/write block RAM memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS}, (clock-to-clock setup) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location will be invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory will be correct, but the read port will have invalid data. At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF primitive names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24). The default is slew rate limited with 12 mA drive.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. Table 17 summarizes the output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 17: **Output Standards Compatibility Requirements**

Rule 1	Only outputs with standards which share compatible V_{CCO} may be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 39, typically implements 3-state outputs or bidirectional I/O.

With no extension or property specified for the generic OBUFT primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT primitive names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

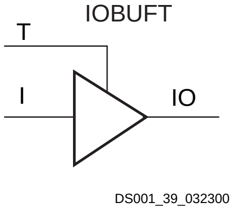


Figure 39: **3-State Output Buffer Primitive (OBUFT**

The Versatile I/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF primitive for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 40.

With no extension or property specified for the generic IOBUF primitive, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF primitive names is as follows:

ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 18 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 19 for the number of effective output power/ground pairs for each Spartan-II device and package combination.

Table 18: **Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package	
	CS, FG	PQ, TQ, VQ
LVTTL Slow Slew Rate, 2 mA drive	68	36
LVTTL Slow Slew Rate, 4 mA drive	41	20
LVTTL Slow Slew Rate, 6 mA drive	29	15
LVTTL Slow Slew Rate, 8 mA drive	22	12
LVTTL Slow Slew Rate, 12 mA drive	17	9
LVTTL Slow Slew Rate, 16 mA drive	14	7
LVTTL Slow Slew Rate, 24 mA drive	9	5
LVTTL Fast Slew Rate, 2 mA drive	40	21
LVTTL Fast Slew Rate, 4 mA drive	24	12
LVTTL Fast Slew Rate, 6 mA drive	17	9
LVTTL Fast Slew Rate, 8 mA drive	13	7
LVTTL Fast Slew Rate, 12 mA drive	10	5
LVTTL Fast Slew Rate, 16 mA drive	8	4
LVTTL Fast Slew Rate, 24 mA drive	5	3
LVCMOS2	10	5
PCI	8	4
GTL	4	4
GTL+	4	4
HSTL Class I	18	9
HSTL Class III	9	5
HSTL Class IV	5	3
SSTL2 Class I	15	8
SSTL2 Class II	10	5
SSTL3 Class I	11	6
SSTL3 Class II	7	4
CTT	14	7
AGP	9	5

Notes:
1. This analysis assumes a 35 pF load for each output.

Table 19: **Effective Output Power/Ground Pairs for Spartan-II Devices**

Pkg.	Spartan-II Devices					
	XC2S 15	XC2S 30	XC2S 50	XC2S 100	XC2S 150	XC2S 200
VQ100	8	8	-	-	-	-
CS144	12	12	-	-	-	-
TQ144	12	12	12	12	-	-
PQ208	-	16	16	16	16	16
FG256	-	-	16	16	16	16
FG456	-	-	-	48	48	48

Termination Examples

Creating a design with the Versatile I/O features requires the instantiation of the desired library primitive within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the Versatile I/O features. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

SSTL3 Class I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 47. DC voltage specifications appear in Table 25 for the SSTL3_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

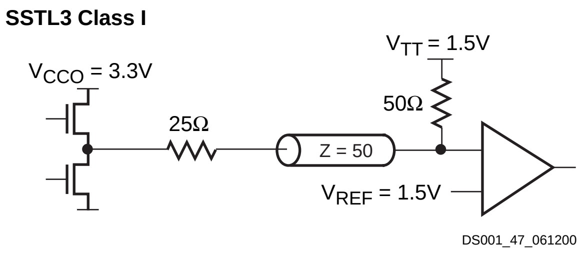


Figure 47: **Terminated SSTL3 Class I**

Table 25: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.6$	1.9	-	-
$V_{OL} \leq V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3.
2. V_{IL} minimum does not conform to the formula.

SSTL3 Class II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 48. DC voltage specifications appear in Table 26 for the SSTL3_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

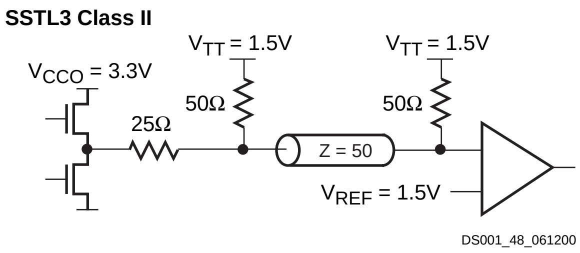


Figure 48: **Terminated SSTL3 Class II**

Table 26: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.8$	2.1	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

Power-On Requirements

Spartan-II FPGAs require that a minimum supply current I_{CCPO} be provided to the V_{CCINT} lines for a successful power-on. If more current is available, the FPGA can consume more than I_{CCPO} minimum, though this cannot adversely affect reliability.

A maximum limit for I_{CCPO} is not specified. Therefore the use of foldback/crowbar supplies and fuses deserves special attention. In these cases, limit the I_{CCPO} current to a level below the trip point for over-current protection in order to avoid inadvertently shutting down the supply.

Symbol	Description	Conditions		New Requirements(1) For Devices with Date Code 0321 or Later		Old Requirements(1) For Devices with Date Code before 0321		Units
		Junction Temperature(2)	Device Temperature Grade	Min	Max	Min	Max	
I_{CCPO}(3)	Total V_{CCINT} supply current required during power-on	$-40°C \leq T_J < -20°C$	Industrial	1.50	-	2.00	-	A
		$-20°C \leq T_J < 0°C$	Industrial	1.00	-	2.00	-	A
		$0°C \leq T_J \leq 85°C$	Commercial	0.25	-	0.50	-	A
		$85°C < T_J \leq 100°C$	Industrial	0.50	-	0.50	-	A
T_{CCPO}(4,5)	V_{CCINT} ramp time	$-40°C \leq T_J \leq 100°C$	All	-	50	-	50	ms

Notes:
1. The date code is printed on the top of the device's package. See the "Device Part Marking" section in Module 1.
2. The expected T_J range for the design determines the I_{CCPO} minimum requirement. Use the applicable ranges in the junction temperature column to find the associated current values in the appropriate new or old requirements column according to the date code. Then choose the highest of these current values to serve as the minimum I_{CCPO} requirement that must be met. For example, if the junction temperature for a given design is $-25°C \leq T_J \leq 75°C$, then the new minimum I_{CCPO} requirement is 1.5A. If $5°C \leq T_J \leq 90°C$, then the new minimum I_{CCPO} requirement is 0.5A.
3. The I_{CCPO} requirement applies for a brief time (commonly only a few milliseconds) when V_{CCINT} ramps from 0 to 2.5V.
4. The ramp time is measured from GND to V_{CCINT} max on a fully loaded board.
5. During power-on, the V_{CCINT} ramp must increase steadily in voltage with no dips.
6. For more information on designing to meet the power-on specifications, refer to the application note **XAPP450 "Power-On Current Requirements for the Spartan-II and Spartan-IIE Families"**

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
LVTTL(1)	–0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3V	–0.5	44% V_{CCINT}	60% V_{CCINT}	$V_{CCO} + 0.5$	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)
PCI, 5.0V	–0.5	0.8	2.0	5.5	0.55	2.4	Note (2)	Note (2)
GTL	–0.5	$V_{REF} - 0.05$	$V_{REF} + 0.05$	3.6	0.4	N/A	40	N/A
GTL+	–0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.6	N/A	36	N/A
HSTL I	–0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	8	–8
HSTL III	–0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	24	–8
HSTL IV	–0.5	$V_{REF} - 0.1$	$V_{REF} + 0.1$	3.6	0.4	$V_{CCO} - 0.4$	48	–8
SSTL3 I	–0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	8	–8
SSTL3 II	–0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	16	–16
SSTL2 I	–0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.6$	$V_{REF} + 0.6$	7.6	–7.6
SSTL2 II	–0.5	$V_{REF} - 0.2$	$V_{REF} + 0.2$	3.6	$V_{REF} - 0.8$	$V_{REF} + 0.8$	15.2	–15.2

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, *with* DLL (Pin-to-Pin)(1)

Symbol	Description	Device	Speed Grade			Units
			All	-6	-5	
			Min	Max	Max	
$T_{ICKOFDLL}$	Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *with* DLL.	All		2.9	3.3	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)(1)

Symbol	Description	Device	Speed Grade			Units
			All	-6	-5	
			Min	Max	Max	
T_{ICKOF}	Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *without* DLL.	XC2S15		4.5	5.4	ns
		XC2S30		4.5	5.4	ns
		XC2S50		4.5	5.4	ns
		XC2S100		4.6	5.5	ns
		XC2S150		4.6	5.5	ns
		XC2S200		4.7	5.6	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Delay Adjustments for Different Standards," page 57.

Symbol	Description	Device	Speed Grade -6 Min	Speed Grade -6 Max	Speed Grade -5 Min	Speed Grade -5 Max	Units
Propagation Delays							
T_{IOPI}	Pad to I output, no delay	All	-	0.8	-	1.0	ns
T_{IOPID}	Pad to I output, with delay	All	-	1.5	-	1.8	ns
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	-	1.7	-	2.0	ns
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S15	-	3.8	-	4.5	ns
		XC2S30	-	3.8	-	4.5	ns
		XC2S50	-	3.8	-	4.5	ns
		XC2S100	-	3.8	-	4.5	ns
		XC2S150	-	4.0	-	4.7	ns
		XC2S200	-	4.0	-	4.7	ns
Sequential Delays							
T_{IOCKIQ}	Clock CLK to output IQ	All	-	0.7	-	0.8	ns
Setup/Hold Times with Respect to Clock CLK(2)							
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	1.7 / 0	-	1.9 / 0	-	ns
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay(1)	XC2S15	3.8 / 0	-	4.4 / 0	-	ns
		XC2S30	3.8 / 0	-	4.4 / 0	-	ns
		XC2S50	3.8 / 0	-	4.4 / 0	-	ns
		XC2S100	3.8 / 0	-	4.4 / 0	-	ns
		XC2S150	3.9 / 0	-	4.6 / 0	-	ns
		XC2S200	3.9 / 0	-	4.6 / 0	-	ns
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	0.9 / 0.01	-	0.9 / 0.01	-	ns
Set/Reset Delays							
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All	-	1.1	-	1.2	ns
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	-	1.5	-	1.7	ns
T_{GSRQ}	GSR to output IQ	All	-	9.9	-	11.7	ns

Notes:

1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.
2. A zero hold time listing indicates no hold time or a negative hold time.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Propagation Delays						
T_{IOOP}	O input to pad	-	2.9	-	3.4	ns
T_{IOOLP}	O input to pad via transparent latch	-	3.4	-	4.0	ns
3-state Delays						
T_{IOTHZ}	T input to pad high-impedance(1)	-	2.0	-	2.3	ns
T_{IOTON}	T input to valid data on pad	-	3.0	-	3.6	ns
$T_{IOTLPHZ}$	T input to pad high impedance via transparent latch(1)	-	2.5	-	2.9	ns
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	-	3.5	-	4.2	ns
T_{GTS}	GTS to pad high impedance(1)	-	5.0	-	5.9	ns
Sequential Delays						
T_{IOCKP}	Clock CLK to pad	-	2.9	-	3.4	ns
T_{IOCKHZ}	Clock CLK to pad high impedance (synchronous)(1)	-	2.3	-	2.7	ns
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	-	3.3	-	4.0	ns
Setup/Hold Times with Respect to Clock CLK(2)						
T_{IOOCK} / T_{IOCKO}	O input	1.1 / 0	-	1.3 / 0	-	ns
$T_{IOOCECK}$ / $T_{IOCKOCE}$	OCE input	0.9 / 0.01	-	0.9 / 0.01	-	ns
$T_{IOSRCKO}$ / $T_{IOCKOSR}$	SR input (OFF)	1.2 / 0	-	1.3 / 0	-	ns
T_{IOTCK} / T_{IOCKT}	3-state setup times, T input	0.8 / 0	-	0.9 / 0	-	ns
$T_{IOTCECK}$ / $T_{IOCKTCE}$	3-state setup times, TCE input	1.0 / 0	-	1.0 / 0	-	ns
$T_{IOSRCKT}$ / $T_{IOCKTSR}$	3-state setup times, SR input (TFF)	1.1 / 0	-	1.2 / 0	-	ns
Set/Reset Delays						
T_{IOSRP}	SR input to pad (asynchronous)	-	3.7	-	4.4	ns
T_{IOSRHZ}	SR input to pad high impedance (asynchronous)(1)	-	3.1	-	3.7	ns
T_{IOSRON}	SR input to valid data on pad (asynchronous)	-	4.1	-	4.9	ns
T_{IOGSRQ}	GSR to pad	-	9.9	-	11.7	ns

Notes:

1. Three-state turn-off delays should not be adjusted.
2. A zero hold time listing indicates no hold time or a negative hold time.

Clock Distribution Guidelines(1)

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
GCLK Clock Skew				
$T_{GSKEWIOB}$	Global clock skew between IOB flip-flops	0.13	0.14	ns

Notes:

1. These clock distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

T_{GPIO} is specified for LVTTL levels. For other standards, adjust T_{GPIO} with the values shown in "I/O Standard Global Clock Input Adjustments".

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
GCLK IOB and Buffer				
T_{GPIO}	Global clock pad to output	0.7	0.8	ns
T_{GIO}	Global clock buffer I input to O output	0.7	0.8	ns

I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Data Input Delay Adjustments					
$T_{GPLVTTL}$	Standard-specific global clock input delay adjustments	LVTTL	0	0	ns
$T_{GPLVCMOS2}$		LVCMOS2	–0.04	–0.05	ns
$T_{GPPCI33\_3}$		PCI, 33 MHz, 3.3V	–0.11	–0.13	ns
$T_{GPPCI33\_5}$		PCI, 33 MHz, 5.0V	0.26	0.30	ns
$T_{GPPCI66\_3}$		PCI, 66 MHz, 3.3V	–0.11	–0.13	ns
T_{GPGTL}		GTL	0.80	0.84	ns
T_{GPGTLP}		GTL+	0.71	0.73	ns
T_{GPHSTL}		HSTL	0.63	0.64	ns
$T_{GPSSTL2}$		SSTL2	0.52	0.51	ns
$T_{GPSSTL3}$		SSTL3	0.56	0.55	ns
T_{GPCTT}		CTT	0.62	0.62	ns
T_{GPAGP}		AGP	0.54	0.53	ns

Notes:

1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	60	200	60	180	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	25	100	25	90	MHz
$T_{DLLPWHF}$	Input clock pulse width (CLKDLLHF)	2.0	-	2.4	-	ns
$T_{DLLPWLF}$	Input clock pulse width (CLKDLL)	2.5	-	3.0	-	ns

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Figure 52, page 63, provides definitions for various parameters in the table below.

Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(1)		-	±60	-	±60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(2)		-	±100	-	±100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(3)		-	±140	-	±140	ps
T_{PHIOM}	Maximum phase difference between CLKIN and CLKO(4)		-	±160	-	±160	ps
T_{PHOOM}	Maximum phase difference between clock outputs on the DLL(5)		-	±200	-	±200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

Spartan-II FPGA Family: Pinout Tables

DS001-4 (v2.8) June 13, 2008

Product Specification

Introduction

This section describes how the various pins on a Spartan®-II FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-II FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-II FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-II FPGA packages, as outlined in Table 35.

Table 35: **Pin Definitions**

Pin Name	Dedicated	Direction	Description
GCK0, GCK1, GCK2, GCK3	No	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin. It is an input for slave-parallel and slave-serial modes, and output in master-serial mode.
$\overline{\text{PROGRAM}}$	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
$\overline{\text{INIT}}$	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. This pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{\text{WRITE}}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{\text{CS}}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	Power supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power supply pins for output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx® PCI cores. If the cores are not used, these pins are available as user I/Os.

Table 36: **Spartan-II Family Package Options**

Package	Leads	Type	Maximum I/O	Lead Pitch (mm)	Footprint Area (mm)	Height (mm)	Mass[(1)] (g)
VQ100 / VQG100	100	Very Thin Quad Flat Pack (VQFP)	60	0.5	16 x 16	1.20	0.6
TQ144 / TQG144	144	Thin Quad Flat Pack (TQFP)	92	0.5	22 x 22	1.60	1.4
CS144 / CSG144	144	Chip Scale Ball Grid Array (CSBGA)	92	0.8	12 x 12	1.20	0.3
PQ208 / PQG208	208	Plastic Quad Flat Pack (PQFP)	140	0.5	30.6 x 30.6	3.70	5.3
FG256 / FGG256	256	Fine-pitch Ball Grid Array (FBGA)	176	1.0	17 x 17	2.00	0.9
FG456 / FGG456	456	Fine-pitch Ball Grid Array (FBGA)	284	1.0	23 x 23	2.60	2.2

Notes:

1. Package mass is ±10%.

Note: Some early versions of Spartan-II devices, including the XC2S15 and XC2S30 ES devices and the XC2S150 with date code 0045 or earlier, included a power-down pin. For more information, see Answer Record 10500.

VCCO Banks

Some of the I/O standards require specific V_{CCO} voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3 in Module 2). Each bank has multiple V_{CCO} pins which must be connected to the same voltage. In the smaller packages, the V_{CCO} pins are connected between banks, effectively reducing the number of independent banks available (see Table 37). These interconnected banks are shown in the Pinout Tables with V_{CCO} pads for multiple banks connected to the same pin.

Table 37: **Independent VCCO Banks Available**

Package	VQ100 PQ208	CS144 TQ144	FG256 FG456
Independent Banks	1	4	8

Package Overview

Table 36 shows the six low-cost, space-saving production package styles for the Spartan-II family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra ‘G’ in the package style name. For example, the standard “CS144” package becomes “CSG144” when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 38.

For additional package information, see UG112: *Device Package User Guide*.

Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 38.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

Table 38: **Xilinx Package Documentation**

Package	Drawing	MDDS
VQ100	Package Drawing	PK173_VQ100
VQG100		PK130_VQG100
TQ144	Package Drawing	PK169_TQ144
TQG144		PK126_TQG144
CS144	Package Drawing	PK149_CS144
CSG144		PK103_CSG144
PQ208	Package Drawing	PK166_PQ208
PQG208		PK123_PQG208
FG256	Package Drawing	PK151_FG256
FGG256		PK105_FGG256
FG456	Package Drawing	PK154_FG456
FGG456		PK109_FGG456

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name						
Function	**Bank**	**TQ144**	**PQ208**	**FG256**	**FG456**	**Bndry Scan**
I/O	0	-	P188	A6	C10	107
I/O, V_{REF}	0	P12	P189	B7	A9	110
GND	-	-	P190	GND*	GND*	-
I/O	0	-	P191	C8	B9	113
I/O	0	-	P192	D7	E10	116
I/O	0	-	P193	E7	A8	122
I/O	0	-	-	-	D9	125
I/O	0	P11	P194	C7	E9	128
I/O	0	P10	P195	B6	A7	131
V_{CCINT}	-	P9	P196	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	0	-	P197	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
GND	-	P8	P198	GND*	GND*	-
I/O	0	P7	P199	A5	B7	134
I/O, V_{REF}	0	P6	P200	C6	E8	137
I/O	0	-	-	-	D8	140
I/O	0	-	P201	B5	C7	143
I/O	0	-	-	D6	D7	146
I/O	0	-	P202	A4	D6	152
I/O, V_{REF}	0	P5	P203	B4	C6	155
V_{CCO}	0	-	-	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
GND	-	-	-	GND*	GND*	-
I/O	0	-	P204	E6	B5	158
I/O	0	-	-	D5	E7	161
I/O	0	-	-	-	E6	164
I/O	0	P4	P205	A3	B4	167
I/O	0	-	-	C5	A3	170
I/O	0	P3	P206	B3	C5	176
TCK	-	P2	P207	C4	C4	-
V_{CCO}	0	P1	P208	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
V_{CCO}	7	P144	P208	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-

04/18/01

Notes:

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S150 Package Pins

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

11/02/00

FG256

V_{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V_{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V_{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V_{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V_{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V_{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V_{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V_{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V_{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

11/02/00

Additional XC2S150 Package Pins *(Continued)*

FG456

V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					
F7	F8	F9	F10	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U7	U8	U9	U10
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A6	A12	A13	A14	B11
B16	C2	C8	C9	D1	D4
D18	D19	E13	E17	E19	F11
G2	G22	H21	J1	J4	K2
K18	K19	L2	L19	M2	M17
M21	N1	P1	P5	P22	R3
R20	R22	U3	U18	V6	W4
W13	W15	W19	Y5	Y22	AA1
AA3	AA9	AA10	AA11	AA16	AB7
AB8	AB12	AB14	AB21	-	-

11/02/00

XC2S200 Device Pinouts

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	257
I/O	7	-	-	E4	263
I/O	7	-	-	C1	266
I/O	7	-	A2	F5	269
GND	-	-	GND*	GND*	-
I/O, V_{REF}	7	P4	B1	D2	272
I/O	7	-	-	E3	275
I/O	7	-	-	F4	281
GND	-	-	GND*	GND*	-
I/O	7	-	E3	G5	284
I/O	7	P5	D2	F3	287
GND	-	-	GND*	GND*	-
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P6	C1	E2	290
I/O	7	P7	F3	E1	293
I/O	7	-	-	G4	296
I/O	7	-	-	G3	299
I/O	7	-	E2	H5	302
GND	-	-	GND*	GND*	-
I/O	7	P8	E4	F2	305
I/O	7	-	-	F1	308
I/O, V_{REF}	7	P9	D1	H4	314
I/O	7	P10	E1	G1	317
GND	-	P11	GND*	GND*	-
V_{CCO}	7	P12	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCINT}	-	P13	V_{CCINT}*	V_{CCINT}*	-
I/O	7	P14	F2	H3	320
I/O	7	P15	G3	H2	323
I/O	7	-	-	J4	326
I/O	7	-	-	H1	329
I/O	7	-	F1	J5	332
GND	-	-	GND*	GND*	-
I/O	7	P16	F4	J2	335
I/O	7	-	-	J3	338
I/O	7	-	-	J1	341
I/O	7	P17	F5	K5	344
I/O	7	P18	G2	K1	347
GND	-	P19	GND*	GND*	-

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P20	H3	K3	350
I/O	7	P21	G4	K4	353
I/O	7	-	-	K2	359
I/O	7	-	H2	L6	362
I/O	7	P22	G5	L1	365
I/O	7	-	-	L5	368
I/O	7	P23	H4	L4	374
I/O, IRDY(1)	7	P24	G1	L3	377
GND	-	P25	GND*	GND*	-
V_{CCO}	7	P26	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCO}	6	P26	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P27	J2	M1	380
V_{CCINT}	-	P28	V_{CCINT}*	V_{CCINT}*	-
I/O	6	-	-	M6	389
I/O	6	P29	H1	M3	392
I/O	6	-	J4	M4	395
I/O	6	-	-	N1	398
I/O	6	P30	J1	M5	404
I/O, V_{REF}	6	P31	J3	N2	407
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	410
I/O	6	P34	K2	N4	413
I/O	6	-	-	P1	416
I/O	6	-	-	N5	419
I/O	6	P35	K1	P2	422
GND	-	-	GND*	GND*	-
I/O	6	-	K3	P4	425
I/O	6	-	-	R1	428
I/O	6	-	-	P5	431
I/O	6	P36	L1	P3	434
I/O	6	P37	L2	R2	437
V_{CCINT}	-	P38	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	6	P39	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	440
I/O, V_{REF}	6	P42	M1	R4	443

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	6	-	-	T2	449
I/O	6	P43	L4	U1	452
GND	-	-	GND*	GND*	-
I/O	6	-	M2	R5	455
I/O	6	-	-	V1	458
I/O	6	-	-	T5	461
I/O	6	P44	L3	U2	464
I/O, V_{REF}	6	P45	N1	T3	467
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-
I/O	6	P46	P1	T4	470
I/O	6	-	L5	W1	473
GND	-	-	GND*	GND*	-
I/O	6	-	-	V2	476
I/O	6	-	-	U4	482
I/O, V_{REF}	6	P47	N2	Y1	485
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	488
I/O	6	-	-	V3	491
I/O	6	-	-	V4	494
I/O	6	P48	R1	Y2	500
I/O	6	P49	M3	W3	503
M1	-	P50	P2	U5	506
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	507
V_{CCO}	6	P53	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
V_{CCO}	5	P53	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
M2	-	P54	R3	Y4	508
I/O	5	-	-	W5	518
I/O	5	-	-	AB3	521
I/O	5	-	N5	V7	524
GND	-	-	GND*	GND*	-
I/O, V_{REF}	5	P57	T2	Y6	527
I/O	5	-	-	AA4	530
I/O	5	-	-	AB4	536
I/O	5	-	P5	W6	539
I/O	5	P58	T3	Y7	542
GND	-	-	GND*	GND*	-

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P59	T4	AA5	545
I/O	5	P60	M6	AB5	548
I/O	5	-	-	V8	551
I/O	5	-	-	AA6	554
I/O	5	-	T5	AB6	557
GND	-	-	GND*	GND*	-
I/O	5	P61	N6	AA7	560
I/O	5	-	-	W7	563
I/O, V_{REF}	5	P62	R5	W8	569
I/O	5	P63	P6	Y8	572
GND	-	P64	GND*	GND*	-
V_{CCO}	5	P65	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCINT}	-	P66	V_{CCINT}*	V_{CCINT}*	-
I/O	5	P67	R6	AA8	575
I/O	5	P68	M7	V9	578
I/O	5	-	-	AB8	581
I/O	5	-	-	W9	584
I/O	5	-	-	AB9	587
GND	-	-	GND*	GND*	-
I/O	5	P69	N7	Y9	590
I/O	5	-	-	V10	593
I/O	5	-	-	AA9	596
I/O	5	P70	T6	W10	599
I/O	5	P71	P7	AB10	602
GND	-	P72	GND*	GND*	-
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P73	P8	Y10	605
I/O	5	P74	R7	V11	608
I/O	5	-	-	AA10	614
I/O	5	-	T7	W11	617
I/O	5	P75	T8	AB11	620
I/O	5	-	-	U11	623
V_{CCINT}	-	P76	V_{CCINT}*	V_{CCINT}*	-
I, GCK1	5	P77	R8	Y11	635
V_{CCO}	5	P78	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCO}	4	P78	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-