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AMD Xilinx - XC2S200-5FG256C Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	57344
Number of I/O	176
Number of Gates	200000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s200-5fg256c

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides capability for high-speed arithmetic functions. The Spartan-II FPGA CLB supports two separate carry chains, one per slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-II FPGA CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing," page 12. Each Spartan-II FPGA BUFT has an independent 3-state control pin and an independent input pin.

Block RAM

Spartan-II FPGAs incorporate several large block RAM memories. These complement the distributed RAM Look-Up Tables (LUTs) that provide shallow memory structures implemented in CLBs.

Block RAM memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks.

Table 5: Spartan-II Block RAM Amounts

Spartan-II Device	# of Blocks	Total Block RAM Bits
XC2S15	4	16K
XC2S30	6	24K
XC2S50	8	32K
XC2S100	10	40K
XC2S150	12	48K
XC2S200	14	56K

Each block RAM cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.



Figure 5: Dual-Port Block RAM

Table 6 shows the depth and width aspect ratios for the block RAM.

Table	6 [.]	Block	RAM	Port	Aspect	Ratios
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Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-II FPGA block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Bit 0 (TDO end) Bit 1 Bit 2	TDO.T TDO.O { Top-edge IOBs (Right to Left)
	Left-edge IOBs (Top to Bottom)
	MODE.I
	Bottom-edge IOBs (Left to Right)
▼ (TDI end)	Right-edge IOBs (Bottom to Top)

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Development System

Spartan-II FPGAs are supported by the Xilinx ISE[®] development tools. The basic methodology for Spartan-II FPGA design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation, while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under a single graphical interface, providing designers with a common user interface regardless of their choice of entry and verification tools. The software simplifies the selection of implementation options with pull-down menus and on-line help.

For HDL design entry, the Xilinx FPGA development system provides interfaces to several synthesis design environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-II FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The design environment supports hierarchical design entry. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, the development system includes a download cable, which connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can read back the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Signals

There are two kinds of pins that are used to configure Spartan-II devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the PROGRAM pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see "Pinout Tables" in Module 4 and XAPP176, Spartan-II FPGA Series Configuration and Readback.

The Process

The sequence of steps necessary to configure Spartan-II devices are shown in Figure 11. The overall flow can be divided into three different phases.

- Initiating Configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

Initiating Configuration

There are two different ways to initiate the configuration process: applying power to the device or asserting the PROGRAM input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Figure 12, page 19. Before configuration can begin, V_{CCO} Bank 2 must be greater than 1.0V. Furthermore, all V_{CCINT} power pins must be connected to a 2.5V supply. For more information on delaying configuration, see "Clearing Configuration Memory," page 19.

Once in user operation, the device can be re-configured simply by pulling the PROGRAM pin Low. The device acknowledges the beginning of the configuration process

by driving DONE Low, then enters the memory-clearing phase.



Figure 11: Configuration Flow Diagram



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Symbol		Description		Units
T _{DCC}		DIN setup	5	ns, min
T _{CCD}		DIN hold	0	ns, min
т _{ссо}		DOUT	12	ns, max
т _{ссн}	COLK	High time	5	ns, min
T _{CCL}		Low time	5	ns, min
F _{CC}		Maximum frequency	66	MHz, max

Figure 16: Slave Serial Mode Timing

division factor N except for non-integer division in High Frequency (HF) mode. For division factor 1.5 the duty cycle in the HF mode is 33.3% High and 66.7% Low. For division factor 2.5, the duty cycle in the HF mode is 40.0% High and 60.0% Low.

1x Clock Outputs — CLK[0/90/180/270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 degree phase-shifted version. The relationship between phase shift and the corresponding period shift appears in Table 10.

The timing diagrams in Figure 26 illustrate the DLL clock output characteristics.

Table 10: Relationship of Phase-Shifted Output Clock to Period Shift

Phase (degrees)	Period Shift (percent)
0	0%
90	25%
180	50%
270	75%

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL primitive. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

Locked Output — LOCKED

In order to achieve lock, the DLL may need to sample several thousand clock cycles. After the DLL achieves lock the LOCKED signal activates. The "DLL Timing Parameters" section of Module 3 provides estimates for locking times.

In order to guarantee that the system clock is established prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other

spurious movement. In particular the CLK2X output will appear as a 1x clock with a 25/75 duty cycle.

DLL Properties

Properties provide access to some of the Spartan-II family DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, such that they exhibit a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL primitive.



Figure 26: DLL Output Characteristics

Clock Divide Property

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Using Block RAM Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block RAM memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block RAM memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Block RAM memory supports two operating modes.

- Read Through
- Write Back

Read Through (One Clock Edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (One Clock Edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

Block RAM Characteristics

- 1. All inputs are registered with the port clock and have a setup to clock timing specification.
- 2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
- 3. The block RAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT cells in the CLBs are still available with this function.
- 4. The ports are completely independent from each other (*i.e.*, clocking, control, address, read/write function, and data width) without arbitration.
- 5. A write operation requires only one clock edge.
- 6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

Library Primitives

Figure 31 and Figure 32 show the two generic library block RAM primitives. Table 11 describes all of the available primitives for synthesis and simulation.



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Figure 32: Single-Port Block RAM Memory

Table 11: Available Library Primitives

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16

PCI — Peripheral Component Interface

The Peripheral Component Interface (PCI) standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a push-pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}). I/Os configured for the PCI, 33 MHz, 5V standard are also 5V-tolerant.

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic (GTL) standard is a high-speed bus standard (JESD8.3). Xilinx has implemented the terminated variation of this standard. This standard requires a differential amplifier input buffer and an open-drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus (GTL+) standard is a high-speed bus standard (JESD8.3).

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed, 1.5V bus standard (EIA/JESD 8-6). This standard has four variations or classes. Versatile I/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V (SSTL3) standard is a general purpose 3.3V memory bus standard (JESD8-8). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V (SSTL2) standard is a general purpose 2.5V memory bus standard (JESD8-9). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated (CTT) standard is a 3.3V memory bus standard (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with processors for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

Library Primitives

The Xilinx library includes an extensive list of primitives designed to provide support for the variety of Versatile I/O features. Most of these primitives represent variations of the five generic Versatile I/O primitives:

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

These primitives are available with various extensions to define the desired I/O standard. However, it is recommended that customers use a a property or attribute on the generic primitive to specify the I/O standard. See "Versatile I/O Properties".

IBUF

Signals used as inputs to the Spartan-II device must source an input buffer (IBUF) via an external input port. The generic IBUF primitive appears in Figure 35. The assumed standard is LVTTL when the generic IBUF has no specified extension or property.



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Figure 35: Input Buffer (IBUF) Primitive

When the IBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 16 summarizes the input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.



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Figure 36: I/O Banks

Table 16: Xilinx Input Standards CompatibilityRequirements

Rule 1	All differential amplifier input signals within a bank are required to be of the same standard.
Rule 2	There are no placement restrictions for inputs with standards that require a single-ended input buffer.

IBUFG

Signals used as high fanout clock inputs to the Spartan-II device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG primitive can only drive a CLKDLL, CLKDLLHF, or a BUFG primitive. The generic IBUFG primitive appears in Figure 37.



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Figure 37: Global Clock Input Buffer (IBUFG) Primitive

With no extension or property specified for the generic IBUFG primitive, the assumed standard is LVTTL.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP primitive represents a combination of the LVTTL IBUFG and BUFG primitives, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

The Spartan-II FPGA BUFGP primitive can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) primitive appears in Figure 38.



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Figure 38: Output Buffer (OBUF) Primitive

With no extension or property specified for the generic OBUF primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. property. This property could have one of the following seven values.

DRIVE=2 DRIVE=4 DRIVE=6 DRIVE=8 DRIVE=12 (Default) DRIVE=16 DRIVE=24

Design Considerations

Reference Voltage (V_{RFF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{RFF}). Provide the V_{RFF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{RFF} banks internally. See Figure 36, page 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{RFF} input.

Within each V_{REF} bank, any input buffers that require a V_{RFF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage (V_{CCO}) . As a result each device can often have to support multiple output drive source voltages.

The V_{CCO} supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined $V_{\mbox{\scriptsize CCO}}$ supply. The TQ144 and the CS144 packages provide four independent V_{CCO} supplies. The FG256 and the FG456 provide eight independent V_{CCO} supplies.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques:

None Series Parallel (Shunt) Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 41.





Unterminated Output Driving a Parallel Terminated Input





Series Terminated Output Driving

Series-Parallel Terminated Output

Series Terminated Output



Driving a Parallel Terminated Input VTT





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Figure 41: Overview of Standard Input and Output **Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

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СТТ

A sample circuit illustrating a valid termination technique for CTT appear in Figure 51. DC voltage specifications appear in Table 29 for the CTT standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics .



Figure 51: Terminated CTT

Table 29: CTT Voltage Specifications

Parameter	Min	Тур	Max
V _{CCO}	2.05 ⁽¹⁾	3.3	3.6
V _{REF}	1.35	1.5	1.65
V _{TT}	1.35	1.5	1.65
$V_{IH} \ge V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} \leq V_{REF} - 0.2$	-	1.3	1.45
$V_{OH} \ge V_{REF} + 0.4$	1.75	1.9	-
$V_{OL} \leq V_{REF} - 0.4$	-	1.1	1.25
I _{OH} at V _{OH} (mA)	-8	-	-
I _{OL} at V _{OL} (mA)	8	-	-

Notes:

1. Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 and PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 30 for the PCI33_3 and PCI66_3 standards. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 30: PCI33_3 and PCI66_3 Voltage Specifications

Parameter	Min	Тур	Max
V _{CCO}	3.0	3.3	3.6
V _{REF}	-	-	-
V _{TT}	-	-	-
$V_{IH} = 0.5 \times V_{CCO}$	1.5	1.65	V _{CCO} + 0.5
$V_{IL} = 0.3 \times V_{CCO}$	-0.5	0.99	1.08
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL} = 0.1 \times V_{CCO}$	-	-	0.36
I _{OH} at V _{OH} (mA)	Note 1	-	-
I _{OL} at V _{OL} (mA)	Note 1	-	-

Notes:

1. Tested according to the relevant specification.

PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in Table 31 for the PCI33_5 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

Table 31: PCI33_5 Voltage Specifications

Parameter	Min	Тур	Max
V _{CCO}	3.0	3.3	3.6
V _{REF}	-	-	-
V _{TT}	-	-	-
V _{IH}	1.425	1.5	5.5
V _{IL}	-0.5	1.0	1.05
V _{OH}	2.4	-	-
V _{OL}	-	-	0.55
I _{OH} at V _{OH} (mA)	Note 1	-	-
I _{OL} at V _{OL} (mA)	Note 1	-	-

Notes:

1. Tested according to the relevant specification.

Input/Output	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{ОН}
Standard	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
CTT	-0.5	V _{REF} – 0.2	V _{REF} + 0.2	3.6	V _{REF} – 0.4	V _{REF} + 0.4	8	-8
AGP	-0.5	V _{REF} – 0.2	V _{REF} + 0.2	3.6	10% V _{CCO}	90% V _{CCO}	Note (2)	Note (2)

Notes:

1. V_{OL} and V_{OH} for lower drive currents are sample tested.

2. Tested according to the relevant specifications.

Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, with DLL (Pin-to-Pin)⁽¹⁾

			S	peed Grad	le	
			All	-6	-5	
Symbol	Description	Device	Min	Max	Max	Units
T _{ICKOFDLL}	Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, <i>with</i> DLL.	All		2.9	3.3	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

- Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
- 3. DLL output jitter is already included in the timing calculation.
- 4. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)⁽¹⁾

				Speed Grade	9	
			All	-6	-5	
Symbol	Description	Device	Min	Max	Max	Units
T _{ICKOF}	Global clock input to output delay	XC2S15		4.5	5.4	ns
	using output flip-flop for LVTTL,	XC2S30		4.5	5.4	ns
	12 mA, fast slew rate, <i>without</i> DLL.	XC2S50		4.5	5.4	ns
		XC2S100		4.6	5.5	ns
		XC2S150		4.6	5.5	ns
		XC2S200		4.7	5.6	ns

Notes:

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

- Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
- For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.



Figure 52: Period Tolerance and Clock Jitter

Revision History

Date	Version No.	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Updated timing to reflect the latest speed files. Added current supply numbers and XC2S200 -5 timing numbers. Approved -5 timing numbers as preliminary information with exceptions as noted.
11/02/00	2.1	Removed Power Down feature.
01/19/01	2.2	DC and timing numbers updated to Preliminary for the XC2S50 and XC2S100. Industrial power-on current specifications and -6 DLL timing numbers added. Power-on specification clarified.
03/09/01	2.3	Added note on power sequencing. Clarified power-on current requirement.
08/28/01	2.4	Added -6 preliminary timing. Added typical and industrial standby current numbers. Specified min. power-on current by junction temperature instead of by device type (Commercial vs. Industrial). Eliminated minimum V_{CCINT} ramp time requirement. Removed footnote limiting DLL operation to the Commercial temperature range.
07/26/02	2.5	Clarified that I/O leakage current is specified over the Recommended Operating Conditions for V_{CCINT} and V_{CCO} .
08/26/02	2.6	Added references for XAPP450 to Power-On Current Specification.
09/03/03	2.7	Added relaxed minimum power-on current (I_{CCPO}) requirements to page 53. On page 64, moved T_{RPW} values from maximum to minimum column.
06/13/08	2.8	Updated I/O measurement thresholds. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.

Package Thermal Characteristics

Table 39 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB})

Table	39:	Spartan-II	Package	Thermal	Characteristics
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value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

				J	unction-to- at Differen	Ambient (θ _J , t Air Flows)	
Package	Device	Junction-to-Case (θ _{JC})	Junction-to- Board (θ _{JB})	Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	Units
VQ100	XC2S15	11.3	N/A	44.1	36.7	34.2	33.3	°C/Watt
VQG100	XC2S30	10.1	N/A	40.7	33.9	31.5	30.8	°C/Watt
	XC2S15	7.3	N/A	38.6	30.0	25.7	24.1	°C/Watt
TQ144	XC2S30	6.7	N/A	34.7	27.0	23.1	21.7	°C/Watt
TQG144	XC2S50	5.8	N/A	32.2	25.1	21.4	20.1	°C/Watt
	XC2S100	5.3	N/A	31.4	24.4	20.9	19.6	°C/Watt
CS144 CSG144	XC2S30	2.8	N/A	34.0	26.0	23.9	23.2	°C/Watt
	XC2S50	6.7	N/A	25.2	18.6	16.4	15.2	°C/Watt
PQ208	XC2S100	5.9	N/A	24.6	18.1	16.0	14.9	°C/Watt
PQG208	XC2S150	5.0	N/A	23.8	17.6	15.6	14.4	°C/Watt
	XC2S200	4.1	N/A	23.0	17.0	15.0	13.9	°C/Watt
	XC2S50	7.1	17.6	27.2	21.4	20.3	19.8	°C/Watt
FG256	XC2S100	5.8	15.1	25.1	19.5	18.3	17.8	°C/Watt
FGG256	XC2S150	4.6	12.7	23.0	17.6	16.3	15.8	°C/Watt
	XC2S200	3.5	10.7	21.4	16.1	14.7	14.2	°C/Watt
FG456	XC2S150	2.0	N/A	21.9	17.3	15.8	15.2	°C/Watt
FGG456	XC2S200	2.0	N/A	21.0	16.6	15.1	14.5	°C/Watt

Bndry

Scan

203

206

209

212

215

218

-

219

-

-

220

227

230

233

236

239

242

-

-

_

245

248

251

254

257

-

260

263

266

-

275

-

-

-

276

280

283

286

289

-

292

XC2S30 Device Pinouts

XC2S30 Pad	Name					Dodov] [XC2S30 Pad	Name				
Function	Bank	VQ100	TQ144	CS144	PQ208	Scan		Function	Bank	VQ100	TQ144	CS144	PQ208
GND	-	P1	P143	A1	P1	-		I/O, V _{REF}	6	P20	P115	K1	P45
TMS	-	P2	P142	B1	P2	-		I/O	6	-	-	-	P46
I/O	7	P3	P141	C2	P3	113	1	I/O	6	-	P114	K2	P47
I/O	7	-	P140	C1	P4	116	1	I/O	6	P21	P113	K3	P48
I/O	7	-	-	-	P5	119	1	I/O	6	P22	P112	L1	P49
I/O, V _{REF}	7	P4	P139	D4	P6	122		M1	-	P23	P111	L2	P50
I/O	7	-	P138	D3	P8	125		GND	-	P24	P110	L3	P51
I/O	7	P5	P137	D2	P9	128	1	MO	-	P25	P109	M1	P52
I/O	7	P6	P136	D1	P10	131	1	V _{CCO}	6	P26	P108	M2	P53
GND	-	-	P135	E4	P11	-	1	V _{CCO}	5	P26	P107	N1	P53
V _{cco}	7	-	-	-	P12	-	1	M2	-	P27	P106	N2	P54
I/O	7	P7	P134	E3	P14	134	1	I/O	5	-	P103	K4	P57
I/O	7	-	P133	E2	P15	137	1	I/O	5	-	-	-	P58
I/O	7	-	-	-	P16	140		I/O, V _{REF}	5	P30	P102	L4	P59
I/O	7	-	-	-	P17	143		I/O	5	-	P101	M4	P61
I/O	7	-	-	-	P18	146	1	I/O	5	P31	P100	N4	P62
GND	-	-	-	-	P19	-		I/O	5	P32	P99	K5	P63
I/O, V _{REF}	7	P8	P132	E1	P20	149	1	GND	-	-	P98	L5	P64
I/O	7	P9	P131	F4	P21	152		V _{CCO}	5	-	-	-	P65
I/O	7	-	P130	F3	P22	155	1	V _{CCINT}	-	P33	P97	M5	P66
I/O	7	-	-	-	P23	158	1	I/O	5	-	P96	N5	P67
I/O, IRDY ⁽¹⁾	7	P10	P129	F2	P24	161	1	I/O	5	-	P95	K6	P68
GND	-	P11	P128	F1	P25	-		I/O	5	-	-	-	P69
V _{CCO}	7	P12	P127	G2	P26	-	1	I/O	5	-	-	-	P70
V _{cco}	6	P12	P127	G2	P26	-		I/O	5	-	-	-	P71
I/O, TRDY ⁽¹⁾	6	P13	P126	G1	P27	164	1	GND	-	-	-	-	P72
V _{CCINT}	-	P14	P125	G3	P28	-	1	I/O, V _{REF}	5	P34	P94	L6	P73
I/O	6	-	P124	G4	P29	170	1	I/O	5	-	-	-	P74
I/O	6	P15	P123	H1	P30	173	1	I/O	5	-	P93	M6	P75
I/O, V _{REF}	6	P16	P122	H2	P31	176		V _{CCINT}	-	P35	P92	N6	P76
GND	-	-	-	-	P32	-		I, GCK1	5	P36	P91	M7	P77
I/O	6	-	-	-	P33	179	1	V _{CCO}	5	P37	P90	N7	P78
I/O	6	-	-	-	P34	182		V _{CCO}	4	P37	P90	N7	P78
I/O	6	-	-	-	P35	185	1	GND	-	P38	P89	L7	P79
I/O	6	-	P121	H3	P36	188	1	I, GCK0	4	P39	P88	K7	P80
I/O	6	P17	P120	H4	P37	191		I/O	4	P40	P87	N8	P81
V _{CCO}	6	-	-	-	P39	-	1 [I/O	4	-	P86	M8	P82
GND	-	-	P119	J1	P40	-	1 [I/O	4	-	-	-	P83
I/O	6	P18	P118	J2	P41	194	1 [I/O, V _{REF}	4	P41	P85	L8	P84
I/O	6	P19	P117	J3	P42	197	1 [GND	-	-	-	-	P85
I/O	6	-	P116	J4	P43	200] [I/O	4	-	-	-	P86

XC2S50 Device Pinouts

XC2S50 Pad N	Name				Bndry
Function Bank		TQ144	PQ208	FG256	Scan
GND	-	P143	P1	GND*	-
TMS	-	P142	P2	D3	-
I/O	7	P141	P3	C2	149
I/O	7	-	-	A2	152
I/O	7	P140	P4	B1	155
I/O	7	-	-	E3	158
I/O	7	-	P5	D2	161
GND	-	-	-	GND*	-
I/O, V _{REF}	7	P139	P6	C1	164
I/O	7	-	P7	F3	167
I/O	7	-	-	E2	170
I/O	7	P138	P8	E4	173
I/O	7	P137	P9	D1	176
I/O	7	P136	P10	E1	179
GND	-	P135	P11	GND*	-
V _{CCO}	7	-	P12	V _{CCO} Bank 7*	-
V _{CCINT}	-	-	P13	V _{CCINT} *	-
I/O	7	P134	P14	F2	182
I/O	7	P133	P15	G3	185
I/O	7	-	-	F1	188
I/O	7	-	P16	F4	191
I/O	7	-	P17	F5	194
I/O	7	-	P18	G2	197
GND	-	-	P19	GND*	-
I/O, V _{REF}	7	P132	P20	H3	200
I/O	7	P131	P21	G4	203
I/O	7	-	-	H2	206
I/O	7	P130	P22	G5	209
I/O	7	-	P23	H4	212
I/O, IRDY ⁽¹⁾	7	P129	P24	G1	215
GND	-	P128	P25	GND*	-
V _{CCO}	7	P127	P26	V _{CCO} Bank 7*	-
V _{CCO}	6	P127	P26	V _{CCO} Bank 6*	-
I/O, TRDY ⁽¹⁾	6	P126	P27	J2	218
V _{CCINT}	-	P125	P28	V_{CCINT}^{*}	-
I/O	6	P124	P29	H1	224
I/O	6	-	-	J4	227
I/O	6	P123	P30	J1	230
I/O, V _{REF}	6	P122	P31	J3	233

XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name					Bndry
Function	Bank	TQ144	PQ208	FG256	Scan
GND	-	-	P32	GND*	-
I/O	6	-	P33	K5	236
I/O	6	-	P34	K2	239
I/O	6	-	P35	K1	242
I/O	6	-	-	K3	245
I/O	6	P121	P36	L1	248
I/O	6	P120	P37	L2	251
V _{CCINT}	-	-	P38	V _{CCINT} *	-
V _{CCO}	6	-	P39	V _{CCO} Bank 6*	-
GND	-	P119	P40	GND*	-
I/O	6	P118	P41	K4	254
I/O	6	P117	P42	M1	257
I/O	6	P116	P43	L4	260
I/O	6	-	-	M2	263
I/O	6	-	P44	L3	266
I/O, V _{REF}	6	P115	P45	N1	269
GND	-	-	-	GND*	-
I/O	6	-	P46	P1	272
I/O	6	-	-	L5	275
I/O	6	P114	P47	N2	278
I/O	6	-	-	M4	281
I/O	6	P113	P48	R1	284
I/O	6	P112	P49	М3	287
M1	-	P111	P50	P2	290
GND	-	P110	P51	GND*	-
MO	-	P109	P52	N3	291
V _{CCO}	6	P108	P53	V _{CCO} Bank 6*	-
V _{CCO}	5	P107	P53	V _{CCO} Bank 5*	-
M2	-	P106	P54	R3	292
I/O	5	-	-	N5	299
I/O	5	P103	P57	T2	302
I/O	5	-	-	P5	305
I/O	5	-	P58	Т3	308
GND	-	-	-	GND*	-
I/O, V _{REF}	5	P102	P59	T4	311
I/O	5	-	P60	M6	314
I/O	5	-	-	T5	317
I/O	5	P101	P61	N6	320
I/O	5	P100	P62	R5	323

XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name					Bndry
Function	Bank	TQ144	PQ208	FG256	Scan
I/O	0	-	-	D8	83
I/O	0	-	P188	A6	86
I/O, V _{REF}	0	P12	P189	B7	89
GND	-	-	P190	GND*	-
I/O	0	-	P191	C8	92
I/O	0	-	P192	D7	95
I/O	0	-	P193	E7	98
I/O	0	P11	P194	C7	104
I/O	0	P10	P195	B6	107
V _{CCINT}	-	P9	P196	V _{CCINT} *	-
V _{CCO}	0	-	P197	V _{CCO} Bank 0*	-
GND	-	P8	P198	GND*	-
I/O	0	P7	P199	A5	110
I/O	0	P6	P200	C6	113
I/O	0	-	P201	B5	116
I/O	0	-	-	D6	119
I/O	0	-	P202	A4	122
I/O, V _{REF}	0	P5	P203	B4	125
GND	-	-	-	GND*	-
I/O	0	-	P204	E6	128
I/O	0	-	-	D5	131
I/O	0	P4	P205	A3	134
I/O	0	-	-	C5	137
I/O	0	P3	P206	B3	140
TCK	-	P2	P207	C4	-
V _{CCO}	0	P1	P208	V _{CCO} Bank 0*	-
V _{CCO}	7	P144	P208	V _{CCO} Bank 7*	-

04/18/01

Notes:

- 1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
- Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
- 3. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S50 Package Pins

TQ1	44
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Not Connected Pins							
P104	P105	-	-	-	-		
11/02/00							

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						Bndry
Function	Bank	TQ144	PQ208	FG256	FG456	Scan
I/O	0	-	P188	A6	C10	107
I/O, V _{REF}	0	P12	P189	B7	A9	110
GND	-	-	P190	GND*	GND*	-
I/O	0	-	P191	C8	B9	113
I/O	0	-	P192	D7	E10	116
I/O	0	-	P193	E7	A8	122
I/O	0	-	-	-	D9	125
I/O	0	P11	P194	C7	E9	128
I/O	0	P10	P195	B6	A7	131
V _{CCINT}	-	P9	P196	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	0	-	P197	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	P8	P198	GND*	GND*	-
I/O	0	P7	P199	A5	B7	134
I/O, V _{REF}	0	P6	P200	C6	E8	137
I/O	0	-	-	-	D8	140
I/O	0	-	P201	B5	C7	143
I/O	0	-	-	D6	D7	146
I/O	0	-	P202	A4	D6	152
I/O, V _{REF}	0	P5	P203	B4	C6	155
V _{CCO}	0	-	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	-	-	GND*	GND*	-
I/O	0	-	P204	E6	B5	158
I/O	0	-	-	D5	E7	161
I/O	0	-	-	-	E6	164
I/O	0	P4	P205	A3	B4	167
I/O	0	-	-	C5	A3	170
I/O	0	P3	P206	B3	C5	176
ТСК	-	P2	P207	C4	C4	-
V _{CCO}	0	P1	P208	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
V _{CCO}	7	P144	P208	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-

^{04/18/01}

Notes:

- 1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
- Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
- 3. See "VCCO Banks" for details on V_{CCO} banking.

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O	4	P90	R11	AA15	595
V _{CCINT}	-	P91	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	4	P92	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	P93	GND*	GND*	-
I/O	4	P94	M11	Y15	598
I/O, V _{REF}	4	P95	T11	AB16	601
I/O	4	-	-	AB17	604
I/O	4	P96	N11	V15	607
I/O	4	-	R12	Y16	610
I/O	4	-	-	AA17	613
I/O	4	-	-	W16	616
I/O	4	P97	P11	AB18	619
I/O, V _{REF}	4	P98	T12	AB19	622
V _{CCO}	4	-	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
GND	-	-	GND*	GND*	-
I/O	4	P99	T13	Y17	625
I/O	4	-	N12	V16	628
I/O	4	-	-	AA18	631
I/O	4	-	-	W17	634
I/O	4	P100	R13	AB20	637
GND	-	-	GND*	GND*	-
I/O	4	-	P12	AA19	640
I/O	4	-	-	V17	643
I/O	4	-	-	Y18	646
I/O	4	P101	P13	AA20	649
I/O	4	P102	T14	W18	652
GND	-	P103	GND*	GND*	-
DONE	3	P104	R14	Y19	655
V _{CCO}	4	P105	V _{CCO} Bank 4*	V _{CCO} Bank 4*	-
V _{CCO}	3	P105	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
PROGRAM	-	P106	P15	W20	658
I/O (INIT)	3	P107	N15	V19	659
I/O (D7)	3	P108	N14	Y21	662
I/O	3	-	-	V20	665
I/O	3	-	-	AA22	668
I/O	3	-	T15	W21	671
GND	-	-	GND*	GND*	-
I/O	3	P109	M13	U20	674

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O	3	-	-	U19	677
I/O	3	-	-	V21	680
I/O	3	-	R16	T18	683
I/O	3	P110	M14	W22	686
GND	-	-	GND*	GND*	-
V _{CCO}	3	-	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
I/O, V _{REF}	3	P111	L14	U21	689
I/O	3	P112	M15	T20	692
I/O	3	-	-	T19	695
I/O	3	-	-	V22	698
I/O	3	-	L12	T21	701
I/O	3	P113	P16	R18	704
I/O	3	-	-	U22	707
I/O, V _{REF}	3	P114	L13	R19	710
I/O (D6)	3	P115	N16	T22	713
GND	-	P116	GND*	GND*	-
V _{CCO}	3	P117	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{CCINT}	-	P118	V _{CCINT} *	V _{CCINT} *	-
I/O (D5)	3	P119	M16	R21	716
I/O	3	P120	K14	P18	719
I/O	3	-	-	P19	725
I/O	3	-	L16	P20	728
I/O	3	P121	K13	P21	731
I/O	3	-	-	N19	734
I/O	3	P122	L15	N18	740
I/O	3	P123	K12	N20	743
GND	-	P124	GND*	GND*	-
V _{CCO}	3	-	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
I/O, V _{REF}	3	P125	K16	N21	746
I/O (D4)	3	P126	J16	N22	749
I/O	3	-	J14	M19	752
I/O	3	P127	K15	M20	755
I/O	3	-	-	M18	758
V _{CCINT}	-	P128	V _{CCINT} *	V _{CCINT} *	-
I/O, TRDY ⁽¹⁾	3	P129	J15	M22	764
V _{CCO}	3	P130	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{cco}	2	P130	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P131	GND*	GND*	-

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
GND	-	P198	GND*	GND*	-
I/O	0	P199	A5	B7	188
I/O, V _{REF}	0	P200	C6	E8	191
I/O	0	-	-	D8	197
I/O	0	P201	B5	C7	200
GND	-	-	GND*	GND*	-
I/O	0	-	D6	D7	203
I/O	0	-	-	B6	206
I/O	0	-	-	A5	209
I/O	0	P202	A4	D6	212
I/O, V _{REF}	0	P203	B4	C6	215
V _{CCO}	0	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	-	GND*	GND*	-
I/O	0	P204	E6	B5	218
I/O	0	-	D5	E7	221
I/O	0	-	-	A4	224
I/O	0	-	-	E6	230
I/O, V _{REF}	0	P205	A3	B4	233
GND	-	-	GND*	GND*	-
I/O	0	-	C5	A3	236
I/O	0	-	-	B3	239
I/O	0	-	-	D5	242
I/O	0	P206	B3	C5	248
тск	-	P207	C4	C4	-
V _{CCO}	0	P208	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
V _{CCO}	7	P208	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-

04/18/01

- 1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
- Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
- 3. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S200 Package Pins

PQ208

Not Connected Pins							
P55	P56	-	-	-	-		
11/02/00		•					

FG256

V _{CCINT} Pins								
C3	C14	D4	D13	E5	E12			
M5	M12	N4	N13	P3	P14			
V _{CCO} Bank 0 Pins								
E8	F8	-	-	-	-			
	V _{CCO} Bank 1 Pins							
E9	F9	-	-	-	-			
		V _{CCO} Ba	nk 2 Pins					
H11	H12	-	-	-	-			
		V _{CCO} Ba	nk 3 Pins					
J11	J12	-	-	-	-			
		V _{CCO} Ba	nk 4 Pins					
L9	M9	-	-	-	-			
	V _{CCO} Bank 5 Pins							
L8	L8 M8							
		V _{CCO} Ba	nk 6 Pins					
J5	J6	-	-	-	-			
		V _{CCO} Ba	nk 7 Pins					
H5	H6	-	-	-	-			
		GND	Pins					
A1	A16	B2	B15	F6	F7			
F10	F11	G6	G7	G8	G9			
G10	G11	H7	H8	H9	H10			
J7	J8	J9	J10	K6	K7			
K8	K9	K10	K11	L6	L7			
L10	L11	R2	R15	T1	T16			
Not Connected Pins								
P4	R4	-	-	-	-			