AMD Xilinx - XC2S200-5FGG256I Datasheet





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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	57344
Number of I/O	176
Number of Gates	200000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s200-5fgg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Ordering Information

Spartan-II devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

Standard Packaging



Device Ordering Options

Device		Speed Grade	Speed Grade N		per of Pins / Package Type	Temperatur	e Range (T _J)
XC2S15	-5	Standard Performance	`	VQ(G)100	100-pin Plastic Very Thin QFP	C = Commercial	0°C to +85°C
XC2S30	-6	Higher Performance ⁽¹⁾	(CS(G)144	144-ball Chip-Scale BGA	I = Industrial	-40°C to +100°C
XC2S50			-	TQ(G)144	144-pin Plastic Thin QFP		
XC2S100			F	PQ(G)208	208-pin Plastic QFP		
XC2S150			F	FG(G)256	256-ball Fine Pitch BGA		
XC2S200			F	FG(G)456	456-ball Fine Pitch BGA		

Notes:

1. The -6 speed grade is exclusively available in the Commercial temperature range.

Device Part Marking



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By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The default timing for start-up is shown in the top half of Figure 13. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in the Xilinx software. Heavy lines show default settings.



Figure 13: Start-Up Waveforms

The bottom half of Figure 13 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

Serial Modes

There are two serial configuration modes: In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the DIN pin first.

See Figure 14 for the sequence for loading data into the Spartan-II FPGA serially. This is an expansion of the "Load Configuration Data Frames" block in Figure 11. Note that CS and WRITE normally are not used during serial configuration. To ensure successful loading of the FPGA, do not toggle WRITE with CS Low during serial configuration.





Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK. Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is 2²⁰-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until INIT pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.



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Notes:

1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 15: Master/Slave Serial Configuration Circuit Diagram



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Symbol		Description		Units
T _{DCC}		DIN setup	5	ns, min
T _{CCD}		DIN hold	0	ns, min
т _{ссо}		DOUT	12	ns, max
т _{ссн}	COLK	High time	5	ns, min
T _{CCL}		Low time	5	ns, min
F _{CC}		Maximum frequency	66	MHz, max

Figure 16: Slave Serial Mode Timing



Figure 18: Slave Parallel Configuration Circuit Diagram

Multiple Spartan-II FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See "Start-up," page 19.

Write

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 19, page 25 shows a flowchart of the write sequence used to load data into the Spartan-II FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 11, page 18. The timing for write operations is shown in Figure 20, page 26. For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise an abort will be initiated, as in the next section.

- 1. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while \overline{CS} is Low and \overline{WRITE} is High. Similarly, while \overline{WRITE} is High, no more than one device's \overline{CS} should be asserted.
- 2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
- 3. Repeat steps 1 and 2 until all the data has been sent.
- 4. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the Startup Sequence following device configuration is paused at a user-specified point until the DLL locks. <u>XAPP176</u>: *Configuration and Readback of the Spartan-II and Spartan-IIE Families* explains how this can result in delaying the assertion of the DONE pin until the DLL locks.

DLL Location Constraints

The DLLs are distributed such that there is one DLL in each corner of the device. The location constraint LOC, attached to the DLL primitive with the numeric identifier 0, 1, 2, or 3, controls DLL location. The orientation of the four DLLs and their corresponding clock resources appears in Figure 27.

The LOC property uses the following form.

LOC = DLL2



Figure 27: Orientation of DLLs

Design Considerations

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the "DLL Timing Parameters" section of the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock in a way that has little impact to the DLL. Stopping the clock should be limited to less than approximately 100 μ s to keep device cooling to a minimum and maintain the validity of the current tap setting. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED will stay High and remain High when the clock is restored. If these conditions may not be met in the design, apply a manual reset to the DLL after re-starting the input clock, even if the LOCKED signal has not changed.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). One DLL output can drive more than one OBUF; however, this adds skew.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Useful Application Examples

The Spartan-II FPGA DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications.

Standard Usage

The circuit shown in Figure 28 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.



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Figure 28: Standard DLL Implementation

Deskew of Clock and Its 2x Multiple

The circuit shown in Figure 29 implements a 2x clock multiplier and also uses the CLK0 clock output with zero ns skew between registers on the same chip. A clock divider circuit could alternatively be implemented using similar connections.



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Figure 29: DLL Deskew of Clock and 2x Multiple

Because any single DLL can only access at most two BUFGs, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

Generating a 4x Clock

By connecting two DLL circuits each implementing a 2x clock multiplier in series as shown in Figure 30, a 4x clock multiply can be implemented with zero skew between registers in the same device.

If other clock output is needed, the clock could access a BUFG only if the DLLs are constrained to exist on opposite edges (Top or Bottom) of the device.



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Figure 30: DLL Generation of 4x Clock

When using this circuit it is vital to use the SRL16 cell to reset the second DLL after the initial chip reset. If this is not done, the second DLL may not recognize the change of frequencies from when the input changes from a 1x (25/75) waveform to a 2x (50/50) waveform. It is not recommended to cascade more than two DLLs.

For design examples and more information on using the DLL, see <u>XAPP174</u>, Using Delay-Locked Loops in Spartan-II FPGAs.

support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features, system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 15, each buffer type can support a variety of voltage requirements.

Table 15: Versatile I/O Supported Standards (Typical Values)

I/O Standard	Input Reference Voltage (V _{REF})	Output Source Voltage (V _{CCO})	Board Termination Voltage (V _{TT})
LVTTL (2-24 mA)	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI (3V/5V, 33 MHz/66 MHz)	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	0.75
HSTL Class III	0.9	1.5	1.5
HSTL Class IV	0.9	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
СТТ	1.5	3.3	1.5
AGP-2X	1.32	3.3	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance JEDEC website at http://www.jedec.org. For more details on the I/O standards and termination application examples, see XAPP179, "Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs."

LVTTL — Low-Voltage TTL

The Low-Voltage TTL (LVTTL) standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5V

The Low-Voltage CMOS for 2.5V or lower (LVCMOS2) standard is an extension of the LVCMOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

property. This property could have one of the following seven values.

DRIVE=2 DRIVE=4 DRIVE=6 DRIVE=8 DRIVE=12 (Default) DRIVE=16 DRIVE=24

Design Considerations

Reference Voltage (V_{RFF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{RFF}). Provide the V_{RFF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{RFF} banks internally. See Figure 36, page 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{RFF} input.

Within each V_{REF} bank, any input buffers that require a V_{RFF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage (V_{CCO}) . As a result each device can often have to support multiple output drive source voltages.

The V_{CCO} supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined $V_{\mbox{\scriptsize CCO}}$ supply. The TQ144 and the CS144 packages provide four independent V_{CCO} supplies. The FG256 and the FG456 provide eight independent V_{CCO} supplies.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques:

None Series Parallel (Shunt) Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 41.





Unterminated Output Driving a Parallel Terminated Input





Series Terminated Output Driving

Series-Parallel Terminated Output

Series Terminated Output



Driving a Parallel Terminated Input VTT





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Figure 41: Overview of Standard Input and Output **Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 45. DC voltage specifications appear in Table 23 for the HSTL_III standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

HSTL Class III



Figure 45: Terminated HSTL Class III

Table	23:	HSTL	Class	III	Voltage	Specification	n
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Parameter	Min	Тур	Мах
V _{CCO}	1.40	1.50	1.60
V _{REF} ⁽¹⁾	-	0.90	-
V _{TT}	-	V _{CCO}	-
V _{IH}	V _{REF} + 0.1	-	-
V _{IL}	-	-	$V_{REF} - 0.1$
V _{OH}	$V_{CCO} - 0.4$	-	-
V _{OL}	-	-	0.4
I _{OH} at V _{OH} (mA)	-8	-	-
I _{OL} at V _{OL} (mA)	24	-	-

Notes:

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class IV

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 46.DC voltage specifications appear in Table 23 for the HSTL_IV standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics



Figure 46: Terminated HSTL Class IV

Table 24: HSTL Class IV Voltage Specification

Parameter	Min	Тур	Max
V _{CCO}	1.40	1.50	1.60
V _{REF}	-	0.90	-
V _{TT}	-	V _{CCO}	-
V _{IH}	V _{REF} + 0.1	-	-
V _{IL}	-	-	V _{REF} – 0.1
V _{OH}	$V_{CCO} - 0.4$	-	-
V _{OL}	-	-	0.4
I _{OH} at V _{OH} (mA)	-8	-	-
I _{OL} at V _{OL} (mA)	48	-	-

Notes:

 Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

Global Clock Setup and Hold for LVTTL Standard, with DLL (Pin-to-Pin)

			Speed	Grade	
			-6	-5	
Symbol	Description	Device	Min	Min	Units
T _{PSDLL} / T _{PHDLL}	Input setup and hold time relative to global clock input signal for LVTTL standard, no delay, IFF, ⁽¹⁾ with DLL	All	1.7 / 0	1.9/0	ns

Notes:

1. IFF = Input Flip-Flop or Latch

2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

3. DLL output jitter is already included in the timing calculation.

4. A zero hold time listing indicates no hold time or a negative hold time.

 For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Delay Adjustments for Different Standards," page 57. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

Global Clock Setup and Hold for LVTTL Standard, without DLL (Pin-to-Pin)

			Speed		
			-6	-5	
Symbol	Description	Device	Min	Min	Units
T _{PSFD} / T _{PHFD}	Input setup and hold time relative to global clock input signal for LVTTL standard, no delay, IFF, ⁽¹⁾ without DLL	XC2S15	2.2 / 0	2.7 / 0	ns
		XC2S30	2.2 / 0	2.7 / 0	ns
		XC2S50	2.2 / 0	2.7 / 0	ns
		XC2S100	2.3 / 0	2.8 / 0	ns
		XC2S150	2.4 / 0	2.9/0	ns
		XC2S200	2.4 / 0	3.0 / 0	ns

Notes:

1. IFF = Input Flip-Flop or Latch

2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

3. A zero hold time listing indicates no hold time or a negative hold time.

4. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Delay Adjustments for Different Standards," page 57. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

IOB Output Delay Adjustments for Different Standards⁽¹⁾

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

			Speed Grade					
Symbol	Description	Standard	-6	-5	Units			
Output Delay Adjustments (Adj)								
T _{OLVTTL_S2}	Standard-specific adjustments for	LVTTL, Slow, 2 mA	14.2	16.9	ns			
T _{OLVTTL_S4}	output delays terminating at pads	4 mA	7.2	8.6	ns			
T _{OLVTTL_S6}	load, C _{SI})	6 mA	4.7	5.5	ns			
T _{OLVTTL_S8}		8 mA	2.9	3.5	ns			
T _{OLVTTL_S12}		12 mA	1.9	2.2	ns			
T _{OLVTTL_S16}		16 mA	1.7	2.0	ns			
T _{OLVTTL_S24}		24 mA	1.3	1.5	ns			
T _{OLVTTL_F2}		LVTTL, Fast, 2 mA	12.6	15.0	ns			
T _{OLVTTL_F4}		4 mA	5.1	6.1	ns			
T _{OLVTTL_F6}		6 mA	3.0	3.6	ns			
T _{OLVTTL_F8}	-	8 mA	1.0	1.2	ns			
T _{OLVTTL_F12}		12 mA	0	0	ns			
T _{OLVTTL_F16}		16 mA	-0.1	-0.1	ns			
T _{OLVTTL_F24}		24 mA	-0.1	-0.2	ns			
T _{OLVCMOS2}		LVCMOS2	0.2	0.2	ns			
T _{OPCI33_3}		PCI, 33 MHz, 3.3V	2.4	2.9	ns			
T _{OPCI33_5}		PCI, 33 MHz, 5.0V	2.9	3.5	ns			
T _{OPCI66_3}		PCI, 66 MHz, 3.3V	-0.3	-0.4	ns			
T _{OGTL}		GTL	0.6	0.7	ns			
T _{OGTLP}		GTL+	0.9	1.1	ns			
T _{OHSTL_I}		HSTL I	-0.4	-0.5	ns			
T _{OHSTL_III}		HSTL III	-0.8	-1.0	ns			
T _{OHSTL_IV}		HSTL IV	-0.9	-1.1	ns			
T _{OSSTL2_I}		SSTL2 I	-0.4	-0.5	ns			
T _{OSSLT2_II}		SSTL2 II	-0.8	-1.0	ns			
T _{OSSTL3_I}		SSTL3 I	-0.4	-0.5	ns			
T _{OSSTL3_II}		SSTL3 II	-0.9	-1.1	ns			
T _{OCTT}		СТТ	-0.5	-0.6	ns			
T _{OAGP}		AGP	-0.8	-1.0	ns			

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.



Figure 52: Period Tolerance and Clock Jitter

XC2S30 Device Pinouts (Continued)

XC2S30 Pad Name						Bndry
Function	Bank	VQ100	TQ144	CS144	PQ208	Scan
I/O	4	-	-	-	P87	295
I/O	4	-	-	-	P88	298
I/O	4	-	P84	K8	P89	301
I/O	4	-	P83	N9	P90	304
V _{CCINT}	-	P42	P82	M9	P91	-
V _{CCO}	4	-	-	-	P92	-
GND	-	-	P81	L9	P93	-
I/O	4	P43	P80	K9	P94	307
I/O	4	P44	P79	N10	P95	310
I/O	4	-	P78	M10	P96	313
I/O, V _{REF}	4	P45	P77	L10	P98	316
I/O	4	-	-	-	P99	319
I/O	4	-	P76	N11	P100	322
I/O	4	P46	P75	M11	P101	325
I/O	4	P47	P74	L11	P102	328
GND	-	P48	P73	N12	P103	-
DONE	3	P49	P72	M12	P104	331
V _{CCO}	4	P50	P71	N13	P105	-
V _{CCO}	3	P50	P70	M13	P105	-
PROGRAM	-	P51	P69	L12	P106	334
I/O (INIT)	3	P52	P68	L13	P107	335
I/O (D7)	3	P53	P67	K10	P108	338
I/O	3	-	P66	K11	P109	341
I/O	3	-	-	-	P110	344
I/O, V _{REF}	3	P54	P65	K12	P111	347
I/O	3	-	P64	K13	P113	350
I/O	3	P55	P63	J10	P114	353
I/O (D6)	3	P56	P62	J11	P115	356
GND	-	-	P61	J12	P116	-
V _{CCO}	3	-	-	-	P117	-
I/O (D5)	3	P57	P60	J13	P119	359
I/O	3	P58	P59	H10	P120	362
I/O	3	-	-	-	P121	365
I/O	3	-	-	-	P122	368
I/O	3	-	-	-	P123	371
GND	-	-	-	-	P124	-
I/O, V _{REF}	3	P59	P58	H11	P125	374
I/O (D4)	3	P60	P57	H12	P126	377
I/O	3	-	P56	H13	P127	380
V _{CCINT}	-	P61	P55	G12	P128	-
I/O, TRDY ⁽¹⁾	3	P62	P54	G13	P129	386
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XC2S30 Device Pinouts (Continued)

XC2S30 Pad Name						Bndry
Function	Bank	VQ100	TQ144	CS144	PQ208	Scan
V _{CCO}	3	P63	P53	G11	P130	-
V _{CCO}	2	P63	P53	G11	P130	-
GND	-	P64	P52	G10	P131	-
I/O, IRDY ⁽¹⁾	2	P65	P51	F13	P132	389
I/O	2	-	-	-	P133	392
I/O	2	-	P50	F12	P134	395
I/O (D3)	2	P66	P49	F11	P135	398
I/O, V _{REF}	2	P67	P48	F10	P136	401
GND	-	-	-	-	P137	-
I/O	2	-	-	-	P138	404
I/O	2	-	-	-	P139	407
I/O	2	-	-	-	P140	410
I/O	2	P68	P47	E13	P141	413
I/O (D2)	2	P69	P46	E12	P142	416
V _{CCO}	2	-	-	-	P144	-
GND	-	-	P45	E11	P145	-
I/O (D1)	2	P70	P44	E10	P146	419
I/O	2	P71	P43	D13	P147	422
I/O	2	-	P42	D12	P148	425
I/O, V _{REF}	2	P72	P41	D11	P150	428
I/O	2	-	-	-	P151	431
I/O	2	-	P40	C13	P152	434
I/O (DIN, D0)	2	P73	P39	C12	P153	437
I/O (DOUT, BUSY)	2	P74	P38	C11	P154	440
CCLK	2	P75	P37	B13	P155	443
V _{CCO}	2	P76	P36	B12	P156	-
V _{CCO}	1	P76	P35	A13	P156	-
TDO	2	P77	P34	A12	P157	-
GND	-	P78	P33	B11	P158	-
TDI	-	P79	P32	A11	P159	-
I/O (CS)	1	P80	P31	D10	P160	0
I/O (WRITE)	1	P81	P30	C10	P161	3
I/O	1	-	P29	B10	P162	6
I/O	1	-	-	-	P163	9
I/O, V _{REF}	1	P82	P28	A10	P164	12
I/O	1	-	-	-	P166	15
I/O	1	P83	P27	D9	P167	18
I/O	1	P84	P26	C9	P168	21
GND	-	-	P25	B9	P169	-
V _{CCO}	1	-	-	-	P170	-

XC2S50 Device Pinouts

XC2S50 Pad N				Bndry	
Function	Function Bank		PQ208	FG256	Scan
GND	-	P143	P1	GND*	-
TMS	-	P142	P2	D3	-
I/O	7	P141	P3	C2	149
I/O	7	-	-	A2	152
I/O	7	P140	P4	B1	155
I/O	7	-	-	E3	158
I/O	7	-	P5	D2	161
GND	-	-	-	GND*	-
I/O, V _{REF}	7	P139	P6	C1	164
I/O	7	-	P7	F3	167
I/O	7	-	-	E2	170
I/O	7	P138	P8	E4	173
I/O	7	P137	P9	D1	176
I/O	7	P136	P10	E1	179
GND	-	P135	P11	GND*	-
V _{CCO}	7	-	P12	V _{CCO} Bank 7*	-
V _{CCINT}	-	-	P13	V _{CCINT} *	-
I/O	7	P134	P14	F2	182
I/O	7	P133	P15	G3	185
I/O	7	-	-	F1	188
I/O	7	-	P16	F4	191
I/O	7	-	P17	F5	194
I/O	7	-	P18	G2	197
GND	-	-	P19	GND*	-
I/O, V _{REF}	7	P132	P20	H3	200
I/O	7	P131	P21	G4	203
I/O	7	-	-	H2	206
I/O	7	P130	P22	G5	209
I/O	7	-	P23	H4	212
I/O, IRDY ⁽¹⁾	7	P129	P24	G1	215
GND	-	P128	P25	GND*	-
V _{CCO}	7	P127	P26	V _{CCO} Bank 7*	-
V _{CCO}	6	P127	P26	V _{CCO} Bank 6*	-
I/O, TRDY ⁽¹⁾	6	P126	P27	J2	218
V _{CCINT}	-	P125	P28	V_{CCINT}^{*}	-
I/O	6	P124	P29	H1	224
I/O	6	-	-	J4	227
I/O	6	P123	P30	J1	230
I/O, V _{REF}	6	P122	P31	J3	233

XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name					Bndry
Function	Bank	TQ144	PQ208	FG256	Scan
GND	-	-	P32	GND*	-
I/O	6	-	P33	K5	236
I/O	6	-	P34	K2	239
I/O	6	-	P35	K1	242
I/O	6	-	-	K3	245
I/O	6	P121	P36	L1	248
I/O	6	P120	P37	L2	251
V _{CCINT}	-	-	P38	V _{CCINT} *	-
V _{CCO}	6	-	P39	V _{CCO} Bank 6*	-
GND	-	P119	P40	GND*	-
I/O	6	P118	P41	K4	254
I/O	6	P117	P42	M1	257
I/O	6	P116	P43	L4	260
I/O	6	-	-	M2	263
I/O	6	-	P44	L3	266
I/O, V _{REF}	6	P115	P45	N1	269
GND	-	-	-	GND*	-
I/O	6	-	P46	P1	272
I/O	6	-	-	L5	275
I/O	6	P114	P47	N2	278
I/O	6	-	-	M4	281
I/O	6	P113	P48	R1	284
I/O	6	P112	P49	М3	287
M1	-	P111	P50	P2	290
GND	-	P110	P51	GND*	-
MO	-	P109	P52	N3	291
V _{CCO}	6	P108	P53	V _{CCO} Bank 6*	-
V _{CCO}	5	P107	P53	V _{CCO} Bank 5*	-
M2	-	P106	P54	R3	292
I/O	5	-	-	N5	299
I/O	5	P103	P57	T2	302
I/O	5	-	-	P5	305
I/O	5	-	P58	Т3	308
GND	-	-	-	GND*	-
I/O, V _{REF}	5	P102	P59	T4	311
I/O	5	-	P60	M6	314
I/O	5	-	-	T5	317
I/O	5	P101	P61	N6	320
I/O	5	P100	P62	R5	323

XC2S50 Device Pinouts (Continued)

XC2S50 Pad Name					Bndry
Function	Bank	TQ144	PQ208	FG256	Scan
I/O	0	-	-	D8	83
I/O	0	-	P188	A6	86
I/O, V _{REF}	0	P12	P189	B7	89
GND	-	-	P190	GND*	-
I/O	0	-	P191	C8	92
I/O	0	-	P192	D7	95
I/O	0	-	P193	E7	98
I/O	0	P11	P194	C7	104
I/O	0	P10	P195	B6	107
V _{CCINT}	-	P9	P196	V _{CCINT} *	-
V _{CCO}	0	-	P197	V _{CCO} Bank 0*	-
GND	-	P8	P198	GND*	-
I/O	0	P7	P199	A5	110
I/O	0	P6	P200	C6	113
I/O	0	-	P201	B5	116
I/O	0	-	-	D6	119
I/O	0	-	P202	A4	122
I/O, V _{REF}	0	P5	P203	B4	125
GND	-	-	-	GND*	-
I/O	0	-	P204	E6	128
I/O	0	-	-	D5	131
I/O	0	P4	P205	A3	134
I/O	0	-	-	C5	137
I/O	0	P3	P206	B3	140
TCK	-	P2	P207	C4	-
V _{CCO}	0	P1	P208	V _{CCO} Bank 0*	-
V _{CCO}	7	P144	P208	V _{CCO} Bank 7*	-

04/18/01

Notes:

- 1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
- Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
- 3. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S50 Package Pins

TQ1	44
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Not Connected Pins								
P104	P105	-	-	-	-			
11/02/00								

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						Bndry
Function	Bank	TQ144 PQ208		FG256	FG456	Scan
I/O	2	-	-	F12	G20	695
I/O	2	-	P149	E15	F19	701
I/O, V _{REF}	2	P41	P150	F13	F21	704
V _{CCO}	2	-	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	-	-	GND*	GND*	-
I/O	2	-	P151	E14	F20	707
I/O	2	-	-	C16	F18	710
I/O	2	-	-	-	E21	713
I/O	2	P40	P152	E13	D22	716
I/O	2	-	-	B16	E20	719
I/O (DIN, D0)	2	P39	P153	D14	D20	725
I/O (DOUT, BUSY)	2	P38	P154	C15	C21	728
CCLK	2	P37	P155	D15	B22	731
V _{CCO}	2	P36	P156	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
V _{CCO}	1	P35	P156	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
TDO	2	P34	P157	B14	A21	-
GND	-	P33	P158	GND*	GND*	-
TDI	-	P32	P159	A15	B20	-
I/O (CS)	1	P31	P160	B13	C19	0
I/O (WRITE)	1	P30	P161	C13	A20	3
I/O	1	-	-	C12	D17	9
I/O	1	P29	P162	A14	A19	12
I/O	1	-	-	-	B18	15
I/O	1	-	-	D12	C17	18
I/O	1	-	P163	B12	D16	21
GND	-	-	-	GND*	GND*	-
V _{CCO}	1	-	-	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
I/O, V _{REF}	1	P28	P164	C11	A18	24
I/O	1	-	P165	A13	B17	27
I/O	1	-	-	D11	D15	33
I/O	1	-	P166	A12	C16	36
I/O	1	-	-	-	D14	39
I/O, V _{REF}	1	P27	P167	E11	E14	42
I/O	1	P26	P168	B11	A16	45
GND	-	P25	P169	GND*	GND*	-

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						Bndrv
Function	Bank	TQ144	PQ208	FG256	FG456	Scan
V _{CCO}	1	-	P170	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCINT}	-	P24	P171	V_{CCINT}^{*}	V _{CCINT} *	-
I/O	1	P23	P172	A11	C15	48
I/O	1	P22	P173	C10	B15	51
I/O	1	-	-	-	F12	54
I/O	1	-	P174	B10	C14	57
I/O	1	-	P175	D10	D13	63
I/O	1	-	P176	A10	C13	66
GND	-	-	P177	GND*	GND*	-
I/O, V _{REF}	1	P21	P178	B9	B13	69
I/O	1	-	P179	E10	E12	72
I/O	1	-	-	A9	B12	75
I/O	1	P20	P180	D9	D12	78
I/O	1	P19	P181	A8	D11	84
I, GCK2	1	P18	P182	C9	A11	90
GND	-	P17	P183	GND*	GND*	-
V _{CCO}	1	P16	P184	V _{CCO} Bank 1*	V _{CCO} Bank 1*	-
V _{CCO}	0	P16	P184	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
I, GCK3	0	P15	P185	B8	C11	91
V _{CCINT}	-	P14	P186	V _{CCINT} *	V_{CCINT}^{*}	-
I/O	0	P13	P187	A7	A10	101
I/O	0	-	-	D8	B10	104

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						Bndry
Function	Bank	TQ144	PQ208	FG256	FG456	Scan
I/O	0	-	P188	A6	C10	107
I/O, V _{REF}	0	P12	P189	B7	A9	110
GND	-	-	P190	GND*	GND*	-
I/O	0	-	P191	C8	B9	113
I/O	0	-	P192	D7	E10	116
I/O	0	-	P193	E7	A8	122
I/O	0	-	-	-	D9	125
I/O	0	P11	P194	C7	E9	128
I/O	0	P10	P195	B6	A7	131
V _{CCINT}	-	P9	P196	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	0	-	P197	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	P8	P198	GND*	GND*	-
I/O	0	P7	P199	A5	B7	134
I/O, V _{REF}	0	P6	P200	C6	E8	137
I/O	0	-	-	-	D8	140
I/O	0	-	P201	B5	C7	143
I/O	0	-	-	D6	D7	146
I/O	0	-	P202	A4	D6	152
I/O, V _{REF}	0	P5	P203	B4	C6	155
V _{CCO}	0	-	-	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
GND	-	-	-	GND*	GND*	-
I/O	0	-	P204	E6	B5	158
I/O	0	-	-	D5	E7	161
I/O	0	-	-	-	E6	164
I/O	0	P4	P205	A3	B4	167
I/O	0	-	-	C5	A3	170
I/O	0	P3	P206	B3	C5	176
ТСК	-	P2	P207	C4	C4	-
V _{CCO}	0	P1	P208	V _{CCO} Bank 0*	V _{CCO} Bank 0*	-
V _{CCO}	7	P144	P208	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-

^{04/18/01}

Notes:

- 1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
- Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
- 3. See "VCCO Banks" for details on V_{CCO} banking.

XC2S150 Device Pinouts

XC2S150 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	221
I/O	7	-	-	E4	224
I/O	7	-	-	C1	227
I/O	7	-	A2	F5	230
GND	-	-	GND*	GND*	-
I/O	7	P4	B1	D2	233
I/O	7	-	-	E3	236
I/O	7	-	-	F4	239
I/O	7	-	E3	G5	242
I/O	7	P5	D2	F3	245
GND	-	-	GND*	GND*	-
V _{CCO}	7	-	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
I/O, V _{REF}	7	P6	C1	E2	248
I/O	7	P7	F3	E1	251
I/O	7	-	-	G4	254
I/O	7	-	-	G3	257
I/O	7	-	E2	H5	260
I/O	7	P8	E4	F2	263
I/O	7	-	-	F1	266
I/O, V _{REF}	7	P9	D1	H4	269
I/O	7	P10	E1	G1	272
GND	-	P11	GND*	GND*	-
V _{CCO}	7	P12	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCINT}	-	P13	V _{CCINT} *	V _{CCINT} *	-
I/O	7	P14	F2	H3	275
I/O	7	P15	G3	H2	278
I/O	7	-	-	H1	284
I/O	7	-	F1	J5	287
I/O	7	P16	F4	J2	290
I/O	7	-	-	J3	293
I/O	7	P17	F5	K5	299
I/O	7	P18	G2	K1	302
GND	-	P19	GND*	GND*	-
V _{CCO}	7	-	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
I/O, V _{REF}	7	P20	H3	K3	305
I/O	7	P21	G4	K4	308
I/O	7	-	H2	L6	311

XC2S150 Device Pinouts (Continued)

XC2S150 Pad Name					Bndry
Function	Bank	PQ208	FG256	FG456	Scan
I/O	7	P22	G5	L1	314
I/O	7	-	-	L5	317
I/O	7	P23	H4	L4	320
I/O, IRDY ⁽¹⁾	7	P24	G1	L3	323
GND	-	P25	GND*	GND*	-
V _{CCO}	7	P26	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCO}	6	P26	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
I/O, TRDY ⁽¹⁾	6	P27	J2	M1	326
V _{CCINT}	-	P28	V_{CCINT}^{*}	V_{CCINT}^{*}	-
I/O	6	-	-	M6	332
I/O	6	P29	H1	M3	335
I/O	6	-	J4	M4	338
I/O	6	P30	J1	M5	341
I/O, V _{REF}	6	P31	J3	N2	344
V _{CCO}	6	-	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	347
I/O	6	P34	K2	N4	350
I/O	6	-	-	N5	356
I/O	6	P35	K1	P2	359
I/O	6	-	K3	P4	362
I/O	6	-	-	R1	365
I/O	6	P36	L1	P3	371
I/O	6	P37	L2	R2	374
V _{CCINT}	-	P38	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	6	P39	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	377
I/O, V _{REF}	6	P42	M1	R4	380
I/O	6	-	-	T2	383
I/O	6	P43	L4	U1	386
I/O	6	-	M2	R5	389
I/O	6	-	-	V1	392
I/O	6	-	-	T5	395
I/O	6	P44	L3	U2	398
I/O, V _{REF}	6	P45	N1	Т3	401
V _{CCO}	6	-	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-

Additional XC2S150 Package Pins

PQ208

Not Connected Pins								
P55	P56	-	-	-	-			
11/02/00	•	*	*	*				

FG256

V _{CCINT} Pins								
C3	C14	D4	D13	E5	E12			
M5	M12	N4	N13	P3	P14			
	1	V _{CCO} Ba	nk 0 Pins					
E8	F8	-	-	-	-			
		V _{CCO} Ba	nk 1 Pins					
E9	F9	-	-	-	-			
	1	V _{CCO} Ba	nk 2 Pins					
H11	H12	-	-	-	-			
	1	V _{CCO} Ba	nk 3 Pins					
J11	J12	-	-	-	-			
		V _{CCO} Ba	nk 4 Pins					
L9	M9	-	-	-	-			
		V _{CCO} Ba	nk 5 Pins					
L8	M8	-	-	-	-			
	1	V _{CCO} Ba	nk 6 Pins					
J5	J6	-	-	-	-			
		V _{CCO} Ba	nk 7 Pins					
H5	H6	-	-	-	-			
		GND	Pins					
A1	A16	B2	B15	F6	F7			
F10	F11	G6	G7	G8	G9			
G10	G11	H7	H8	H9	H10			
J7	J8	J9	J10	K6	K7			
K8	K9	K10	K11	L6	L7			
L10	L11	R2	R15	T1	T16			
	1	Not Conn	ected Pins	1				
P4	R4	-	-	-	-			
11/02/00								

Additional XC2S150 Package Pins (Continued)

FG456

V _{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	Т9	T14	T15	T16
U6	U17	V5	V18	-	-
V _{CCO} Bank 0 Pins					
F7	F8	F9	F10	G10	G11
V _{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V _{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V _{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V _{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V _{CCO} Bank 5 Pins					
T10	T11	U7	U8	U9	U10
V _{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	Т6
V _{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A6	A12	A13	A14	B11
B16	C2	C8	C9	D1	D4
D18	D19	E13	E17	E19	F11
G2	G22	H21	J1	J4	K2
K18	K19	L2	L19	M2	M17
M21	N1	P1	P5	P22	R3
R20	R22	U3	U18	V6	W4
W13	W15	W19	Y5	Y22	AA1
AA3	AA9	AA10	AA11	AA16	AB7
AB8	AB12	AB14	AB21	-	-

11/02/00