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Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

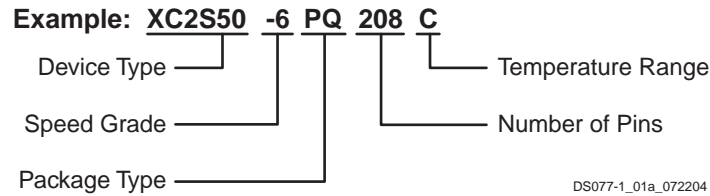
Details

Product Status	Active
Number of LABs/CLBs	1176
Number of Logic Elements/Cells	5292
Total RAM Bits	57344
Number of I/O	176
Number of Gates	200000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-BGA
Supplier Device Package	256-FBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s200-6fgg256c

Ordering Information

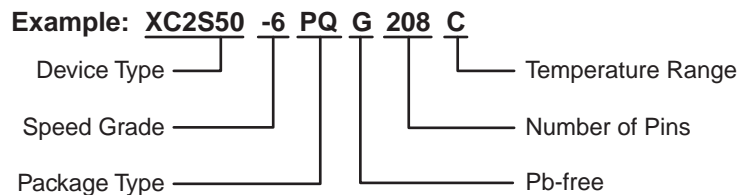
Spartan-II devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

Standard Packaging



DS077-1_01a_072204

Pb-Free Packaging



DS077-1_01b_072204

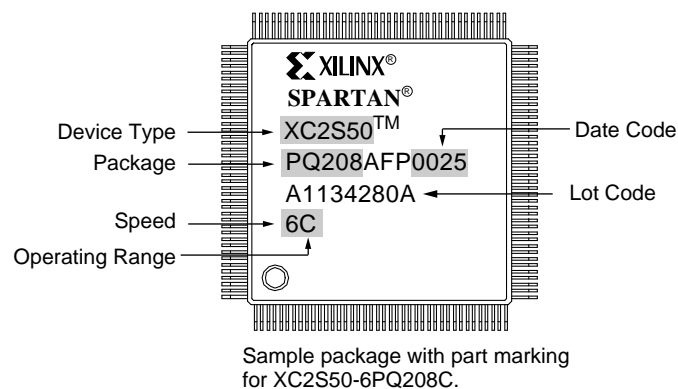
Device Ordering Options

Device	Speed Grade		Number of Pins / Package Type		Temperature Range (T _J)	
XC2S15	-5	Standard Performance	VQ(G)100	100-pin Plastic Very Thin QFP	C = Commercial	0°C to +85°C
XC2S30	-6	Higher Performance ⁽¹⁾	CS(G)144	144-ball Chip-Scale BGA	I = Industrial	-40°C to +100°C
XC2S50			TQ(G)144	144-pin Plastic Thin QFP		
XC2S100			PQ(G)208	208-pin Plastic QFP		
XC2S150			FG(G)256	256-ball Fine Pitch BGA		
XC2S200			FG(G)456	456-ball Fine Pitch BGA		

Notes:

- The -6 speed grade is exclusively available in the Commercial temperature range.

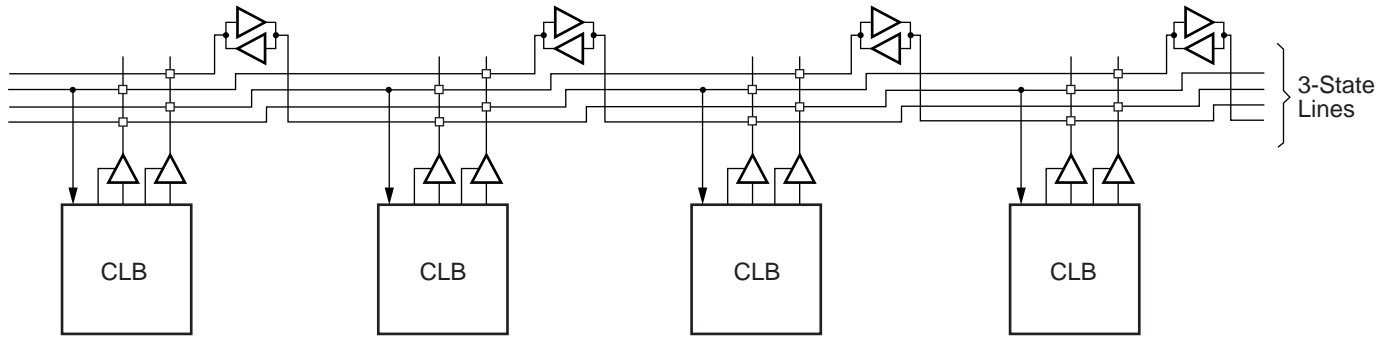
Device Part Marking



ds001-1_02_090303

Revision History

Date	Version No.	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Added industrial temperature range information.
10/31/00	2.1	Removed Power down feature.
03/05/01	2.2	Added statement on PROMs.
11/01/01	2.3	Updated Product Availability chart. Minor text edits.
09/03/03	2.4	Added device part marking.
08/02/04	2.5	Added information on Pb-free packaging options and removed discontinued options.
06/13/08	2.8	Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.



DS001_07_090600

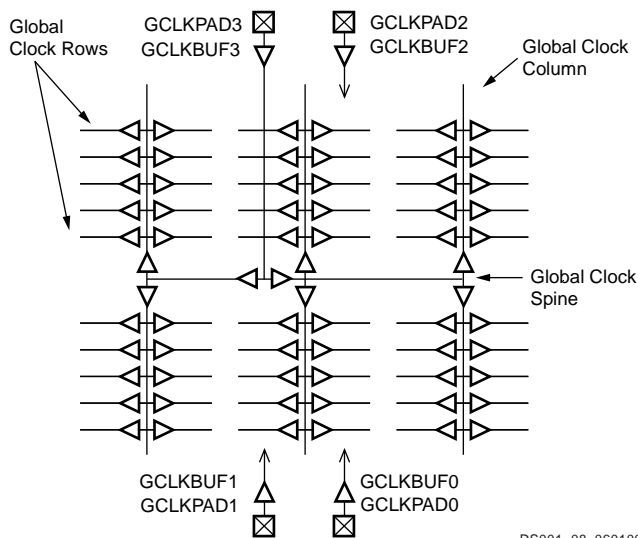
Figure 7: BUFT Connections to Dedicated Horizontal Bus Lines

Clock Distribution

The Spartan-II family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 8.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing. Global clock pins do not have the option for internal, weak pull-up resistors.



DS001_08_060100

Figure 8: Global Clock Distribution Network

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock

networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-II devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

Boundary Scan

Spartan-II devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains.

The TAP uses dedicated package pins that always operate using LVTTTL. For TDO to operate using LVTTTL, the V_{CCO} for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO} . TDI, TMS, and TCK have a default internal weak pull-up resistor, and TDO has no default resistor. Bitstream options allow setting any of the four TAP pins to have an internal pull-up, pull-down, or neither.

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

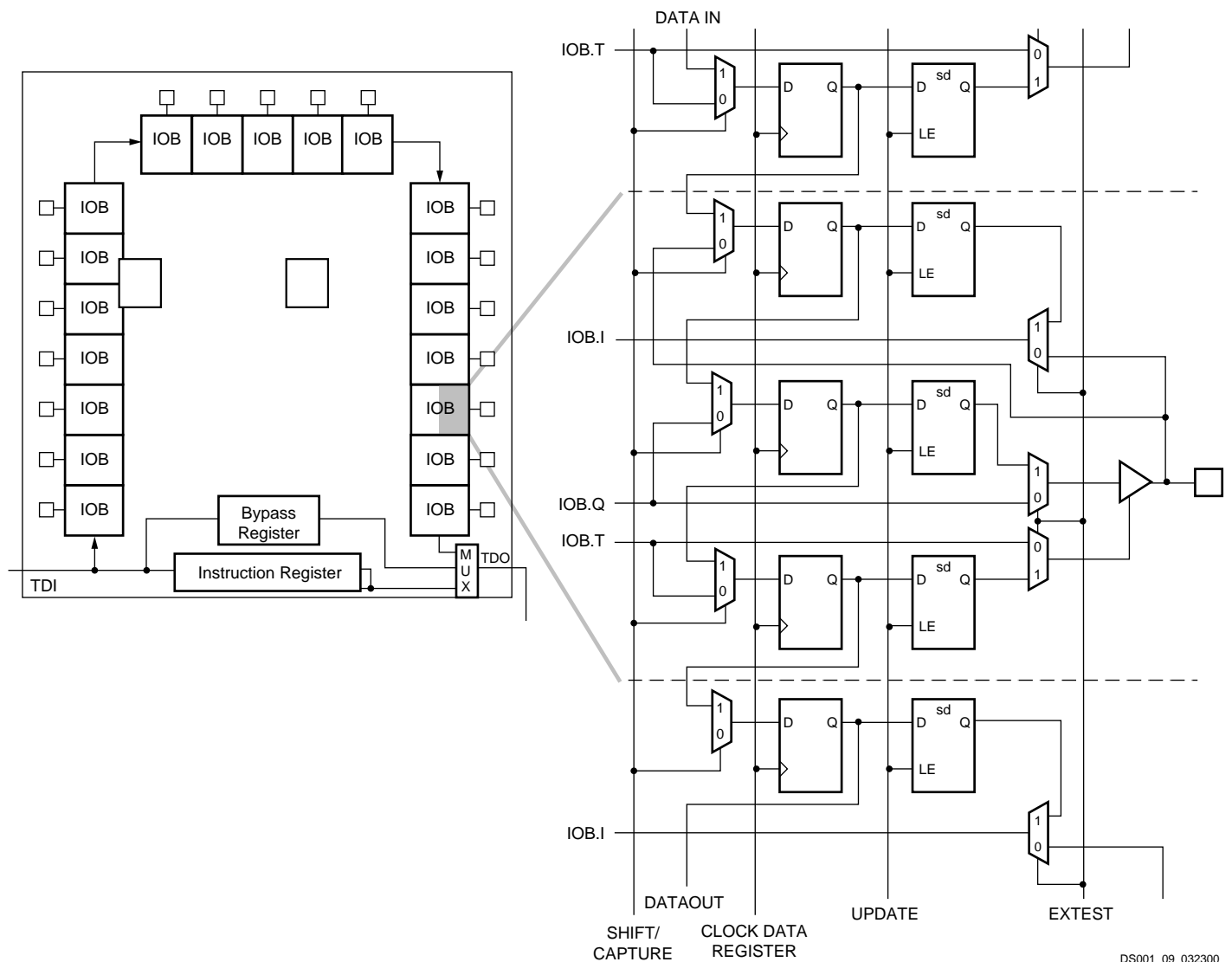


Figure 9: Spartan-II Family Boundary Scan Logic

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contribute all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the [Downloads](#) area.

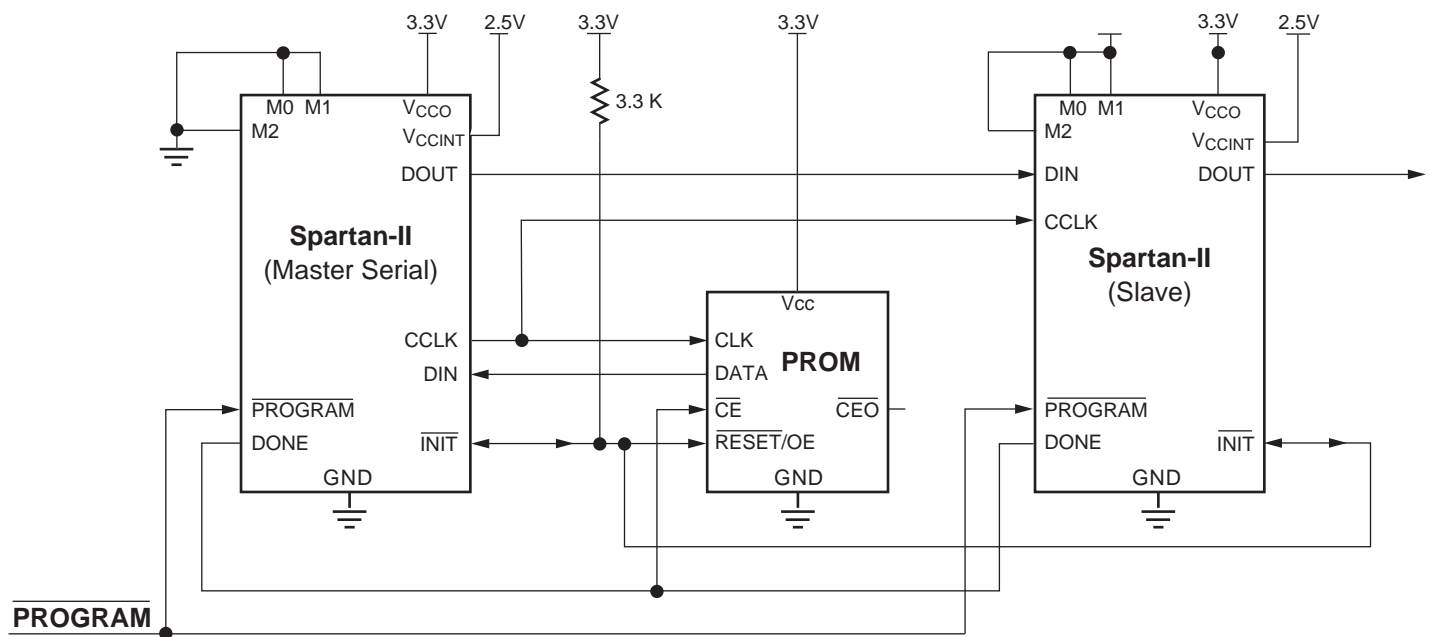
Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is $2^{20}-1$ (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until INIT pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.

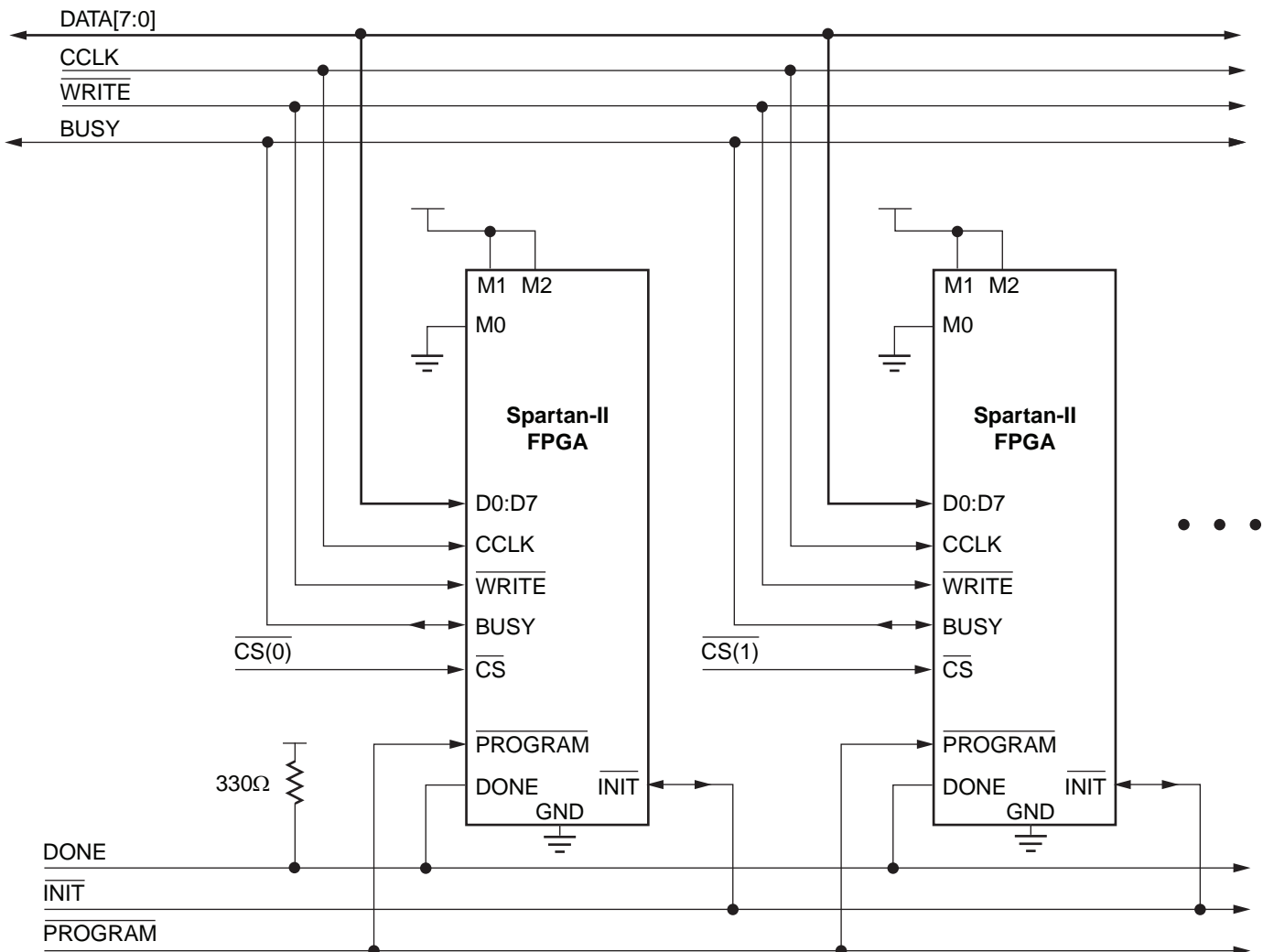


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Notes:

1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 15: Master/Slave Serial Configuration Circuit Diagram



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Figure 18: Slave Parallel Configuration Circuit Diagram

Multiple Spartan-II FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See "Start-up," page 19.

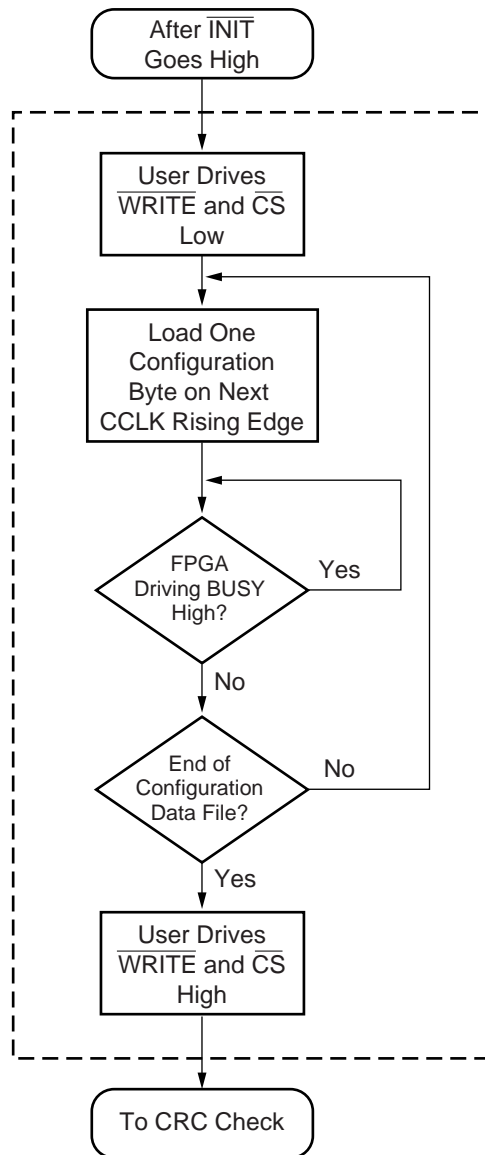
Write

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 19, page 25 shows a flowchart of the write sequence used to load data into the Spartan-II FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 11, page 18. The timing for write operations is shown in Figure 20, page 26.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise an abort will be initiated, as in the next section.

1. Drive data onto D0:D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
2. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
3. Repeat steps 1 and 2 until all the data has been sent.
4. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

If CCLK is slower than F_{CCNH} , the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.



DS001_19_032300

Figure 19: Loading Configuration Data for the Slave Parallel Mode

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of \overline{CS} .

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the \overline{CS} signal may be de-asserted until the next byte is valid on D0-D7. While \overline{CS} is High, the Slave Parallel

interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, \overline{WRITE} must continue to be asserted while \overline{CS} is asserted.

Abort

To abort configuration during a write sequence, de-assert \overline{WRITE} while holding \overline{CS} Low. The abort operation is initiated at the rising edge of CCLK, as shown in Figure 21, page 26. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

Boundary-Scan Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2).

Readback

The configuration data stored in the Spartan-II FPGA configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see [XAPP176](#), *Spartan-II FPGA Family Configuration and Readback*.

Design Considerations

This section contains more detailed design information on the following features:

- Delay-Locked Loop . . . see [page 27](#)
- Block RAM . . . see [page 32](#)
- Versatile I/O . . . see [page 36](#)

Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

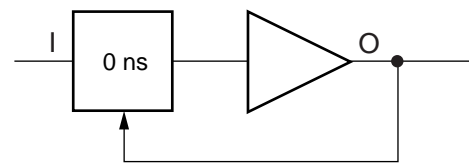
In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of

the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

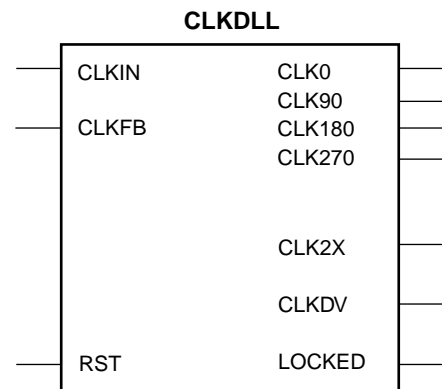
Library DLL Primitives

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.



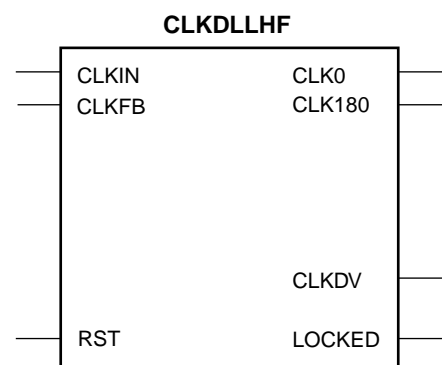
DS001_22_032300

Figure 22: Simplified DLL Macro BUFGDLL



DS001_23_032300

Figure 23: Standard DLL Primitive CLKDLL



DS001_24_032300

Figure 24: High-Frequency DLL Primitive CLKDLLHF

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 25.

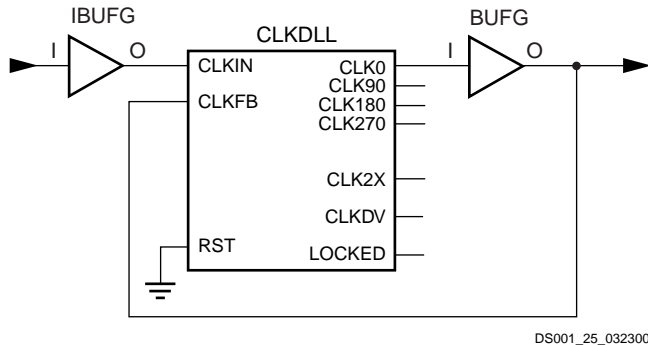


Figure 25: BUFGDLL Block Diagram

This macro does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This macro also does not provide access to the RST or LOCKED pins of the DLL. For access to these features, a designer must use the DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG primitive, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50/50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL

or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. Either a global clock buffer (BUFG) or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feed back to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software to determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates, the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or be tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer deskew with respect to one another. The DLL must be reset when the input clock frequency changes, if the device is reconfigured in Boundary-Scan mode, if the device undergoes a hot swap, and after the device is configured if the input clock is not stable during the startup sequence.

2x Clock Output — CLK2X

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

Clock Divide Output — CLKDV

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction. The CLKDV output pin has a 50/50 duty cycle for all values of the

PCI — Peripheral Component Interface

The Peripheral Component Interface (PCI) standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTTL input buffer and a push-pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}). I/Os configured for the PCI, 33 MHz, 5V standard are also 5V-tolerant.

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic (GTL) standard is a high-speed bus standard (JESD8.3). Xilinx has implemented the terminated variation of this standard. This standard requires a differential amplifier input buffer and an open-drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus (GTL+) standard is a high-speed bus standard (JESD8.3).

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic (HSTL) standard is a general purpose high-speed, 1.5V bus standard (EIA/JESD 8-6). This standard has four variations or classes. Versatile I/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V (SSTL3) standard is a general purpose 3.3V memory bus standard (JESD8-8). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V (SSTL2) standard is a general purpose 2.5V memory bus standard (JESD8-9). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated (CTT) standard is a 3.3V memory bus standard (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with processors for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

Library Primitives

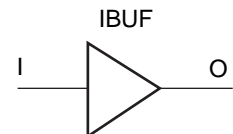
The Xilinx library includes an extensive list of primitives designed to provide support for the variety of Versatile I/O features. Most of these primitives represent variations of the five generic Versatile I/O primitives:

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

These primitives are available with various extensions to define the desired I/O standard. However, it is recommended that customers use a property or attribute on the generic primitive to specify the I/O standard. See "[Versatile I/O Properties](#)".

IBUF

Signals used as inputs to the Spartan-II device must source an input buffer (IBUF) via an external input port. The generic IBUF primitive appears in [Figure 35](#). The assumed standard is LVTTTL when the generic IBUF has no specified extension or property.



DS001_35_061200

Figure 35: Input Buffer (IBUF) Primitive

When the IBUF primitive supports an I/O standard such as LVTTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard ($V_{CCO} < 2V$), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See [Figure 36](#) for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 42. Table 20 lists DC voltage specifications for the GTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

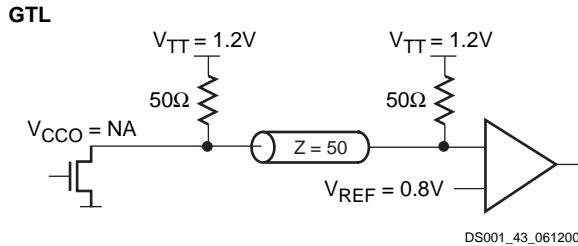


Figure 42: Terminated GTL

Table 20: GTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}^{(1)}$	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} \geq V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} \leq V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.4V	32	-	-
I_{OL} at V_{OL} (mA) at 0.2V	-	-	40

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 43. DC voltage specifications appear in Table 21 for the GTL+ standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

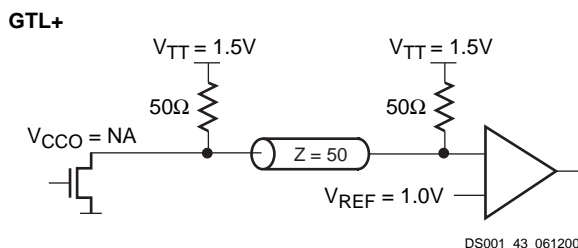


Figure 43: Terminated GTL+

Table 21: GTL+ Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}^{(1)}$	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} \geq V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} \leq V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.6V	36	-	-
I_{OL} at V_{OL} (mA) at 0.3V	-	-	48

Notes:

1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

HSTL Class I

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 44. DC voltage specifications appear in Table 22 for the HSTL_1 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

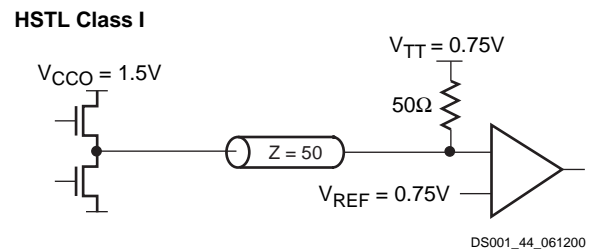


Figure 44: Terminated HSTL Class I

Table 22: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	-8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T _J	Junction temperature ⁽¹⁾	Commercial	0	85	°C
		Industrial	−40	100	°C
V _{CCINT}	Supply voltage relative to GND ^(2,5)	Commercial	2.5 − 5%	2.5 + 5%	V
		Industrial	2.5 − 5%	2.5 + 5%	V
V _{CCO}	Supply voltage relative to GND ^(3,5)	Commercial	1.4	3.6	V
		Industrial	1.4	3.6	V
T _{IN}	Input signal transition time ⁽⁴⁾		-	250	ns

Notes:

- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
- Functional operation is guaranteed down to a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} – 10%). For every 50 mV reduction in V_{CCINT} below 2.375V (nominal V_{CCINT} – 5%), all delay parameters increase by 3%.
- Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
- Input and output measurement threshold is ~50% of V_{CCO} . See "Delay Measurement Methodology," page 60 for specific levels.
- Supply voltages may be applied in any order desired.

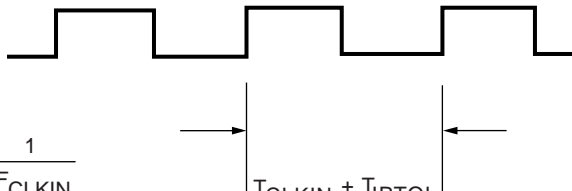
DC Characteristics Over Operating Conditions

Symbol	Description			Min	Typ	Max	Units
V _{DRINT}	Data Retention V _{CCINT} voltage (below which configuration data may be lost)			2.0	-	-	V
V _{DRIO}	Data Retention V _{CCO} voltage (below which configuration data may be lost)			1.2	-	-	V
I _{CCINTQ}	Quiescent V _{CCINT} supply current ⁽¹⁾	XC2S15	Commercial	-	10	30	mA
			Industrial	-	10	60	mA
		XC2S30	Commercial	-	10	30	mA
			Industrial	-	10	60	mA
		XC2S50	Commercial	-	12	50	mA
			Industrial	-	12	100	mA
		XC2S100	Commercial	-	12	50	mA
			Industrial	-	12	100	mA
		XC2S150	Commercial	-	15	50	mA
			Industrial	-	15	100	mA
		XC2S200	Commercial	-	15	75	mA
			Industrial	-	15	150	mA
I _{CCOQ}	Quiescent V _{CCO} supply current ⁽¹⁾			-	-	2	mA
I _{REF}	V _{REF} current per V _{REF} pin			-	-	20	μA
I _L	Input or output leakage current ⁽²⁾			-10	-	+10	μA
C _{IN}	Input capacitance (sample tested)	VQ, CS, TQ, PQ, FG packages		-	-	8	pF
I _{RPU}	Pad pull-up (when selected) @ V _{IN} = 0V, V _{CCO} = 3.3V (sample tested) ⁽³⁾			-	-	0.25	mA
I _{RPD}	Pad pull-down (when selected) @ V _{IN} = 3.6V (sample tested) ⁽³⁾			-	-	0.15	mA

Notes:

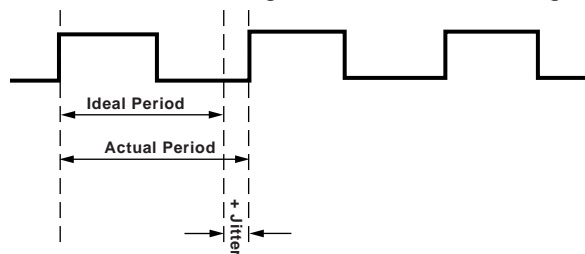
- With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
- The I/O leakage current specification applies only when the V_{CCINT} and V_{CCO} supply voltages have reached their respective minimum Recommended Operating Conditions.
- Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

Period Tolerance: the allowed input clock period change in nanoseconds.

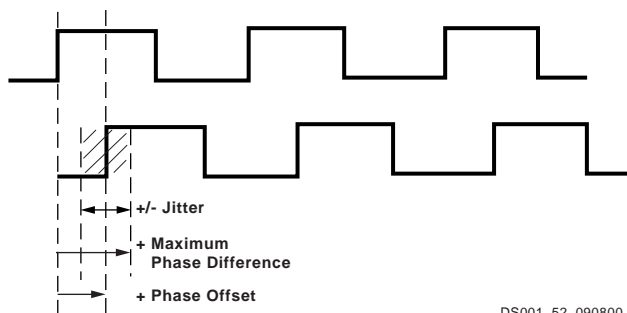
$$T_{CLKIN} = \frac{1}{F_{CLKIN}}$$


$$T_{CLKIN} \pm T_{IPTOL}$$

Output Jitter: the difference between an ideal reference clock edge and the actual design.



Phase Offset and Maximum Phase Difference



DS001_52_090800

Figure 52: Period Tolerance and Clock Jitter

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Combinatorial Delays						
T _{OPX}	F operand inputs to X via XOR	-	0.8	-	0.9	ns
T _{OPXB}	F operand input to XB output	-	1.3	-	1.5	ns
T _{OPY}	F operand input to Y via XOR	-	1.7	-	2.0	ns
T _{OPYB}	F operand input to YB output	-	1.7	-	2.0	ns
T _{OPCYF}	F operand input to COUT output	-	1.3	-	1.5	ns
T _{OPGY}	G operand inputs to Y via XOR	-	0.9	-	1.1	ns
T _{OPGYB}	G operand input to YB output	-	1.6	-	2.0	ns
T _{OPCYG}	G operand input to COUT output	-	1.2	-	1.4	ns
T _{BXCY}	BX initialization input to COUT	-	0.9	-	1.0	ns
T _{CINX}	CIN input to X output via XOR	-	0.4	-	0.5	ns
T _{CINXB}	CIN input to XB	-	0.1	-	0.1	ns
T _{CINY}	CIN input to Y via XOR	-	0.5	-	0.6	ns
T _{CINYB}	CIN input to YB	-	0.6	-	0.7	ns
T _{BYP}	CIN input to COUT output	-	0.1	-	0.1	ns
Multiplier Operation						
T _{FANDXB}	F1/2 operand inputs to XB output via AND	-	0.5	-	0.5	ns
T _{FANDYB}	F1/2 operand inputs to YB output via AND	-	0.9	-	1.1	ns
T _{FANDCY}	F1/2 operand inputs to COUT output via AND	-	0.5	-	0.6	ns
T _{GANDYB}	G1/2 operand inputs to YB output via AND	-	0.6	-	0.7	ns
T _{GANDCY}	G1/2 operand inputs to COUT output via AND	-	0.2	-	0.2	ns
Setup/Hold Times with Respect to Clock CLK ⁽¹⁾						
T _{CCKX} / T _{CKCX}	CIN input to FFX	1.1 / 0	-	1.2 / 0	-	ns
T _{CCKY} / T _{CKCY}	CIN input to FFY	1.2 / 0	-	1.3 / 0	-	ns

Notes:

1. A zero hold time listing indicates no hold time or a negative hold time.

Package Thermal Characteristics

Table 39 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on [www.xilinx.com](http://www.xilinx.com/cgi-bin/thermal/thermal.pl) (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance (θ_{JC}) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board (θ_{JB})

value similarly reports the difference between the board and junction temperature. The junction-to-ambient (θ_{JA}) value reports the temperature difference between the ambient environment and the junction temperature. The θ_{JA} value is reported at different air velocities, measured in linear feet per minute (LFM). The “Still Air (0 LFM)” column shows the θ_{JA} value in a system without a fan. The thermal resistance drops with increasing air flow.

Table 39: Spartan-II Package Thermal Characteristics

Package	Device	Junction-to-Case (θ_{JC})	Junction-to-Board (θ_{JB})	Junction-to-Ambient (θ_{JA}) at Different Air Flows				Units
				Still Air (0 LFM)	250 LFM	500 LFM	750 LFM	
VQ100 VQG100	XC2S15	11.3	N/A	44.1	36.7	34.2	33.3	°C/Watt
	XC2S30	10.1	N/A	40.7	33.9	31.5	30.8	°C/Watt
TQ144 TQG144	XC2S15	7.3	N/A	38.6	30.0	25.7	24.1	°C/Watt
	XC2S30	6.7	N/A	34.7	27.0	23.1	21.7	°C/Watt
	XC2S50	5.8	N/A	32.2	25.1	21.4	20.1	°C/Watt
	XC2S100	5.3	N/A	31.4	24.4	20.9	19.6	°C/Watt
CS144 CSG144	XC2S30	2.8	N/A	34.0	26.0	23.9	23.2	°C/Watt
PQ208 PQG208	XC2S50	6.7	N/A	25.2	18.6	16.4	15.2	°C/Watt
	XC2S100	5.9	N/A	24.6	18.1	16.0	14.9	°C/Watt
	XC2S150	5.0	N/A	23.8	17.6	15.6	14.4	°C/Watt
	XC2S200	4.1	N/A	23.0	17.0	15.0	13.9	°C/Watt
FG256 FGG256	XC2S50	7.1	17.6	27.2	21.4	20.3	19.8	°C/Watt
	XC2S100	5.8	15.1	25.1	19.5	18.3	17.8	°C/Watt
	XC2S150	4.6	12.7	23.0	17.6	16.3	15.8	°C/Watt
	XC2S200	3.5	10.7	21.4	16.1	14.7	14.2	°C/Watt
FG456 FGG456	XC2S150	2.0	N/A	21.9	17.3	15.8	15.2	°C/Watt
	XC2S200	2.0	N/A	21.0	16.6	15.1	14.5	°C/Watt

XC2S30 Device Pinouts (Continued)

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
I/O	4	-	-	-	P87	295
I/O	4	-	-	-	P88	298
I/O	4	-	P84	K8	P89	301
I/O	4	-	P83	N9	P90	304
V _{CCINT}	-	P42	P82	M9	P91	-
V _{CCO}	4	-	-	-	P92	-
GND	-	-	P81	L9	P93	-
I/O	4	P43	P80	K9	P94	307
I/O	4	P44	P79	N10	P95	310
I/O	4	-	P78	M10	P96	313
I/O, V _{REF}	4	P45	P77	L10	P98	316
I/O	4	-	-	-	P99	319
I/O	4	-	P76	N11	P100	322
I/O	4	P46	P75	M11	P101	325
I/O	4	P47	P74	L11	P102	328
GND	-	P48	P73	N12	P103	-
DONE	3	P49	P72	M12	P104	331
V _{CCO}	4	P50	P71	N13	P105	-
V _{CCO}	3	P50	P70	M13	P105	-
PROGRAM	-	P51	P69	L12	P106	334
I/O (INIT)	3	P52	P68	L13	P107	335
I/O (D7)	3	P53	P67	K10	P108	338
I/O	3	-	P66	K11	P109	341
I/O	3	-	-	-	P110	344
I/O, V _{REF}	3	P54	P65	K12	P111	347
I/O	3	-	P64	K13	P113	350
I/O	3	P55	P63	J10	P114	353
I/O (D6)	3	P56	P62	J11	P115	356
GND	-	-	P61	J12	P116	-
V _{CCO}	3	-	-	-	P117	-
I/O (D5)	3	P57	P60	J13	P119	359
I/O	3	P58	P59	H10	P120	362
I/O	3	-	-	-	P121	365
I/O	3	-	-	-	P122	368
I/O	3	-	-	-	P123	371
GND	-	-	-	-	P124	-
I/O, V _{REF}	3	P59	P58	H11	P125	374
I/O (D4)	3	P60	P57	H12	P126	377
I/O	3	-	P56	H13	P127	380
V _{CCINT}	-	P61	P55	G12	P128	-
I/O, TRDY ⁽¹⁾	3	P62	P54	G13	P129	386

XC2S30 Device Pinouts (Continued)

XC2S30 Pad Name		VQ100	TQ144	CS144	PQ208	Bndry Scan
Function	Bank					
V _{CCO}	3	P63	P53	G11	P130	-
V _{CCO}	2	P63	P53	G11	P130	-
GND	-	P64	P52	G10	P131	-
I/O, IRDY ⁽¹⁾	2	P65	P51	F13	P132	389
I/O	2	-	-	-	P133	392
I/O	2	-	P50	F12	P134	395
I/O (D3)	2	P66	P49	F11	P135	398
I/O, V _{REF}	2	P67	P48	F10	P136	401
GND	-	-	-	-	P137	-
I/O	2	-	-	-	P138	404
I/O	2	-	-	-	P139	407
I/O	2	-	-	-	P140	410
I/O	2	P68	P47	E13	P141	413
I/O (D2)	2	P69	P46	E12	P142	416
V _{CCO}	2	-	-	-	P144	-
GND	-	-	P45	E11	P145	-
I/O (D1)	2	P70	P44	E10	P146	419
I/O	2	P71	P43	D13	P147	422
I/O	2	-	P42	D12	P148	425
I/O, V _{REF}	2	P72	P41	D11	P150	428
I/O	2	-	-	-	P151	431
I/O	2	-	P40	C13	P152	434
I/O (DIN, D0)	2	P73	P39	C12	P153	437
I/O (DOUT, BUSY)	2	P74	P38	C11	P154	440
CCLK	2	P75	P37	B13	P155	443
V _{CCO}	2	P76	P36	B12	P156	-
V _{CCO}	1	P76	P35	A13	P156	-
TDO	2	P77	P34	A12	P157	-
GND	-	P78	P33	B11	P158	-
TDI	-	P79	P32	A11	P159	-
I/O (CS)	1	P80	P31	D10	P160	0
I/O (WRITE)	1	P81	P30	C10	P161	3
I/O	1	-	P29	B10	P162	6
I/O	1	-	-	-	P163	9
I/O, V _{REF}	1	P82	P28	A10	P164	12
I/O	1	-	-	-	P166	15
I/O	1	P83	P27	D9	P167	18
I/O	1	P84	P26	C9	P168	21
GND	-	-	P25	B9	P169	-
V _{CCO}	1	-	-	-	P170	-

Additional XC2S50 Package Pins (Continued)

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

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FG256

V _{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V _{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V _{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V _{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V _{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V _{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V _{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V _{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V _{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

11/02/00

XC2S100 Device Pinouts

XC2S100 Pad Name						
Function	Bank	TQ144	PQ208	FG256	FG456	Bndry Scan
GND	-	P143	P1	GND*	GND*	-
TMS	-	P142	P2	D3	D3	-
I/O	7	P141	P3	C2	B1	185
I/O	7	-	-	A2	F5	191
I/O	7	P140	P4	B1	D2	194
I/O	7	-	-	-	E3	197
I/O	7	-	-	E3	G5	200
I/O	7	-	P5	D2	F3	203
GND	-	-	-	GND*	GND*	-
V _{CCO}	7	-	-	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
I/O, V _{REF}	7	P139	P6	C1	E2	206

XC2S100 Device Pinouts (Continued)

XC2S100 Pad Name						
Function	Bank	TQ144	PQ208	FG256	FG456	Bndry Scan
I/O	7	-	P7	F3	E1	209
I/O	7	-	-	E2	H5	215
I/O	7	P138	P8	E4	F2	218
I/O	7	-	-	-	F1	221
I/O, V _{REF}	7	P137	P9	D1	H4	224
I/O	7	P136	P10	E1	G1	227
GND	-	P135	P11	GND*	GND*	-
V _{CCO}	7	-	P12	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCINT}	-	-	P13	V _{CCINT} *	V _{CCINT} *	-
I/O	7	P134	P14	F2	H3	230
I/O	7	P133	P15	G3	H2	233
I/O	7	-	-	F1	J5	236
I/O	7	-	P16	F4	J2	239
I/O	7	-	P17	F5	K5	245
I/O	7	-	P18	G2	K1	248
GND	-	-	P19	GND*	GND*	-
I/O, V _{REF}	7	P132	P20	H3	K3	251
I/O	7	P131	P21	G4	K4	254
I/O	7	-	-	H2	L6	257
I/O	7	P130	P22	G5	L1	260
I/O	7	-	P23	H4	L4	266
I/O, IRDY ⁽¹⁾	7	P129	P24	G1	L3	269
GND	-	P128	P25	GND*	GND*	-
V _{CCO}	7	P127	P26	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCO}	6	P127	P26	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
I/O, TRDY ⁽¹⁾	6	P126	P27	J2	M1	272
V _{CCINT}	-	P125	P28	V _{CCINT} *	V _{CCINT} *	-
I/O	6	P124	P29	H1	M3	281
I/O	6	-	-	J4	M4	284
I/O	6	P123	P30	J1	M5	287
I/O, V _{REF}	6	P122	P31	J3	N2	290
GND	-	-	P32	GND*	GND*	-
I/O	6	-	P33	K5	N3	293
I/O	6	-	P34	K2	N4	296
I/O	6	-	P35	K1	P2	302
I/O	6	-	-	K3	P4	305
I/O	6	P121	P36	L1	P3	308
I/O	6	P120	P37	L2	R2	311

Additional XC2S150 Package Pins

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

11/02/00

FG256

V _{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V _{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V _{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V _{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V _{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V _{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V _{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V _{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V _{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

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Additional XC2S150 Package Pins (Continued)

FG456

V _{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V _{CCO} Bank 0 Pins					
F7	F8	F9	F10	G10	G11
V _{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V _{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V _{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V _{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V _{CCO} Bank 5 Pins					
T10	T11	U7	U8	U9	U10
V _{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V _{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A6	A12	A13	A14	B11
B16	C2	C8	C9	D1	D4
D18	D19	E13	E17	E19	F11
G2	G22	H21	J1	J4	K2
K18	K19	L2	L19	M2	M17
M21	N1	P1	P5	P22	R3
R20	R22	U3	U18	V6	W4
W13	W15	W19	Y5	Y22	AA1
AA3	AA9	AA10	AA11	AA16	AB7
AB8	AB12	AB14	AB21	-	-

11/02/00

XC2S200 Device Pinouts

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	257
I/O	7	-	-	E4	263
I/O	7	-	-	C1	266
I/O	7	-	A2	F5	269
GND	-	-	GND*	GND*	-
I/O, V _{REF}	7	P4	B1	D2	272
I/O	7	-	-	E3	275
I/O	7	-	-	F4	281
GND	-	-	GND*	GND*	-
I/O	7	-	E3	G5	284
I/O	7	P5	D2	F3	287
GND	-	-	GND*	GND*	-
V _{CCO}	7	-	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
I/O, V _{REF}	7	P6	C1	E2	290
I/O	7	P7	F3	E1	293
I/O	7	-	-	G4	296
I/O	7	-	-	G3	299
I/O	7	-	E2	H5	302
GND	-	-	GND*	GND*	-
I/O	7	P8	E4	F2	305
I/O	7	-	-	F1	308
I/O, V _{REF}	7	P9	D1	H4	314
I/O	7	P10	E1	G1	317
GND	-	P11	GND*	GND*	-
V _{CCO}	7	P12	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCINT}	-	P13	V _{CCINT} *	V _{CCINT} *	-
I/O	7	P14	F2	H3	320
I/O	7	P15	G3	H2	323
I/O	7	-	-	J4	326
I/O	7	-	-	H1	329
I/O	7	-	F1	J5	332
GND	-	-	GND*	GND*	-
I/O	7	P16	F4	J2	335
I/O	7	-	-	J3	338
I/O	7	-	-	J1	341
I/O	7	P17	F5	K5	344
I/O	7	P18	G2	K1	347
GND	-	P19	GND*	GND*	-

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V _{CCO}	7	-	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
I/O, V _{REF}	7	P20	H3	K3	350
I/O	7	P21	G4	K4	353
I/O	7	-	-	K2	359
I/O	7	-	H2	L6	362
I/O	7	P22	G5	L1	365
I/O	7	-	-	L5	368
I/O	7	P23	H4	L4	374
I/O, IRDY ⁽¹⁾	7	P24	G1	L3	377
GND	-	P25	GND*	GND*	-
V _{CCO}	7	P26	V _{CCO} Bank 7*	V _{CCO} Bank 7*	-
V _{CCO}	6	P26	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
I/O, TRDY ⁽¹⁾	6	P27	J2	M1	380
V _{CCINT}	-	P28	V _{CCINT} *	V _{CCINT} *	-
I/O	6	-	-	M6	389
I/O	6	P29	H1	M3	392
I/O	6	-	J4	M4	395
I/O	6	-	-	N1	398
I/O	6	P30	J1	M5	404
I/O, V _{REF}	6	P31	J3	N2	407
V _{CCO}	6	-	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	410
I/O	6	P34	K2	N4	413
I/O	6	-	-	P1	416
I/O	6	-	-	N5	419
I/O	6	P35	K1	P2	422
GND	-	-	GND*	GND*	-
I/O	6	-	K3	P4	425
I/O	6	-	-	R1	428
I/O	6	-	-	P5	431
I/O	6	P36	L1	P3	434
I/O	6	P37	L2	R2	437
V _{CCINT}	-	P38	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	6	P39	V _{CCO} Bank 6*	V _{CCO} Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	440
I/O, V _{REF}	6	P42	M1	R4	443

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V _{CCO}	3	P117	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{CCINT}	-	P118	V _{CCINT} *	V _{CCINT} *	-
I/O (D5)	3	P119	M16	R21	833
I/O	3	P120	K14	P18	836
I/O	3	-	-	R22	839
I/O	3	-	-	P19	842
I/O	3	-	L16	P20	845
GND	-	-	GND*	GND*	-
I/O	3	P121	K13	P21	848
I/O	3	-	-	N19	851
I/O	3	-	-	P22	854
I/O	3	P122	L15	N18	857
I/O	3	P123	K12	N20	860
GND	-	P124	GND*	GND*	-
V _{CCO}	3	-	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
I/O, V _{REF}	3	P125	K16	N21	863
I/O (D4)	3	P126	J16	N22	866
I/O	3	-	-	M17	872
I/O	3	-	J14	M19	875
I/O	3	P127	K15	M20	878
I/O	3	-	-	M18	881
V _{CCINT}	-	P128	V _{CCINT} *	V _{CCINT} *	-
I/O, TRDY ⁽¹⁾	3	P129	J15	M22	890
V _{CCO}	3	P130	V _{CCO} Bank 3*	V _{CCO} Bank 3*	-
V _{CCO}	2	P130	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P131	GND*	GND*	-
I/O, IRDY ⁽¹⁾	2	P132	H16	L20	893
I/O	2	P133	H14	L17	896
I/O	2	-	-	L18	902
I/O	2	P134	H15	L21	905
I/O	2	-	J13	L22	908
I/O	2	-	-	K19	911
I/O (D3)	2	P135	G16	K20	917
I/O, V _{REF}	2	P136	H13	K21	920
V _{CCO}	2	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P137	GND*	GND*	-
I/O	2	P138	G14	K22	923
I/O	2	P139	G15	J21	926

XC2S200 Device Pinouts (Continued)

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	2	-	-	K18	929
I/O	2	-	-	J20	932
I/O	2	P140	G12	J18	935
GND	-	-	GND*	GND*	-
I/O	2	-	F16	J22	938
I/O	2	-	-	J19	941
I/O	2	-	-	H21	944
I/O	2	P141	G13	H19	947
I/O (D2)	2	P142	F15	H20	950
V _{CCINT}	-	P143	V _{CCINT} *	V _{CCINT} *	-
V _{CCO}	2	P144	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	P145	GND*	GND*	-
I/O (D1)	2	P146	E16	H22	953
I/O, V _{REF}	2	P147	F14	H18	956
I/O	2	-	-	G21	962
I/O	2	P148	D16	G18	965
GND	-	-	GND*	GND*	-
I/O	2	-	F12	G20	968
I/O	2	-	-	G19	971
I/O	2	-	-	F22	974
I/O	2	P149	E15	F19	977
I/O, V _{REF}	2	P150	F13	F21	980
V _{CCO}	2	-	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-
GND	-	-	GND*	GND*	-
I/O	2	P151	E14	F20	983
I/O	2	-	C16	F18	986
GND	-	-	GND*	GND*	-
I/O	2	-	-	E22	989
I/O	2	-	-	E21	995
I/O, V _{REF}	2	P152	E13	D22	998
GND	-	-	GND*	GND*	-
I/O	2	-	B16	E20	1001
I/O	2	-	-	D21	1004
I/O	2	-	-	C22	1007
I/O (DIN, D0)	2	P153	D14	D20	1013
I/O (DOUT, BUSY)	2	P154	C15	C21	1016
CCLK	2	P155	D15	B22	1019
V _{CCO}	2	P156	V _{CCO} Bank 2*	V _{CCO} Bank 2*	-