# AMD Xilinx - XC2S30-5PQ208C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

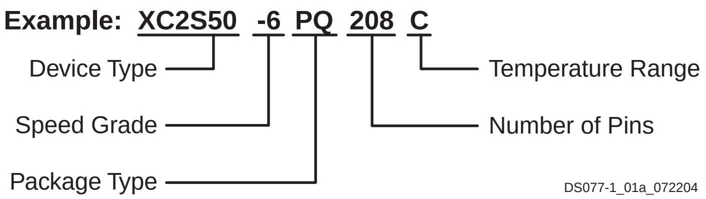
| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 972 |
| Total RAM Bits | 24576 |
| Number of I/O | 140 |
| Number of Gates | 30000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s30-5pq208c |

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

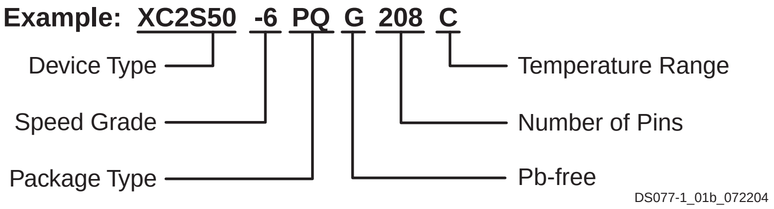
## Ordering Information

Spartan-II devices are available in both standard and Pb-free packaging options for all device/package combinations. The Pb-free packages include a special "G" character in the ordering code.

### *Standard Packaging*



### *Pb-Free Packaging*



## Device Ordering Options

| Device |
|---|
| XC2S15 |
| XC2S30 |
| XC2S50 |
| XC2S100 |
| XC2S150 |
| XC2S200 |

| Speed Grade | |
|---|---|
| -5 | Standard Performance |
| -6 | Higher Performance[1] |

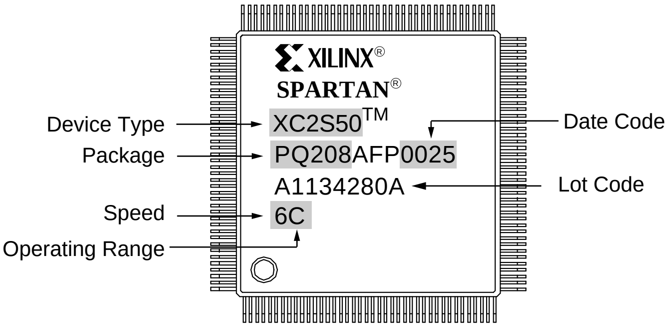
| Number of Pins / Package Type | |
|---|---|
| VQ(G)100 | 100-pin Plastic Very Thin QFP |
| CS(G)144 | 144-ball Chip-Scale BGA |
| TQ(G)144 | 144-pin Plastic Thin QFP |
| PQ(G)208 | 208-pin Plastic QFP |
| FG(G)256 | 256-ball Fine Pitch BGA |
| FG(G)456 | 456-ball Fine Pitch BGA |

| Temperature Range ($T_J$) | |
|---|---|
| C = Commercial | 0°C to +85°C |
| I = Industrial | –40°C to +100°C |

**Notes:**

1. The -6 speed grade is exclusively available in the Commercial temperature range.

## Device Part Marking



Sample package with part marking for XC2S50-6PQ208C.

ds001-1_02_090303

# Spartan-II FPGA Family: Functional Description

DS001-2 (v2.8) June 13, 2008

**Product Specification**

## Architectural Description

### Spartan-II FPGA Array

The Spartan®-II field-programmable gate array, shown in Figure 2, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versatile multi-level interconnect structure

As can be seen in Figure 2, the CLBs form the central logic structure with easy access to all support and routing structures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be discussed in detail in the following sections.

### Input/Output Block

The Spartan-II FPGA IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signaling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and bus interfaces. Table 3 lists several of the standards which are supported along with the required reference, output and termination voltages needed to meet the standard.

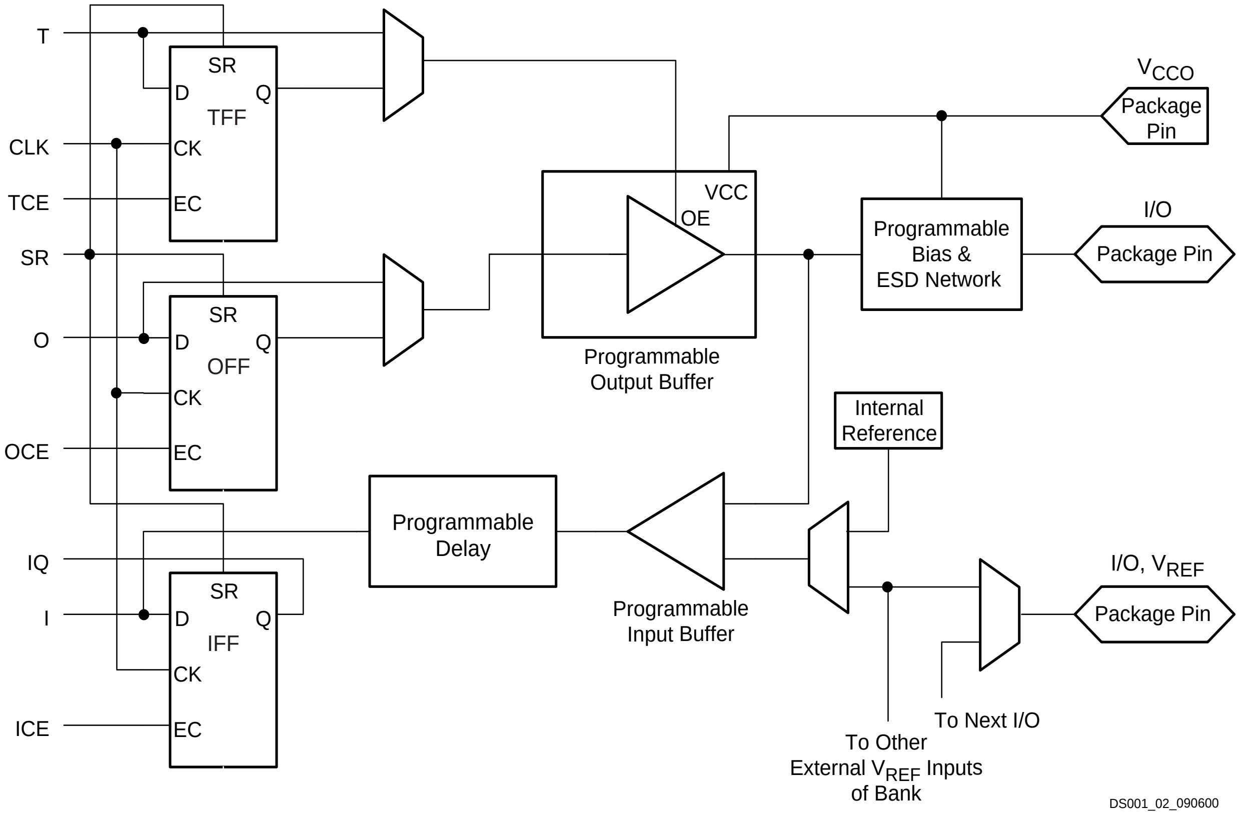


*Figure 2:* **Spartan-II FPGA Input/Output Block (IOB)**

## Configuration

Configuration is the process by which the bitstream of a design, as generated by the Xilinx software, is loaded into the internal configuration memory of the FPGA. Spartan-II devices support both serial configuration, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

### Configuration File

Spartan-II devices are configured by sequentially loading frames of data that have been concatenated into a configuration file. Table 8 shows how much nonvolatile storage space is needed for Spartan-II devices.

It is important to note that, while a PROM is commonly used to store configuration data before loading them into the FPGA, it is by no means required. Any of a number of different kinds of under populated nonvolatile storage already available either on or off the board (i.e., hard drives, FLASH cards, etc.) can be used. For more information on configuration without a PROM, refer to XAPP098, *The Low-Cost, Efficient Serial Configuration of Spartan FPGAs*.

*Table 8:* **Spartan-II Configuration File Size**

| Device | Configuration File Size (Bits) |
|---|---|
| XC2S15 | 197,696 |
| XC2S30 | 336,768 |
| XC2S50 | 559,200 |
| XC2S100 | 781,216 |
| XC2S150 | 1,040,096 |
| XC2S200 | 1,335,840 |

### Modes

Spartan-II devices support the following four configuration modes:

- Slave Serial mode
- Master Serial mode
- Slave Parallel mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to the end of configuration. The selection codes are listed in Table 9.

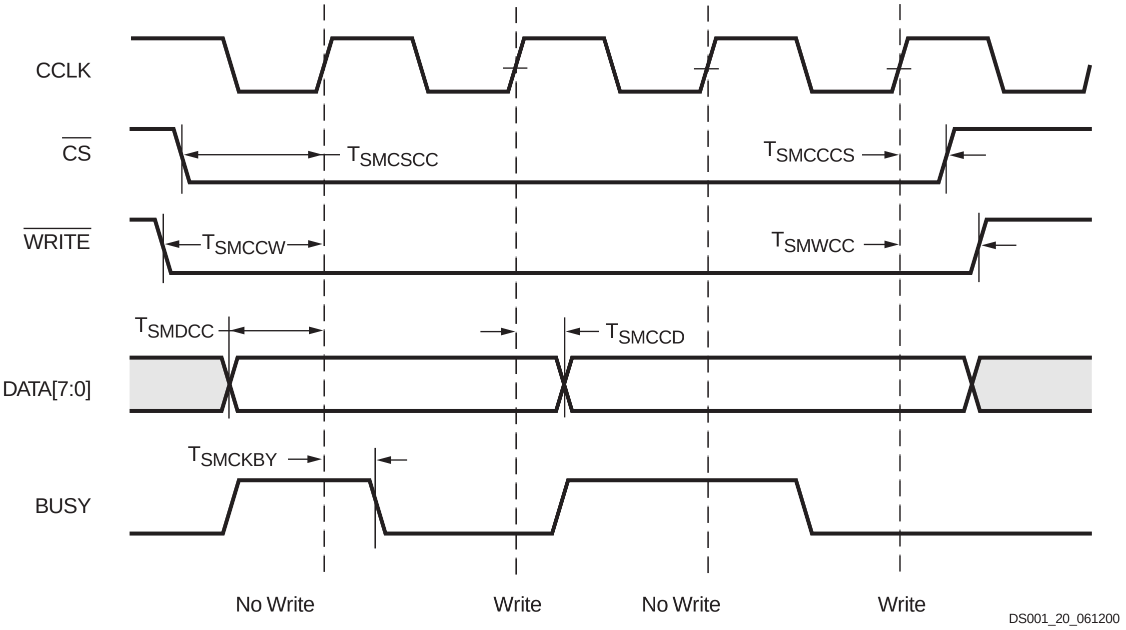
Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

*Table 9:* **Configuration Modes**

| Configuration Mode | Preconfiguration Pull-ups | M0 | M1 | M2 | CCLK Direction | Data Width | Serial $D_{OUT}$ |
|---|---|---|---|---|---|---|---|
| Master Serial mode | No | 0 | 0 | 0 | Out | 1 | Yes |
| | Yes | 0 | 0 | 1 | | | |
| Slave Parallel mode | Yes | 0 | 1 | 0 | In | 8 | No |
| | No | 0 | 1 | 1 | | | |
| Boundary-Scan mode | Yes | 1 | 0 | 0 | N/A | 1 | No |
| | No | 1 | 0 | 1 | | | |
| Slave Serial mode | Yes | 1 | 1 | 0 | In | 1 | Yes |
| | No | 1 | 1 | 1 | | | |

**Notes:**

1. During power-on and throughout configuration, the I/O drivers will be in a high-impedance state. After configuration, all unused I/Os (those not assigned signals) will remain in a high-impedance state. Pins used as outputs may pulse High at the end of configuration (see Answer 10504).
2. If the Mode pins are set for preconfiguration pull-ups, those resistors go into effect once the rising edge of INIT samples the Mode pins. They will stay in effect until GTS is released during startup, after which the UnusedPin bitstream generator option will determine whether the unused I/Os have a pull-up, pull-down, or no resistor.



| Symbol | | Description | | Units |
|---|---|---|---|---|
| $T_{SMDCC}$ | CCLK | D0-D7 setup/hold | 5 | ns, min |
| $T_{SMCCD}$ | | D0-D7 hold | 0 | ns, min |
| $T_{SMCSCC}$ | | $\overline{\text{CS}}$ setup | 7 | ns, min |
| $T_{SMCCCS}$ | | $\overline{\text{CS}}$ hold | 0 | ns, min |
| $T_{SMCCW}$ | | $\overline{\text{WRITE}}$ setup | 7 | ns, min |
| $T_{SMWCC}$ | | $\overline{\text{WRITE}}$ hold | 0 | ns, min |
| $T_{SMCKBY}$ | | BUSY propagation delay | 12 | ns, max |
| $F_{CC}$ | | Maximum frequency | 66 | MHz, max |
| $F_{CCNH}$ | | Maximum frequency with no handshake | 50 | MHz, max |

*Figure 20:* **Slave Parallel Write Timing**

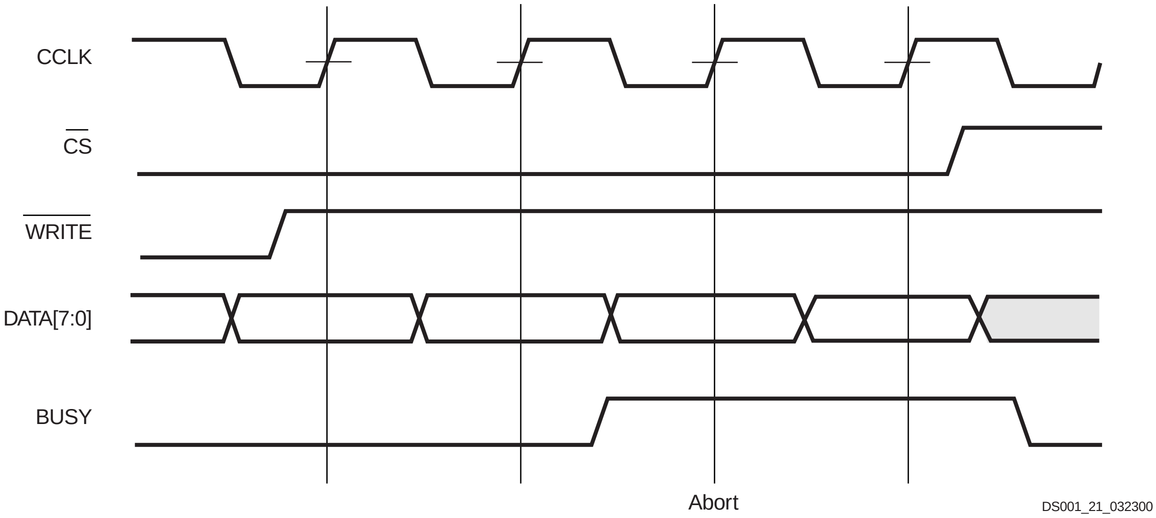


*Figure 21:* **Slave Parallel Write Abort Waveforms**

## Design Considerations

This section contains more detailed design information on the following features:

- Delay-Locked Loop . . . see page 27
- Block RAM . . . see page 32
- Versatile I/O . . . see page 36

## Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

### Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

### Library DLL Primitives

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.

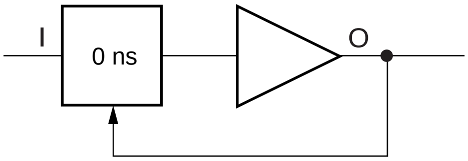


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*Figure 22:* **Simplified DLL Macro BUFGDLL**

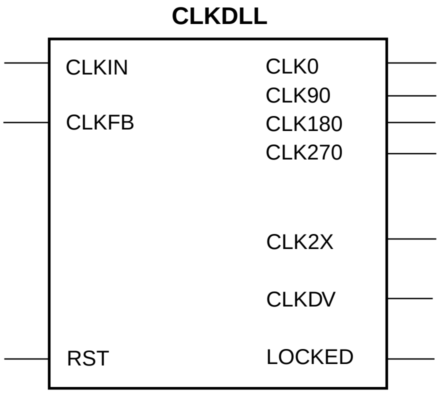

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*Figure 23:* **Standard DLL Primitive CLKDLL**

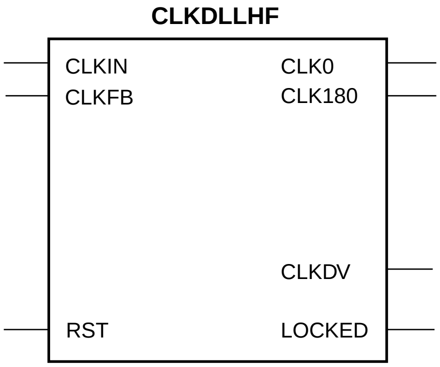

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*Figure 24:* **High-Frequency DLL Primitive CLKDLLHF**

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF primitive names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24). The default is slew rate limited with 12 mA drive.

OBUF placement restrictions require that within a given $V_{CCO}$ bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within any $V_{CCO}$ bank. Table 17 summarizes the output compatibility requirements. The LOC property can specify a location for the OBUF.

*Table 17:* **Output Standards Compatibility Requirements**

| | |
|---|---|
| Rule 1 | Only outputs with standards which share compatible $V_{CCO}$ may be used within the same bank. |
| Rule 2 | There are no placement restrictions for outputs with standards that do not require a $V_{CCO}$. |
| $V_{CCO}$ | Compatible Standards |
| 3.3 | LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3 |
| 2.5 | SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+ |
| 1.5 | HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+ |

### *OBUFT*

The generic 3-state output buffer OBUFT, shown in Figure 39, typically implements 3-state outputs or bidirectional I/O.

With no extension or property specified for the generic OBUFT primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT primitive names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

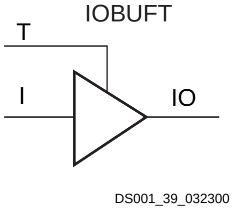

*Figure 39:* **3-State Output Buffer Primitive (OBUFT**

The Versatile I/O OBUFT placement restrictions require that within a given $V_{CCO}$ bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a $V_{REF}$ have automatic placement of a $V_{REF}$ in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding $V_{REF}$) are explicitly placed.

The LOC property can specify a location for the OBUFT.

### *IOBUF*

Use the IOBUF primitive for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 40.

With no extension or property specified for the generic IOBUF primitive, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF primitive names is as follows:

property. This property could have one of the following seven values.

DRIVE=2

DRIVE=4

DRIVE=6

DRIVE=8

DRIVE=12 (Default)

DRIVE=16

DRIVE=24

## Design Considerations

### Reference Voltage ($V_{REF}$) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage ($V_{REF}$). Provide the $V_{REF}$ as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 36, page 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input.

Within each $V_{REF}$ bank, any input buffers that require a $V_{REF}$ signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same $V_{REF}$ bank.

### Output Drive Source Voltage ($V_{CCO}$) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage ($V_{CCO}$). As a result each device can often have to support multiple output drive source voltages.

The $V_{CCO}$ supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined $V_{CCO}$ supply. The TQ144 and the CS144 packages provide four independent $V_{CCO}$ supplies. The FG256 and the FG456 provide eight independent $V_{CCO}$ supplies.

Output buffers within a given $V_{CCO}$ bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the $V_{CCO}$ voltage for Input $V_{CCO}$ voltage.

### Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

### Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques:

None
Series
Parallel (Shunt)
Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None
Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 41.

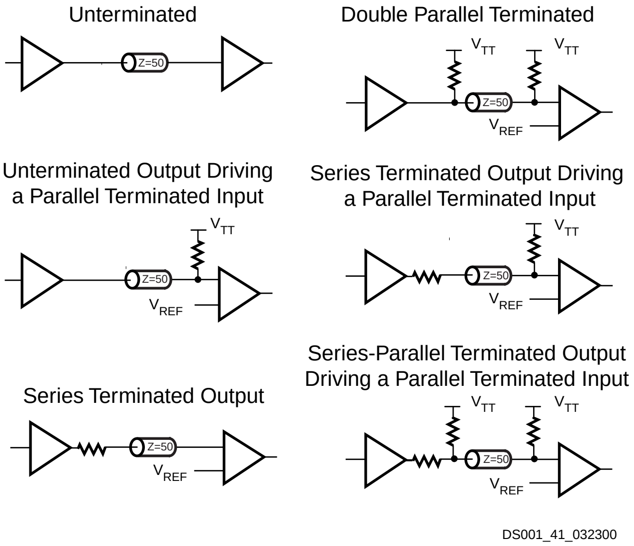

*Figure 41:* **Overview of Standard Input and Output Termination Methods**

### Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

### SSTL3 Class I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 47. DC voltage specifications appear in Table 25 for the SSTL3_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

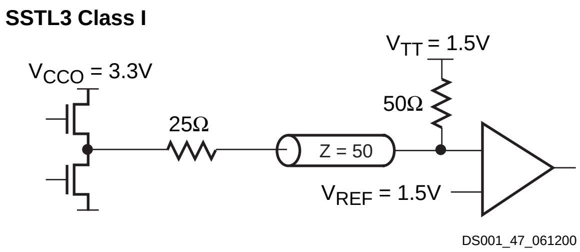

*Figure 47:* **Terminated SSTL3 Class I**

*Table 25:* **SSTL3_I Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = 0.45 \times V_{CCO}$ | 1.3 | 1.5 | 1.7 |
| $V_{TT} = V_{REF}$ | 1.3 | 1.5 | 1.7 |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.5 | 1.7 | $3.9^{(1)}$ |
| $V_{IL} \leq V_{REF} - 0.2$ | $-0.3^{(2)}$ | 1.3 | 1.5 |
| $V_{OH} \geq V_{REF} + 0.6$ | 1.9 | - | - |
| $V_{OL} \leq V_{REF} - 0.6$ | - | - | 1.1 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

**Notes:**

1. $V_{IH}$ maximum is $V_{CCO} + 0.3$.
2. $V_{IL}$ minimum does not conform to the formula.

### SSTL3 Class II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 48. DC voltage specifications appear in Table 26 for the SSTL3_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

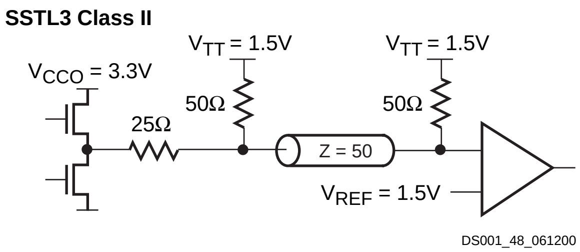

*Figure 48:* **Terminated SSTL3 Class II**

*Table 26:* **SSTL3_II Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = 0.45 \times V_{CCO}$ | 1.3 | 1.5 | 1.7 |
| $V_{TT} = V_{REF}$ | 1.3 | 1.5 | 1.7 |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.5 | 1.7 | $3.9^{(1)}$ |
| $V_{IL} \leq V_{REF} - 0.2$ | $-0.3^{(2)}$ | 1.3 | 1.5 |
| $V_{OH} \geq V_{REF} + 0.8$ | 2.1 | - | - |
| $V_{OL} \leq V_{REF} - 0.8$ | - | - | 0.9 |
| $I_{OH}$ at $V_{OH}$ (mA) | –16 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 16 | - | - |

**Notes:**

1. $V_{IH}$ maximum is $V_{CCO} + 0.3$
2. $V_{IL}$ minimum does not conform to the formula

### LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 32 for the LVTTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 32:* **LVTTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 2.0 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.8 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –24 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 | - | - |

**Notes:**
1. $V_{OL}$ and $V_{OH}$ for lower drive currents sample tested.

### LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 33 for the LVCMOS2 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 33:* **LVCMOS2 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.7 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.7 |
| $V_{OH}$ | 1.9 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –12 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 12 | - | - |

### AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 34 for the AGP-2X standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 34:* **AGP-2X Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = N \times V_{CCO}^{(1)}$ | 1.17 | 1.32 | 1.48 |
| $V_{TT}$ | - | - | - |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.37 | 1.52 | - |
| $V_{IL} \leq V_{REF} - 0.2$ | - | 1.12 | 1.28 |
| $V_{OH} \geq 0.9 \times V_{CCO}$ | 2.7 | 3.0 | - |
| $V_{OL} \leq 0.1 \times V_{CCO}$ | - | 0.33 | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 2 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 2 | - | - |

**Notes:**
1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

For design examples and more information on using the I/O, see XAPP179, *Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs*.

| Input/Output Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA | mA |
| CTT | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | $V_{REF}$ – 0.4 | $V_{REF}$ + 0.4 | 8 | –8 |
| AGP | –0.5 | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | 3.6 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | Note (2) | Note (2) |

**Notes:**

1. $V_{OL}$ and $V_{OH}$ for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

## Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

### Global Clock Input to Output Delay for LVTTL, *with* DLL (Pin-to-Pin)(1)

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | All | -6 | -5 | |
| | | | Min | Max | Max | |
| $T_{ICKOFDLL}$ | Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *with* DLL. | All | | 2.9 | 3.3 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

### Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)(1)

| Symbol | Description | Device | Speed Grade | | | Units |
|---|---|---|---|---|---|---|
| | | | All | -6 | -5 | |
| | | | Min | Max | Max | |
| $T_{ICKOF}$ | Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *without* DLL. | XC2S15 | | 4.5 | 5.4 | ns |
| | | XC2S30 | | 4.5 | 5.4 | ns |
| | | XC2S50 | | 4.5 | 5.4 | ns |
| | | XC2S100 | | 4.6 | 5.5 | ns |
| | | XC2S150 | | 4.6 | 5.5 | ns |
| | | XC2S200 | | 4.7 | 5.6 | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

## Calculation of $T_{IOOP}$ as a Function of Capacitance

$T_{IOOP}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{IOOP}$ are based on the standard capacitive load ($C_{SL}$) for each I/O standard as listed in the table "Constants for Calculating TIOOP", below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, $T_{IOOP1}$.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

| | |
|---|---|
| Adj | is selected from "IOB Output Delay Adjustments for Different Standards", page 59, according to the I/O standard used |
| $C_{LOAD}$ | is the capacitive load for the design |
| $F_L$ | is the capacitance scaling factor |

## Delay Measurement Methodology

| Standard | $V_L$ (1) | $V_H$ (1) | Meas. Point | $V_{REF}$ Typ (2) |
|---|---|---|---|---|
| LVTTL | 0 | 3 | 1.4 | - |
| LVCMOS2 | 0 | 2.5 | 1.125 | - |
| PCI33_5 | Per PCI Spec | | | - |
| PCI33_3 | Per PCI Spec | | | - |
| PCI66_3 | Per PCI Spec | | | - |
| GTL | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | $V_{REF}$ | 0.80 |
| GTL+ | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | $V_{REF}$ | 1.0 |
| HSTL Class I | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.75 |
| HSTL Class III | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.90 |
| HSTL Class IV | $V_{REF} - 0.5$ | $V_{REF} + 0.5$ | $V_{REF}$ | 0.90 |
| SSTL3 I and II | $V_{REF} - 1.0$ | $V_{REF} + 1.0$ | $V_{REF}$ | 1.5 |
| SSTL2 I and II | $V_{REF} - 0.75$ | $V_{REF} + 0.75$ | $V_{REF}$ | 1.25 |
| CTT | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | $V_{REF}$ | 1.5 |
| AGP | $V_{REF} -$ $(0.2 \times V_{CCO})$ | $V_{REF} +$ $(0.2 \times V_{CCO})$ | $V_{REF}$ | Per AGP Spec |

**Notes:**
1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at $V_{REF}$ Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the table, "Constants for Calculating TIOOP". See Xilinx application note XAPP179 for the appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## Constants for Calculating $T_{IOOP}$

| Standard | $C_{SL}$ (1) (pF) | $F_L$ (ns/pF) |
|---|---|---|
| LVTTL Fast Slew Rate, 2 mA drive | 35 | 0.41 |
| LVTTL Fast Slew Rate, 4 mA drive | 35 | 0.20 |
| LVTTL Fast Slew Rate, 6 mA drive | 35 | 0.13 |
| LVTTL Fast Slew Rate, 8 mA drive | 35 | 0.079 |
| LVTTL Fast Slew Rate, 12 mA drive | 35 | 0.044 |
| LVTTL Fast Slew Rate, 16 mA drive | 35 | 0.043 |
| LVTTL Fast Slew Rate, 24 mA drive | 35 | 0.033 |
| LVTTL Slow Slew Rate, 2 mA drive | 35 | 0.41 |
| LVTTL Slow Slew Rate, 4 mA drive | 35 | 0.20 |
| LVTTL Slow Slew Rate, 6 mA drive | 35 | 0.100 |
| LVTTL Slow Slew Rate, 8 mA drive | 35 | 0.086 |
| LVTTL Slow Slew Rate, 12 mA drive | 35 | 0.058 |
| LVTTL Slow Slew Rate, 16 mA drive | 35 | 0.050 |
| LVTTL Slow Slew Rate, 24 mA drive | 35 | 0.048 |
| LVCMOS2 | 35 | 0.041 |
| PCI 33 MHz 5V | 50 | 0.050 |
| PCI 33 MHZ 3.3V | 10 | 0.050 |
| PCI 66 MHz 3.3V | 10 | 0.033 |
| GTL | 0 | 0.014 |
| GTL+ | 0 | 0.017 |
| HSTL Class I | 20 | 0.022 |
| HSTL Class III | 20 | 0.016 |
| HSTL Class IV | 20 | 0.014 |
| SSTL2 Class I | 30 | 0.028 |
| SSTL2 Class II | 30 | 0.016 |
| SSTL3 Class I | 30 | 0.029 |
| SSTL3 Class II | 30 | 0.016 |
| CTT | 20 | 0.035 |
| AGP | 10 | 0.037 |

**Notes:**
1. I/O parameter measurements are made with the capacitance values shown above. See Xilinx application note XAPP179 for the appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## CLB Distributed RAM Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{SHCKO16}$ | Clock CLK to X/Y outputs (WE active, 16 x 1 mode) | - | 2.2 | - | 2.6 | ns |
| $T_{SHCKO32}$ | Clock CLK to X/Y outputs (WE active, 32 x 1 mode) | - | 2.5 | - | 3.0 | ns |
| **Setup/Hold Times with Respect to Clock CLK**(1) | | | | | | |
| $T_{AS}$ / $T_{AH}$ | F/G address inputs | 0.7 / 0 | - | 0.7 / 0 | - | ns |
| $T_{DS}$ / $T_{DH}$ | BX/BY data inputs (DIN) | 0.8 / 0 | - | 0.9 / 0 | - | ns |
| $T_{WS}$ / $T_{WH}$ | CE input (WS) | 0.9 / 0 | - | 1.0 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{WPH}$ | Minimum pulse width, High | - | 2.9 | - | 2.9 | ns |
| $T_{WPL}$ | Minimum pulse width, Low | - | 2.9 | - | 2.9 | ns |
| $T_{WC}$ | Minimum clock period to meet address write cycle time | - | 5.8 | - | 5.8 | ns |

**Notes:**
1. A zero hold time listing indicates no hold time or a negative hold time.

## CLB Shift Register Switching Characteristics

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Sequential Delays** | | | | | | |
| $T_{REG}$ | Clock CLK to X/Y outputs | - | 3.47 | - | 3.88 | ns |
| **Setup Times with Respect to Clock CLK** | | | | | | |
| $T_{SHDICK}$ | BX/BY data inputs (DIN) | 0.8 | - | 0.9 | - | ns |
| $T_{SHCECK}$ | CE input (WS) | 0.9 | - | 1.0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{SRPH}$ | Minimum pulse width, High | - | 2.9 | - | 2.9 | ns |
| $T_{SRPL}$ | Minimum pulse width, Low | - | 2.9 | - | 2.9 | ns |

## Block RAM Switching Characteristics

| Symbol | Description | Speed Grade -6 Min | -6 Max | -5 Min | -5 Max | Units |
|---|---|---|---|---|---|---|
| **Sequential Delays** | | | | | | |
| $T_{BCKO}$ | Clock CLK to DOUT output | - | 3.4 | - | 4.0 | ns |
| **Setup/Hold Times with Respect to Clock CLK**(1) | | | | | | |
| $T_{BACK}$ / $T_{BCKA}$ | ADDR inputs | 1.4 / 0 | - | 1.4 / 0 | - | ns |
| $T_{BDCK}$/ $T_{BCKD}$ | DIN inputs | 1.4 / 0 | - | 1.4 / 0 | - | ns |
| $T_{BECK}$/ $T_{BCKE}$ | EN inputs | 2.9 / 0 | - | 3.2 / 0 | - | ns |
| $T_{BRCK}$/ $T_{BCKR}$ | RST input | 2.7 / 0 | - | 2.9 / 0 | - | ns |
| $T_{BWCK}$/ $T_{BCKW}$ | WEN input | 2.6 / 0 | - | 2.8 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{BPWH}$ | Minimum pulse width, High | - | 1.9 | - | 1.9 | ns |
| $T_{BPWL}$ | Minimum pulse width, Low | - | 1.9 | - | 1.9 | ns |
| $T_{BCCS}$ | CLKA -> CLKB setup time for different ports | - | 3.0 | - | 4.0 | ns |

**Notes:**
1. A zero hold time listing indicates no hold time or a negative hold time.

## TBUF Switching Characteristics

| Symbol | Description | Speed Grade -6 Max | -5 Max | Units |
|---|---|---|---|---|
| **Combinatorial Delays** | | | | |
| $T_{IO}$ | IN input to OUT output | 0 | 0 | ns |
| $T_{OFF}$ | TRI input to OUT output high impedance | 0.1 | 0.2 | ns |
| $T_{ON}$ | TRI input to valid data on OUT output | 0.1 | 0.2 | ns |

## JTAG Test Access Port Switching Characteristics

| Symbol | Description | Speed Grade -6 Min | -6 Max | -5 Min | -5 Max | Units |
|---|---|---|---|---|---|---|
| **Setup and Hold Times with Respect to TCK** | | | | | | |
| $T_{TAPTCK}$ / $T_{TCKTAP}$ | TMS and TDI setup and hold times | 4.0 / 2.0 | - | 4.0 / 2.0 | - | ns |
| **Sequential Delays** | | | | | | |
| $T_{TCKTDO}$ | Output delay from clock TCK to output TDO | - | 11.0 | - | 11.0 | ns |
| FTCK | Maximum TCK clock frequency | - | 33 | - | 33 | MHz |

## XC2S15 Device Pinouts *(Continued)*

| XC2S15 Pad Name | | | | | |
|---|---|---|---|---|---|
| **Function** | **Bank** | **VQ100** | **TQ144** | **CS144** | **Bndry Scan** |
| GND | - | - | P61 | J12 | - |
| I/O (D5) | 3 | P57 | P60 | J13 | 245 |
| I/O | 3 | P58 | P59 | H10 | 248 |
| I/O, $V_{REF}$ | 3 | P59 | P58 | H11 | 251 |
| I/O (D4) | 3 | P60 | P57 | H12 | 254 |
| I/O | 3 | - | P56 | H13 | 257 |
| $V_{CCINT}$ | - | P61 | P55 | G12 | - |
| I/O, TRDY(1) | 3 | P62 | P54 | G13 | 260 |
| $V_{CCO}$ | 3 | P63 | P53 | G11 | - |
| $V_{CCO}$ | 2 | P63 | P53 | G11 | - |
| GND | - | P64 | P52 | G10 | - |
| I/O, IRDY(1) | 2 | P65 | P51 | F13 | 263 |
| I/O | 2 | - | P50 | F12 | 266 |
| I/O (D3) | 2 | P66 | P49 | F11 | 269 |
| I/O, $V_{REF}$ | 2 | P67 | P48 | F10 | 272 |
| I/O | 2 | P68 | P47 | E13 | 275 |
| I/O (D2) | 2 | P69 | P46 | E12 | 278 |
| GND | - | - | P45 | E11 | - |
| I/O (D1) | 2 | P70 | P44 | E10 | 281 |
| I/O | 2 | P71 | P43 | D13 | 284 |
| I/O, $V_{REF}$ | 2 | P72 | P41 | D11 | 287 |
| I/O | 2 | - | P40 | C13 | 290 |
| I/O (DIN, D0) | 2 | P73 | P39 | C12 | 293 |
| I/O (DOUT, BUSY) | 2 | P74 | P38 | C11 | 296 |
| CCLK | 2 | P75 | P37 | B13 | 299 |
| $V_{CCO}$ | 2 | P76 | P36 | B12 | - |
| $V_{CCO}$ | 1 | P76 | P35 | A13 | - |
| TDO | 2 | P77 | P34 | A12 | - |
| GND | - | P78 | P33 | B11 | - |
| TDI | - | P79 | P32 | A11 | - |
| I/O ($\overline{CS}$) | 1 | P80 | P31 | D10 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P81 | P30 | C10 | 3 |
| I/O | 1 | - | P29 | B10 | 6 |
| I/O, $V_{REF}$ | 1 | P82 | P28 | A10 | 9 |
| I/O | 1 | P83 | P27 | D9 | 12 |
| I/O | 1 | P84 | P26 | C9 | 15 |
| GND | - | - | P25 | B9 | - |
| $V_{CCINT}$ | - | P85 | P24 | A9 | - |
| I/O | 1 | - | P23 | D8 | 18 |
| I/O | 1 | - | P22 | C8 | 21 |

## XC2S15 Device Pinouts *(Continued)*

| XC2S15 Pad Name | | | | | |
|---|---|---|---|---|---|
| **Function** | **Bank** | **VQ100** | **TQ144** | **CS144** | **Bndry Scan** |
| I/O, $V_{REF}$ | 1 | P86 | P21 | B8 | 24 |
| I/O | 1 | - | P20 | A8 | 27 |
| I/O | 1 | P87 | P19 | B7 | 30 |
| I, GCK2 | 1 | P88 | P18 | A7 | 36 |
| GND | - | P89 | P17 | C7 | - |
| $V_{CCO}$ | 1 | P90 | P16 | D7 | - |
| $V_{CCO}$ | 0 | P90 | P16 | D7 | - |
| I, GCK3 | 0 | P91 | P15 | A6 | 37 |
| $V_{CCINT}$ | - | P92 | P14 | B6 | - |
| I/O | 0 | - | P13 | C6 | 44 |
| I/O, $V_{REF}$ | 0 | P93 | P12 | D6 | 47 |
| I/O | 0 | - | P11 | A5 | 50 |
| I/O | 0 | - | P10 | B5 | 53 |
| $V_{CCINT}$ | - | P94 | P9 | C5 | - |
| GND | - | - | P8 | D5 | - |
| I/O | 0 | P95 | P7 | A4 | 56 |
| I/O | 0 | P96 | P6 | B4 | 59 |
| I/O, $V_{REF}$ | 0 | P97 | P5 | C4 | 62 |
| I/O | 0 | - | P4 | A3 | 65 |
| I/O | 0 | P98 | P3 | B3 | 68 |
| TCK | - | P99 | P2 | C3 | - |
| $V_{CCO}$ | 0 | P100 | P1 | A2 | - |
| $V_{CCO}$ | 7 | P100 | P144 | B2 | - |

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**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S15 Package Pins

**VQ100**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P28 | P29 | - | - | - | - |

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**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P42 | P64 | P78 | P101 | P104 | P105 |
| P116 | P138 | - | - | - | - |

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**CS144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| D3 | D12 | J4 | K13 | M3 | M4 |
| M10 | N3 | - | - | - | - |

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## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | TQ144 | PQ208 | FG256 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 3 | - | - | J14 | 503 |
| I/O | 3 | P56 | P127 | K15 | 506 |
| $V_{CCINT}$ | - | P55 | P128 | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P54 | P129 | J15 | 512 |
| $V_{CCO}$ | 3 | P53 | P130 | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P53 | P130 | $V_{CCO}$ Bank 2* | - |
| GND | - | P52 | P131 | GND* | - |
| I/O, IRDY(1) | 2 | P51 | P132 | H16 | 515 |
| I/O | 2 | - | P133 | H14 | 518 |
| I/O | 2 | P50 | P134 | H15 | 521 |
| I/O | 2 | - | - | J13 | 524 |
| I/O (D3) | 2 | P49 | P135 | G16 | 527 |
| I/O, $V_{REF}$ | 2 | P48 | P136 | H13 | 530 |
| GND | - | - | P137 | GND* | - |
| I/O | 2 | - | P138 | G14 | 533 |
| I/O | 2 | - | P139 | G15 | 536 |
| I/O | 2 | - | P140 | G12 | 539 |
| I/O | 2 | - | - | F16 | 542 |
| I/O | 2 | P47 | P141 | G13 | 545 |
| I/O (D2) | 2 | P46 | P142 | F15 | 548 |
| $V_{CCINT}$ | - | - | P143 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | - | P144 | $V_{CCO}$ Bank 2* | - |
| GND | - | P45 | P145 | GND* | - |
| I/O (D1) | 2 | P44 | P146 | E16 | 551 |
| I/O | 2 | P43 | P147 | F14 | 554 |
| I/O | 2 | P42 | P148 | D16 | 557 |
| I/O | 2 | - | - | F12 | 560 |
| I/O | 2 | - | P149 | E15 | 563 |
| I/O, $V_{REF}$ | 2 | P41 | P150 | F13 | 566 |
| GND | - | - | - | GND* | - |
| I/O | 2 | - | P151 | E14 | 569 |
| I/O | 2 | - | - | C16 | 572 |
| I/O | 2 | P40 | P152 | E13 | 575 |
| I/O | 2 | - | - | B16 | 578 |
| I/O (DIN, D0) | 2 | P39 | P153 | D14 | 581 |
| I/O (DOUT, BUSY) | 2 | P38 | P154 | C15 | 584 |
| CCLK | 2 | P37 | P155 | D15 | 587 |
| $V_{CCO}$ | 2 | P36 | P156 | $V_{CCO}$ Bank 2* | - |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | TQ144 | PQ208 | FG256 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| $V_{CCO}$ | 1 | P35 | P156 | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P34 | P157 | B14 | - |
| GND | - | P33 | P158 | GND* | - |
| TDI | - | P32 | P159 | A15 | - |
| I/O ($\overline{CS}$) | 1 | P31 | P160 | B13 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P30 | P161 | C13 | 3 |
| I/O | 1 | - | - | C12 | 6 |
| I/O | 1 | P29 | P162 | A14 | 9 |
| I/O | 1 | - | - | D12 | 12 |
| I/O | 1 | - | P163 | B12 | 15 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 1 | P28 | P164 | C11 | 18 |
| I/O | 1 | - | P165 | A13 | 21 |
| I/O | 1 | - | - | D11 | 24 |
| I/O | 1 | - | P166 | A12 | 27 |
| I/O | 1 | P27 | P167 | E11 | 30 |
| I/O | 1 | P26 | P168 | B11 | 33 |
| GND | - | P25 | P169 | GND* | - |
| $V_{CCO}$ | 1 | - | P170 | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P24 | P171 | $V_{CCINT}$* | - |
| I/O | 1 | P23 | P172 | A11 | 36 |
| I/O | 1 | P22 | P173 | C10 | 39 |
| I/O | 1 | - | P174 | B10 | 45 |
| I/O | 1 | - | P175 | D10 | 48 |
| I/O | 1 | - | P176 | A10 | 51 |
| GND | - | - | P177 | GND* | - |
| I/O, $V_{REF}$ | 1 | P21 | P178 | B9 | 54 |
| I/O | 1 | - | P179 | E10 | 57 |
| I/O | 1 | - | - | A9 | 60 |
| I/O | 1 | P20 | P180 | D9 | 63 |
| I/O | 1 | P19 | P181 | A8 | 66 |
| I, GCK2 | 1 | P18 | P182 | C9 | 72 |
| GND | - | P17 | P183 | GND* | - |
| $V_{CCO}$ | 1 | P16 | P184 | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P16 | P184 | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P15 | P185 | B8 | 73 |
| $V_{CCINT}$ | - | P14 | P186 | $V_{CCINT}$* | - |
| I/O | 0 | P13 | P187 | A7 | 80 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| **Function** | **Bank** | | | | | |
| I/O, $V_{REF}$ | 4 | P79 | P95 | T11 | AB16 | 502 |
| I/O | 4 | - | - | - | AB17 | 505 |
| I/O | 4 | P78 | P96 | N11 | V15 | 508 |
| I/O | 4 | - | - | R12 | Y16 | 511 |
| I/O | 4 | - | P97 | P11 | AB18 | 517 |
| I/O, $V_{REF}$ | 4 | P77 | P98 | T12 | AB19 | 520 |
| $V_{CCO}$ | 4 | - | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 4 | - | P99 | T13 | Y17 | 523 |
| I/O | 4 | - | - | N12 | V16 | 526 |
| I/O | 4 | - | - | - | W17 | 529 |
| I/O | 4 | P76 | P100 | R13 | AB20 | 532 |
| I/O | 4 | - | - | P12 | AA19 | 535 |
| I/O | 4 | P75 | P101 | P13 | AA20 | 541 |
| I/O | 4 | P74 | P102 | T14 | W18 | 544 |
| GND | - | P73 | P103 | GND* | GND* | - |
| DONE | 3 | P72 | P104 | R14 | Y19 | 547 |
| $V_{CCO}$ | 4 | P71 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P70 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{\text{PROGRAM}}$ | - | P69 | P106 | P15 | W20 | 550 |
| I/O ($\overline{\text{INIT}}$) | 3 | P68 | P107 | N15 | V19 | 551 |
| I/O (D7) | 3 | P67 | P108 | N14 | Y21 | 554 |
| I/O | 3 | - | - | T15 | W21 | 560 |
| I/O | 3 | P66 | P109 | M13 | U20 | 563 |
| I/O | 3 | - | - | - | U19 | 566 |
| I/O | 3 | - | - | R16 | T18 | 569 |
| I/O | 3 | - | P110 | M14 | W22 | 572 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P65 | P111 | L14 | U21 | 575 |
| I/O | 3 | - | P112 | M15 | T20 | 578 |
| I/O | 3 | - | - | L12 | T21 | 584 |
| I/O | 3 | P64 | P113 | P16 | R18 | 587 |
| I/O | 3 | - | - | - | U22 | 590 |
| I/O, $V_{REF}$ | 3 | P63 | P114 | L13 | R19 | 593 |
| I/O (D6) | 3 | P62 | P115 | N16 | T22 | 596 |
| GND | - | P61 | P116 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| **Function** | **Bank** | | | | | |
| $V_{CCO}$ | 3 | - | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P60 | P119 | M16 | R21 | 599 |
| I/O | 3 | P59 | P120 | K14 | P18 | 602 |
| I/O | 3 | - | - | L16 | P20 | 605 |
| I/O | 3 | - | P121 | K13 | P21 | 608 |
| I/O | 3 | - | P122 | L15 | N18 | 614 |
| I/O | 3 | - | P123 | K12 | N20 | 617 |
| GND | - | - | P124 | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P58 | P125 | K16 | N21 | 620 |
| I/O (D4) | 3 | P57 | P126 | J16 | N22 | 623 |
| I/O | 3 | - | - | J14 | M19 | 626 |
| I/O | 3 | P56 | P127 | K15 | M20 | 629 |
| $V_{CCINT}$ | - | P55 | P128 | E5 | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P54 | P129 | J15 | M22 | 638 |
| $V_{CCO}$ | 3 | P53 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P53 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P52 | P131 | GND* | GND* | - |
| I/O, IRDY(1) | 2 | P51 | P132 | H16 | L20 | 641 |
| I/O | 2 | - | P133 | H14 | L17 | 644 |
| I/O | 2 | P50 | P134 | H15 | L21 | 650 |
| I/O | 2 | - | - | J13 | L22 | 653 |
| I/O (D3) | 2 | P49 | P135 | G16 | K20 | 656 |
| I/O, $V_{REF}$ | 2 | P48 | P136 | H13 | K21 | 659 |
| GND | - | - | P137 | GND* | GND* | - |
| I/O | 2 | - | P138 | G14 | K22 | 662 |
| I/O | 2 | - | P139 | G15 | J21 | 665 |
| I/O | 2 | - | P140 | G12 | J18 | 671 |
| I/O | 2 | - | - | F16 | J22 | 674 |
| I/O | 2 | P47 | P141 | G13 | H19 | 677 |
| I/O (D2) | 2 | P46 | P142 | F15 | H20 | 680 |
| $V_{CCINT}$ | - | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | - | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P45 | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P44 | P146 | E16 | H22 | 683 |
| I/O, $V_{REF}$ | 2 | P43 | P147 | F14 | H18 | 686 |
| I/O | 2 | - | - | - | G21 | 689 |
| I/O | 2 | P42 | P148 | D16 | G18 | 692 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| **Function** | **Bank** | **TQ144** | **PQ208** | **FG256** | **FG456** | **Bndry Scan** |
| I/O | 2 | - | - | F12 | G20 | 695 |
| I/O | 2 | - | P149 | E15 | F19 | 701 |
| I/O, $V_{REF}$ | 2 | P41 | P150 | F13 | F21 | 704 |
| $V_{CCO}$ | 2 | - | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 2 | - | P151 | E14 | F20 | 707 |
| I/O | 2 | - | - | C16 | F18 | 710 |
| I/O | 2 | - | - | - | E21 | 713 |
| I/O | 2 | P40 | P152 | E13 | D22 | 716 |
| I/O | 2 | - | - | B16 | E20 | 719 |
| I/O (DIN, D0) | 2 | P39 | P153 | D14 | D20 | 725 |
| I/O (DOUT, BUSY) | 2 | P38 | P154 | C15 | C21 | 728 |
| CCLK | 2 | P37 | P155 | D15 | B22 | 731 |
| $V_{CCO}$ | 2 | P36 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| $V_{CCO}$ | 1 | P35 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P34 | P157 | B14 | A21 | - |
| GND | - | P33 | P158 | GND* | GND* | - |
| TDI | - | P32 | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P31 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P30 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | C12 | D17 | 9 |
| I/O | 1 | P29 | P162 | A14 | A19 | 12 |
| I/O | 1 | - | - | - | B18 | 15 |
| I/O | 1 | - | - | D12 | C17 | 18 |
| I/O | 1 | - | P163 | B12 | D16 | 21 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P28 | P164 | C11 | A18 | 24 |
| I/O | 1 | - | P165 | A13 | B17 | 27 |
| I/O | 1 | - | - | D11 | D15 | 33 |
| I/O | 1 | - | P166 | A12 | C16 | 36 |
| I/O | 1 | - | - | - | D14 | 39 |
| I/O, $V_{REF}$ | 1 | P27 | P167 | E11 | E14 | 42 |
| I/O | 1 | P26 | P168 | B11 | A16 | 45 |
| GND | - | P25 | P169 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| **Function** | **Bank** | **TQ144** | **PQ208** | **FG256** | **FG456** | **Bndry Scan** |
| $V_{CCO}$ | 1 | - | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P24 | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P23 | P172 | A11 | C15 | 48 |
| I/O | 1 | P22 | P173 | C10 | B15 | 51 |
| I/O | 1 | - | - | - | F12 | 54 |
| I/O | 1 | - | P174 | B10 | C14 | 57 |
| I/O | 1 | - | P175 | D10 | D13 | 63 |
| I/O | 1 | - | P176 | A10 | C13 | 66 |
| GND | - | - | P177 | GND* | GND* | - |
| I/O, $V_{REF}$ | 1 | P21 | P178 | B9 | B13 | 69 |
| I/O | 1 | - | P179 | E10 | E12 | 72 |
| I/O | 1 | - | - | A9 | B12 | 75 |
| I/O | 1 | P20 | P180 | D9 | D12 | 78 |
| I/O | 1 | P19 | P181 | A8 | D11 | 84 |
| I, GCK2 | 1 | P18 | P182 | C9 | A11 | 90 |
| GND | - | P17 | P183 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P16 | P184 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P16 | P184 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P15 | P185 | B8 | C11 | 91 |
| $V_{CCINT}$ | - | P14 | P186 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 0 | P13 | P187 | A7 | A10 | 101 |
| I/O | 0 | - | - | D8 | B10 | 104 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O, IRDY(1) | 2 | P132 | H16 | L20 | 767 |
| I/O | 2 | P133 | H14 | L17 | 770 |
| I/O | 2 | - | - | L18 | 773 |
| I/O | 2 | P134 | H15 | L21 | 776 |
| I/O | 2 | - | J13 | L22 | 779 |
| I/O (D3) | 2 | P135 | G16 | K20 | 782 |
| I/O, $V_{REF}$ | 2 | P136 | H13 | K21 | 785 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P137 | GND* | GND* | - |
| I/O | 2 | P138 | G14 | K22 | 788 |
| I/O | 2 | P139 | G15 | J21 | 791 |
| I/O | 2 | - | - | J20 | 797 |
| I/O | 2 | P140 | G12 | J18 | 800 |
| I/O | 2 | - | F16 | J22 | 803 |
| I/O | 2 | - | - | J19 | 806 |
| I/O | 2 | P141 | G13 | H19 | 812 |
| I/O (D2) | 2 | P142 | F15 | H20 | 815 |
| $V_{CCINT}$ | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P146 | E16 | H22 | 818 |
| I/O, $V_{REF}$ | 2 | P147 | F14 | H18 | 821 |
| I/O | 2 | - | - | G21 | 824 |
| I/O | 2 | P148 | D16 | G18 | 827 |
| I/O | 2 | - | F12 | G20 | 830 |
| I/O | 2 | - | - | G19 | 833 |
| I/O | 2 | - | - | F22 | 836 |
| I/O | 2 | P149 | E15 | F19 | 839 |
| I/O, $V_{REF}$ | 2 | P150 | F13 | F21 | 842 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | P151 | E14 | F20 | 845 |
| I/O | 2 | - | C16 | F18 | 848 |
| I/O | 2 | - | - | E22 | 851 |
| I/O | 2 | - | - | E21 | 854 |
| I/O | 2 | P152 | E13 | D22 | 857 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | B16 | E20 | 860 |
| I/O | 2 | - | - | D21 | 863 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 2 | - | - | C22 | 866 |
| I/O (DIN, D0) | 2 | P153 | D14 | D20 | 869 |
| I/O (DOUT, BUSY) | 2 | P154 | C15 | C21 | 872 |
| CCLK | 2 | P155 | D15 | B22 | 875 |
| $V_{CCO}$ | 2 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| $V_{CCO}$ | 1 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P157 | B14 | A21 | - |
| GND | - | P158 | GND* | GND* | - |
| TDI | - | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | B19 | 6 |
| I/O | 1 | - | - | C18 | 9 |
| I/O | 1 | - | C12 | D17 | 12 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P162 | A14 | A19 | 15 |
| I/O | 1 | - | - | B18 | 18 |
| I/O | 1 | - | - | E16 | 21 |
| I/O | 1 | - | D12 | C17 | 24 |
| I/O | 1 | P163 | B12 | D16 | 27 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P164 | C11 | A18 | 30 |
| I/O | 1 | P165 | A13 | B17 | 33 |
| I/O | 1 | - | - | E15 | 36 |
| I/O | 1 | - | - | A17 | 39 |
| I/O | 1 | - | D11 | D15 | 42 |
| I/O | 1 | P166 | A12 | C16 | 45 |
| I/O | 1 | - | - | D14 | 48 |
| I/O, $V_{REF}$ | 1 | P167 | E11 | E14 | 51 |
| I/O | 1 | P168 | B11 | A16 | 54 |
| GND | - | P169 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P172 | A11 | C15 | 57 |
| I/O | 1 | P173 | C10 | B15 | 60 |
| I/O | 1 | - | - | A15 | 66 |
| I/O | 1 | - | - | F12 | 69 |

## Additional XC2S150 Package Pins

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

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**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

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## Additional XC2S150 Package Pins *(Continued)*

**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| F7 | F8 | F9 | F10 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U7 | U8 | U9 | U10 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A6 | A12 | A13 | A14 | B11 |
| B16 | C2 | C8 | C9 | D1 | D4 |
| D18 | D19 | E13 | E17 | E19 | F11 |
| G2 | G22 | H21 | J1 | J4 | K2 |
| K18 | K19 | L2 | L19 | M2 | M17 |
| M21 | N1 | P1 | P5 | P22 | R3 |
| R20 | R22 | U3 | U18 | V6 | W4 |
| W13 | W15 | W19 | Y5 | Y22 | AA1 |
| AA3 | AA9 | AA10 | AA11 | AA16 | AB7 |
| AB8 | AB12 | AB14 | AB21 | - | - |

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## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| $V_{CCO}$ | 1 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P157 | B14 | A21 | - |
| GND | - | P158 | GND* | GND* | - |
| TDI | - | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | B19 | 9 |
| I/O | 1 | - | - | C18 | 12 |
| I/O | 1 | - | C12 | D17 | 15 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 1 | P162 | A14 | A19 | 18 |
| I/O | 1 | - | - | B18 | 21 |
| I/O | 1 | - | - | E16 | 27 |
| I/O | 1 | - | D12 | C17 | 30 |
| I/O | 1 | P163 | B12 | D16 | 33 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P164 | C11 | A18 | 36 |
| I/O | 1 | P165 | A13 | B17 | 39 |
| I/O | 1 | - | - | E15 | 42 |
| I/O | 1 | - | - | A17 | 45 |
| I/O | 1 | - | D11 | D15 | 48 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P166 | A12 | C16 | 51 |
| I/O | 1 | - | - | D14 | 54 |
| I/O, $V_{REF}$ | 1 | P167 | E11 | E14 | 60 |
| I/O | 1 | P168 | B11 | A16 | 63 |
| GND | - | P169 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P172 | A11 | C15 | 66 |
| I/O | 1 | P173 | C10 | B15 | 69 |
| I/O | 1 | - | - | E13 | 72 |
| I/O | 1 | - | - | A15 | 75 |
| I/O | 1 | - | - | F12 | 78 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P174 | B10 | C14 | 81 |
| I/O | 1 | - | - | B14 | 84 |
| I/O | 1 | - | - | A14 | 87 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 1 | P175 | D10 | D13 | 90 |
| I/O | 1 | P176 | A10 | C13 | 93 |
| GND | - | P177 | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P178 | B9 | B13 | 96 |
| I/O | 1 | P179 | E10 | E12 | 99 |
| I/O | 1 | - | - | A13 | 105 |
| I/O | 1 | - | A9 | B12 | 108 |
| I/O | 1 | P180 | D9 | D12 | 111 |
| I/O | 1 | - | - | C12 | 114 |
| I/O | 1 | P181 | A8 | D11 | 120 |
| I, GCK2 | 1 | P182 | C9 | A11 | 126 |
| GND | - | P183 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P184 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P184 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P185 | B8 | C11 | 127 |
| $V_{CCINT}$ | - | P186 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 0 | - | - | E11 | 137 |
| I/O | 0 | P187 | A7 | A10 | 140 |
| I/O | 0 | - | D8 | B10 | 143 |
| I/O | 0 | - | - | F11 | 146 |
| I/O | 0 | P188 | A6 | C10 | 152 |
| I/O, $V_{REF}$ | 0 | P189 | B7 | A9 | 155 |
| $V_{CCO}$ | 0 | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | P190 | GND* | GND* | - |
| I/O | 0 | P191 | C8 | B9 | 158 |
| I/O | 0 | P192 | D7 | E10 | 161 |
| I/O | 0 | - | - | C9 | 164 |
| I/O | 0 | - | - | D10 | 167 |
| I/O | 0 | P193 | E7 | A8 | 170 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | - | D9 | 173 |
| I/O | 0 | - | - | B8 | 176 |
| I/O | 0 | - | - | C8 | 179 |
| I/O | 0 | P194 | C7 | E9 | 182 |
| I/O | 0 | P195 | B6 | A7 | 185 |
| $V_{CCINT}$ | - | P196 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 0 | P197 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |