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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 972 |
| Total RAM Bits | 24576 |
| Number of I/O | 92 |
| Number of Gates | 30000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s30-5tq144c |

## Revision History

| Date | Version No. | Description |
|---|---|---|
| 09/18/00 | 2.0 | Sectioned the Spartan-II Family data sheet into four modules. Added industrial temperature range information. |
| 10/31/00 | 2.1 | Removed Power down feature. |
| 03/05/01 | 2.2 | Added statement on PROMs. |
| 11/01/01 | 2.3 | Updated Product Availability chart. Minor text edits. |
| 09/03/03 | 2.4 | Added device part marking. |
| 08/02/04 | 2.5 | Added information on Pb-free packaging options and removed discontinued options. |
| 06/13/08 | 2.8 | Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |

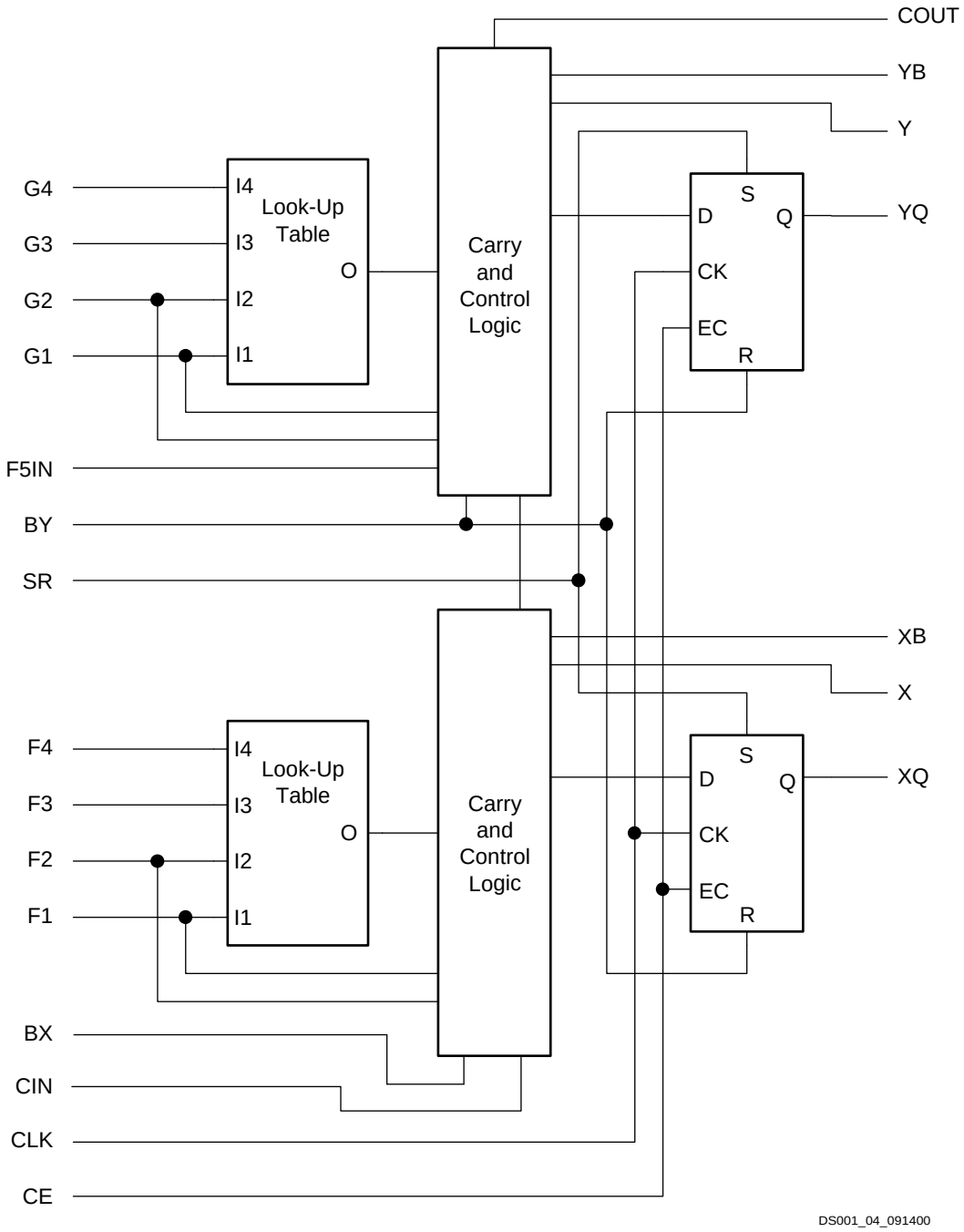



*Figure 4:* **Spartan-II CLB Slice** (two identical slices in each CLB)

### *Storage Elements*

Storage elements in the Spartan-II FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

### *Additional Logic*

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

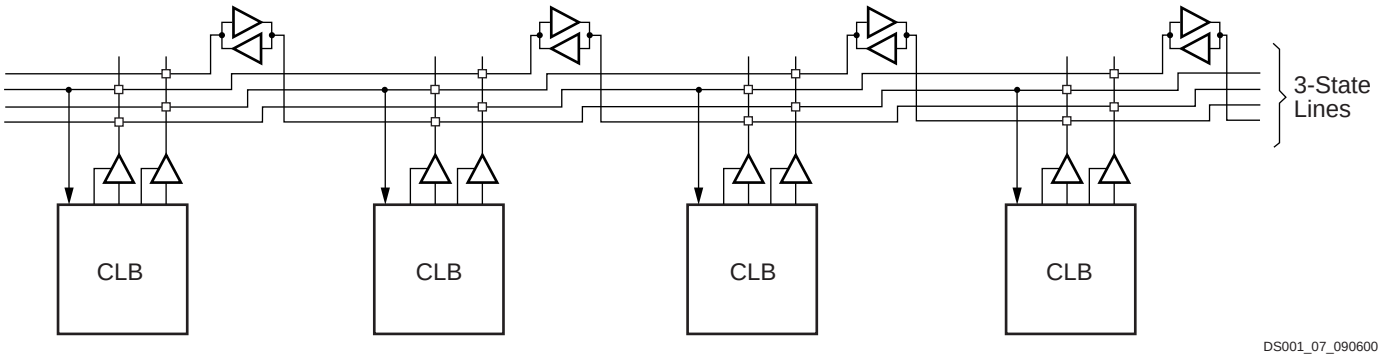



*Figure 7:* **BUFT Connections to Dedicated Horizontal Bus Lines**

## Clock Distribution

The Spartan-II family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 8.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing. Global clock pins do not have the option for internal, weak pull-up resistors.

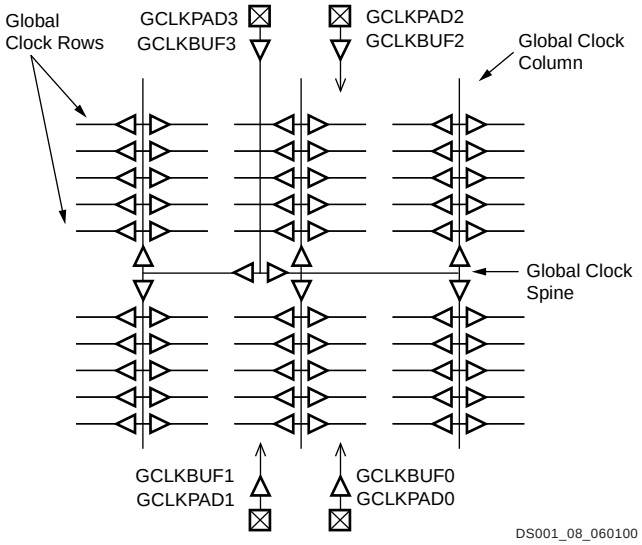



*Figure 8:* **Global Clock Distribution Network**

### *Delay-Locked Loop (DLL)*

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-II devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

## Boundary Scan

Spartan-II devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the $V_{CCO}$ for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and $V_{CCO}$. TDI, TMS, and TCK have a default internal weak pull-up resistor, and TDO has no default resistor. Bitstream options allow setting any of the four TAP pins to have an internal pull-up, pull-down, or neither.

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

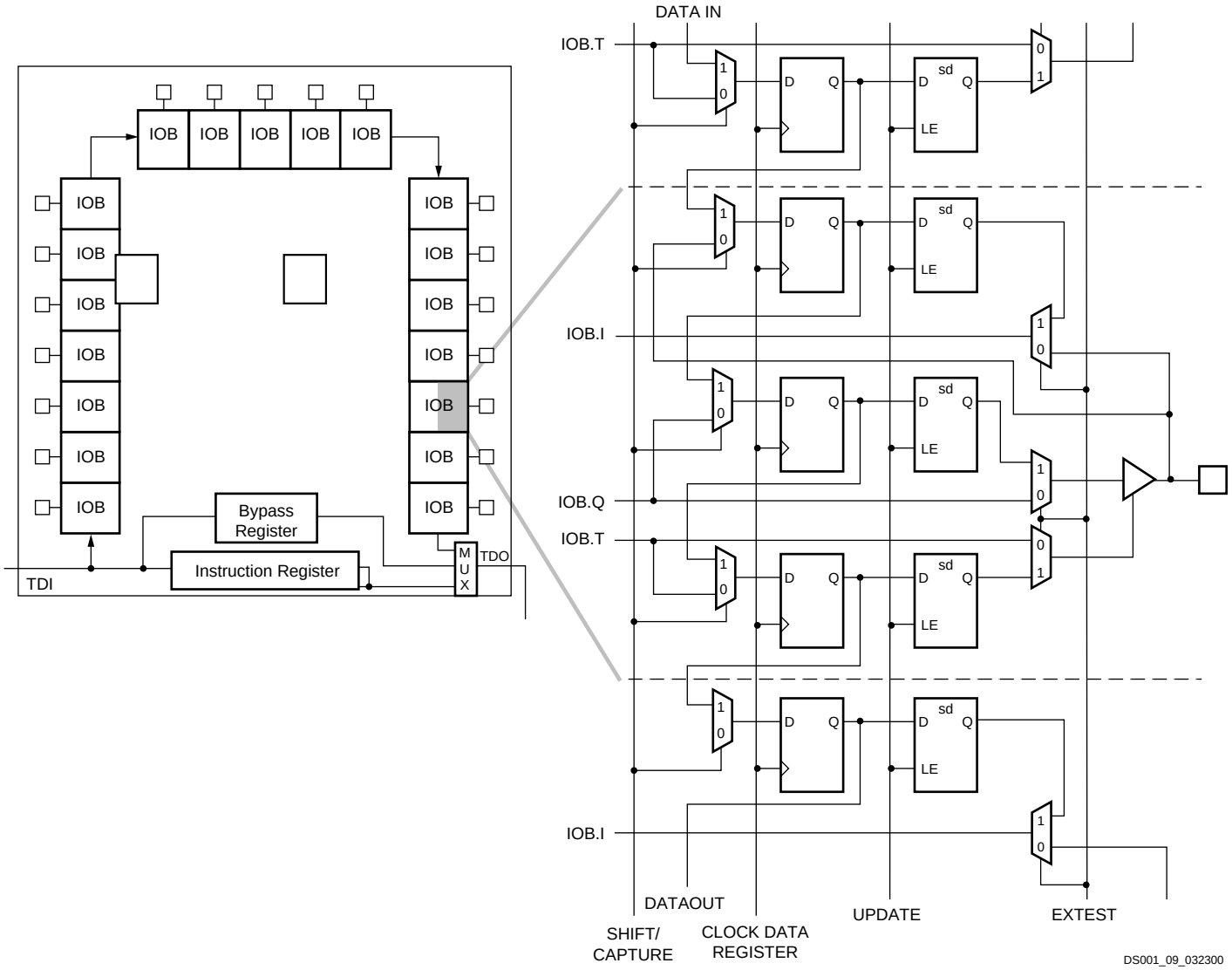



*Figure 9:* **Spartan-II Family Boundary Scan Logic**

### *Bit Sequence*

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the Downloads area.

## Signals

There are two kinds of pins that are used to configure Spartan-II devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{PROGRAM}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a $V_{CCO}$ of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see "Pinout Tables" in Module 4 and XAPP176, *Spartan-II FPGA Series Configuration and Readback*.

## The Process

The sequence of steps necessary to configure Spartan-II devices are shown in Figure 11. The overall flow can be divided into three different phases.

- Initiating Configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

### *Initiating Configuration*

There are two different ways to initiate the configuration process: applying power to the device or asserting the $\overline{\text{PROGRAM}}$ input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Figure 12, page 19. Before configuration can begin, $V_{CCO}$ Bank 2 must be greater than 1.0V. Furthermore, all $V_{CCINT}$ power pins must be connected to a 2.5V supply. For more information on delaying configuration, see "Clearing Configuration Memory," page 19.

Once in user operation, the device can be re-configured simply by pulling the $\overline{\text{PROGRAM}}$ pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase.

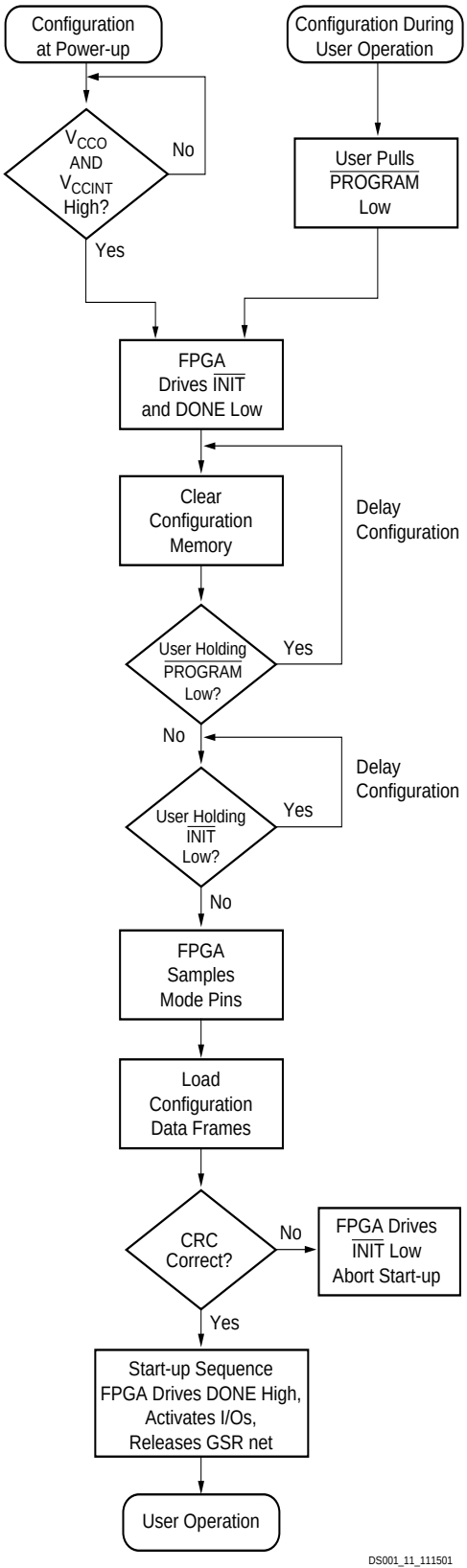
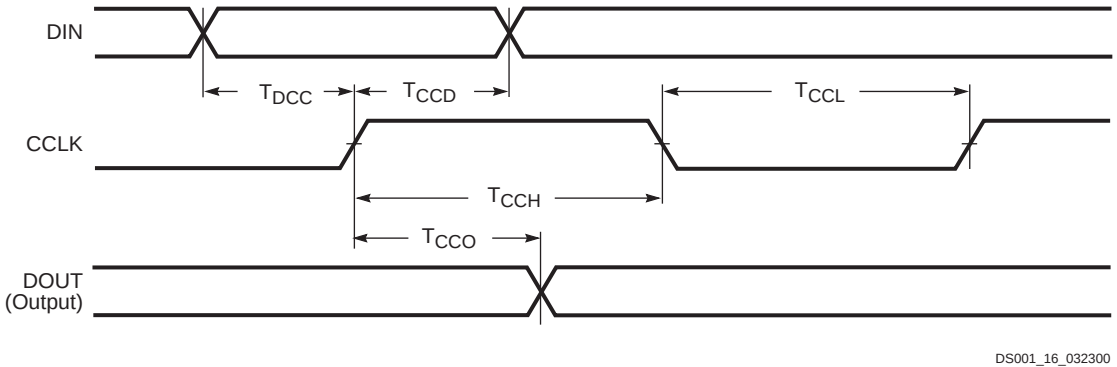



*Figure 11:* **Configuration Flow Diagram**




| Symbol | | Description | | Units |
|---|---|---|---|---|
| $T_{DCC}$ | CCLK | DIN setup | 5 | ns, min |
| $T_{CCD}$ | | DIN hold | 0 | ns, min |
| $T_{CCO}$ | | DOUT | 12 | ns, max |
| $T_{CCH}$ | | High time | 5 | ns, min |
| $T_{CCL}$ | | Low time | 5 | ns, min |
| $F_{CC}$ | | Maximum frequency | 66 | MHz, max |

*Figure 16:* **Slave Serial Mode Timing**

If CCLK is slower than $F_{CCNH}$, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

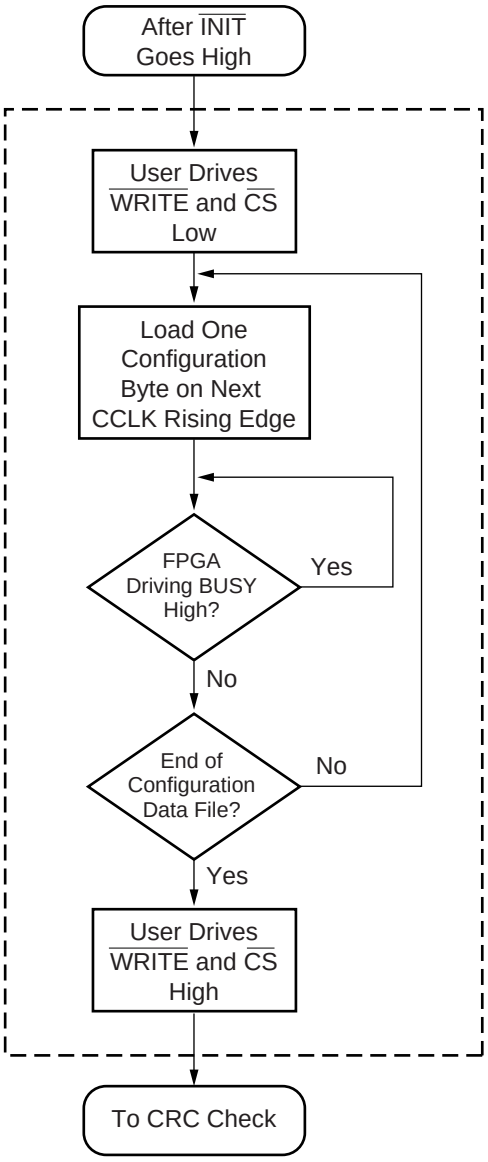



*Figure 19:* **Loading Configuration Data for the Slave Parallel Mode**

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of $\overline{CS}$.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the $\overline{CS}$ signal may be de-asserted until the next byte is valid on D0-D7. While $\overline{CS}$ is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted.

### *Abort*

To abort configuration during a write sequence, de-assert $\overline{WRITE}$ while holding $\overline{CS}$ Low. The abort operation is initiated at the rising edge of CCLK, as shown in Figure 21, page 26. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

## Boundary-Scan Mode

In the boundary-scan mode, no nondedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <10x> on the mode pins (M0, M1, M2).

# Readback

The configuration data stored in the Spartan-II FPGA configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents of all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see XAPP176, *Spartan-II FPGA Family Configuration and Readback.*

### Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the Startup Sequence following device configuration is paused at a user-specified point until the DLL locks. **XAPP176**: *Configuration and Readback of the Spartan-II and Spartan-IIE Families* explains how this can result in delaying the assertion of the DONE pin until the DLL locks.

### DLL Location Constraints

The DLLs are distributed such that there is one DLL in each corner of the device. The location constraint LOC, attached to the DLL primitive with the numeric identifier 0, 1, 2, or 3, controls DLL location. The orientation of the four DLLs and their corresponding clock resources appears in Figure 27.

The LOC property uses the following form.

LOC = DLL2

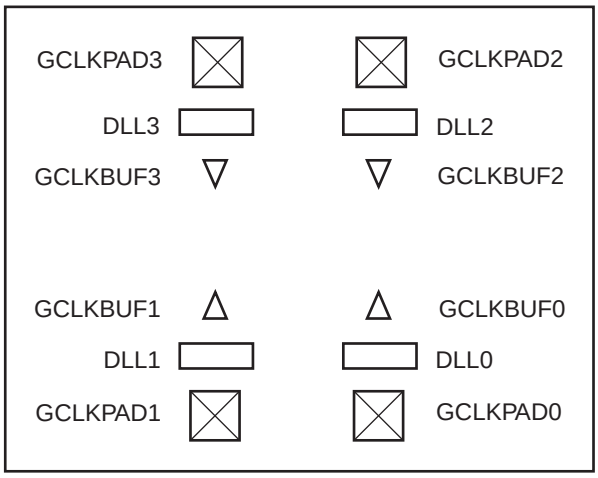



*Figure 27:* **Orientation of DLLs**

## Design Considerations

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

### Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the "DLL Timing Parameters" section of the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

### Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock in a way that has little impact to the DLL. Stopping the clock should be limited to less than approximately 100 µs to keep device cooling to a minimum and maintain the validity of the current tap setting. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED will stay High and remain High when the clock is restored. If these conditions may not be met in the design, apply a manual reset to the DLL after re-starting the input clock, even if the LOCKED signal has not changed.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

### Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). One DLL output can drive more than one OBUF; however, this adds skew.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

# Using Block RAM Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the block RAM memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The block RAM memory offers new capabilities allowing the FPGA designer to simplify designs.

## Operating Modes

Block RAM memory supports two operating modes.

- Read Through
- Write Back

### *Read Through (One Clock Edge)*

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus setup time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

### *Write Back (One Clock Edge)*

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

## Block RAM Characteristics

1. All inputs are registered with the port clock and have a setup to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The block RAM are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

## Library Primitives

Figure 31 and Figure 32 show the two generic library block RAM primitives. Table 11 describes all of the available primitives for synthesis and simulation.

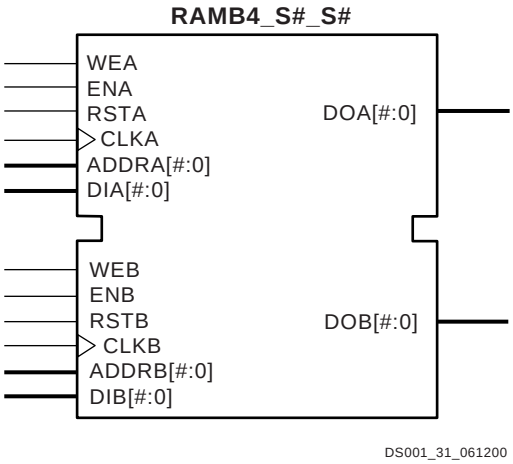



*Figure 31:* **Dual-Port Block RAM Memory**

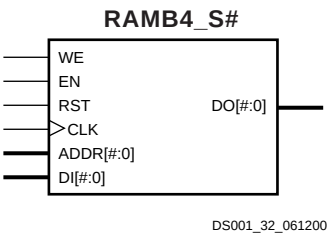



*Figure 32:* **Single-Port Block RAM Memory**

*Table 11:* **Available Library Primitives**

| Primitive | Port A Width | Port B Width |
|---|---|---|
| RAMB4_S1 | 1 | N/A |
| RAMB4_S1_S1 | | 1 |
| RAMB4_S1_S2 | | 2 |
| RAMB4_S1_S4 | | 4 |
| RAMB4_S1_S8 | | 8 |
| RAMB4_S1_S16 | | 16 |
| RAMB4_S2 | 2 | N/A |
| RAMB4_S2_S2 | | 2 |
| RAMB4_S2_S4 | | 4 |
| RAMB4_S2_S8 | | 8 |
| RAMB4_S2_S16 | | 16 |

## Creating Larger RAM Structures

The block RAM columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

## Location Constraints

Block RAM instances can have LOC properties attached to them to constrain the placement. The block RAM placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form:

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

## Conflict Resolution

The block RAM memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
  - The write succeeds
  - The data out on the writing port accurately reflects the data written.
  - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

### *Single Port Timing*

Figure 33 shows a timing diagram for a single port of a block RAM memory. The block RAM AC switching characteristics are specified in the data sheet. The block RAM memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the block RAM memory is now disabled. The DO bus retains the last value.

### *Dual Port Timing*

Figure 34 shows a timing diagram for a true dual-port read/write block RAM memory. The clock on port A has a longer period than the clock on Port B. The timing parameter $T_{BCCS}$, (clock-to-clock setup) is shown on this diagram. The parameter, $T_{BCCS}$ is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

$T_{BCCS}$ is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location will be invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory will be correct, but the read port will have invalid data. At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the $T_{BCCS}$ parameter and the DOB reflects the new memory values written by Port A.

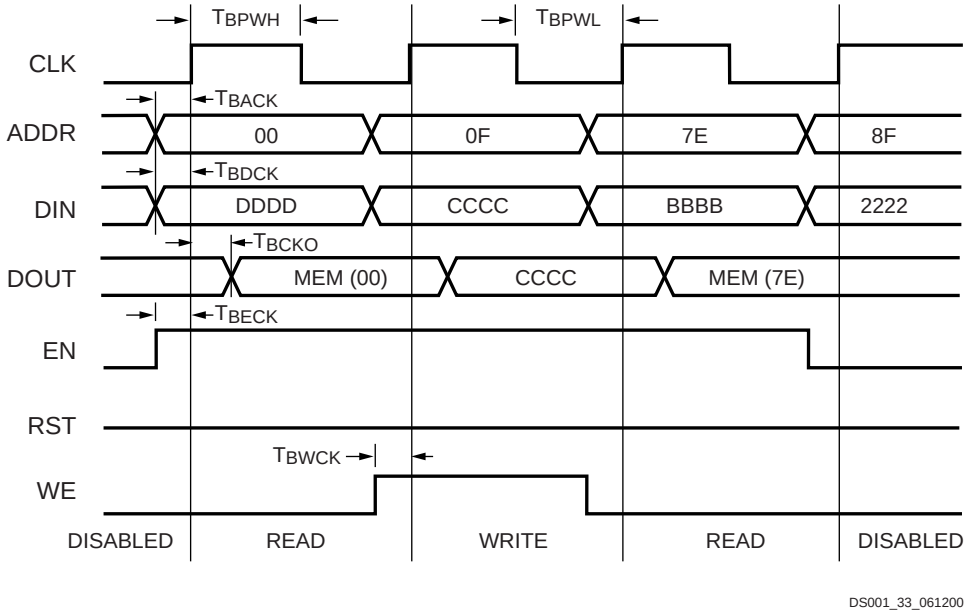



*Figure 33:* **Timing Diagram for Single-Port Block RAM Memory**

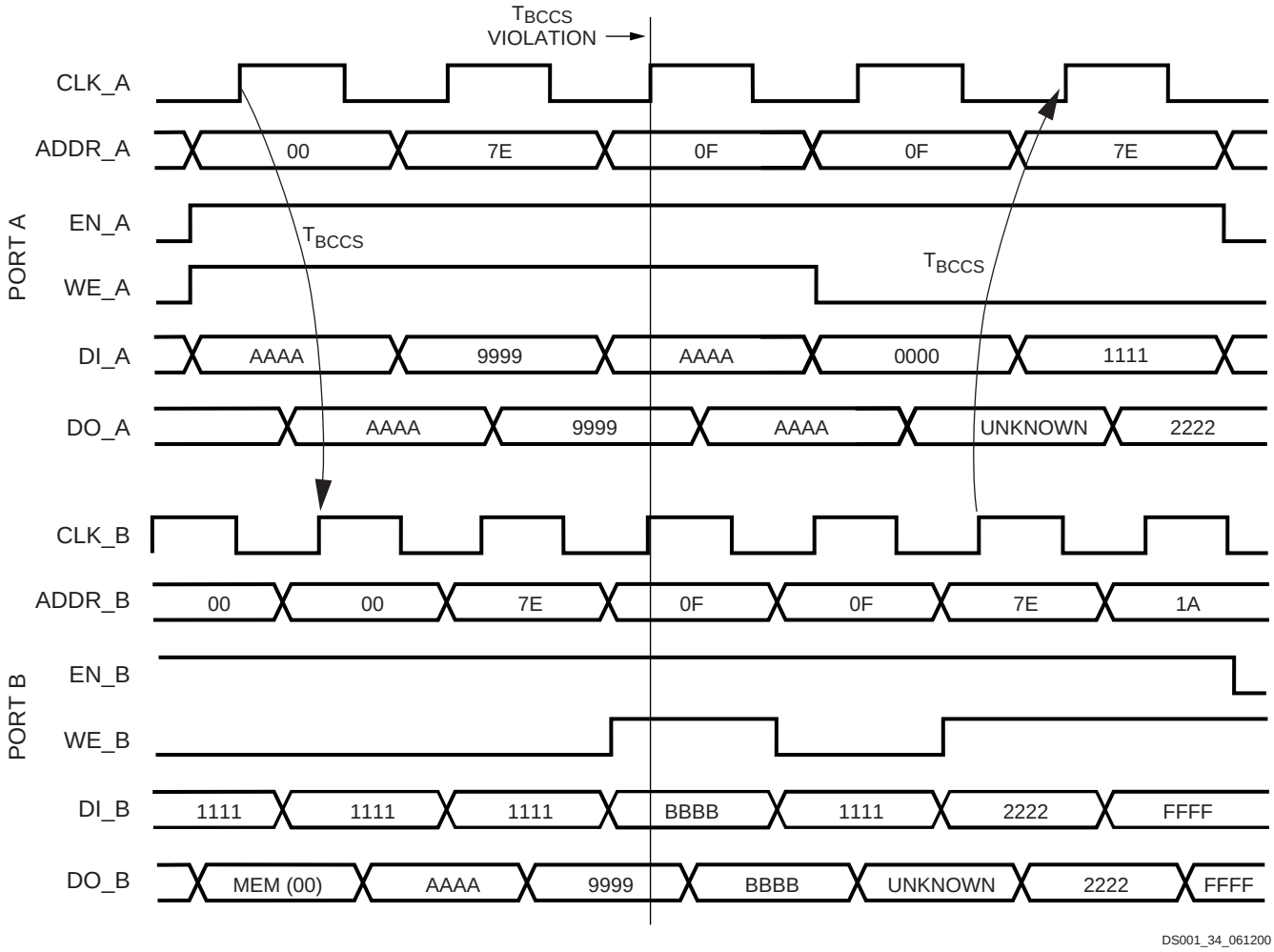



*Figure 34:* **Timing Diagram for a True Dual-Port Read/Write Block RAM Memory**

### CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 51. DC voltage specifications appear in Table 29 for the CTT standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics .

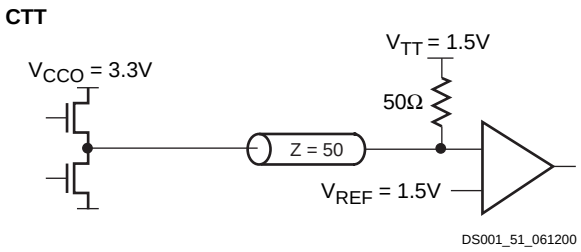



*Figure 51:* **Terminated CTT**

*Table 29:* **CTT Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.05(1) | 3.3 | 3.6 |
| $V_{REF}$ | 1.35 | 1.5 | 1.65 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.55 | 1.7 | - |
| $V_{IL} \leq V_{REF} - 0.2$ | - | 1.3 | 1.45 |
| $V_{OH} \geq V_{REF} + 0.4$ | 1.75 | 1.9 | - |
| $V_{OL} \leq V_{REF} - 0.4$ | - | 1.1 | 1.25 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

**Notes:**
1. Timing delays are calculated based on $V_{CCO}$ min of 3.0V.

### PCI33_3 and PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 30 for the PCI33_3 and PCI66_3 standards. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 30:* **PCI33_3 and PCI66_3 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH} = 0.5 \times V_{CCO}$ | 1.5 | 1.65 | $V_{CCO}$+ 0.5 |
| $V_{IL} = 0.3 \times V_{CCO}$ | –0.5 | 0.99 | 1.08 |
| $V_{OH} = 0.9 \times V_{CCO}$ | 2.7 | - | - |
| $V_{OL} = 0.1 \times V_{CCO}$ | - | - | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 1 | - | - |

**Notes:**
1. Tested according to the relevant specification.

### PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in Table 31 for the PCI33_5 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 31:* **PCI33_5 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.425 | 1.5 | 5.5 |
| $V_{IL}$ | –0.5 | 1.0 | 1.05 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.55 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 1 | - | - |

**Notes:**
1. Tested according to the relevant specification.

### LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 32 for the LVTTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 32:* **LVTTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 2.0 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.8 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –24 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 | - | - |

**Notes:**
1. $V_{OL}$ and $V_{OH}$ for lower drive currents sample tested.

### LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 33 for the LVCMOS2 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 33:* **LVCMOS2 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.7 | - | 5.5 |
| $V_{IL}$ | –0.5 | - | 0.7 |
| $V_{OH}$ | 1.9 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –12 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 12 | - | - |

### AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 34 for the AGP-2X standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

*Table 34:* **AGP-2X Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = N \times V_{CCO}$ (1) | 1.17 | 1.32 | 1.48 |
| $V_{TT}$ | - | - | - |
| $V_{IH} \geq V_{REF} + 0.2$ | 1.37 | 1.52 | - |
| $V_{IL} \leq V_{REF} - 0.2$ | - | 1.12 | 1.28 |
| $V_{OH} \geq 0.9 \times V_{CCO}$ | 2.7 | 3.0 | - |
| $V_{OL} \leq 0.1 \times V_{CCO}$ | - | 0.33 | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 2 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 2 | - | - |

**Notes:**
1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

For design examples and more information on using the I/O, see XAPP179, *Using SelectIO Interfaces in Spartan-II and Spartan-IIE FPGAs*.

## Definition of Terms

In this document, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

**Advance:** Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

**Preliminary:** Based on preliminary characterization. Further changes are not expected.

**Unmarked:** Specifications not identified as either Advance or Preliminary are to be considered Final.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All limits are representative of worst-case supply voltage and junction temperature conditions. Typical numbers are based on measurements taken at a nominal $V_{CCINT}$ level of 2.5V and a junction temperature of 25°C. The parameters included are common to popular designs and typical applications. **All specifications are subject to change without notice.**

## DC Specifications

### Absolute Maximum Ratings(1)

| Symbol | Description | | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage relative to GND(2) | | –0.5 | 3.0 | V |
| $V_{CCO}$ | Supply voltage relative to GND(2) | | –0.5 | 4.0 | V |
| $V_{REF}$ | Input reference voltage | | –0.5 | 3.6 | V |
| $V_{IN}$ | Input voltage relative to GND(3) | 5V tolerant I/O(4) | –0.5 | 5.5 | V |
| | | No 5V tolerance(5) | –0.5 | $V_{CCO}$ + 0.5 | V |
| $V_{TS}$ | Voltage applied to 3-state output | 5V tolerant I/O(4) | –0.5 | 5.5 | V |
| | | No 5V tolerance(5) | –0.5 | $V_{CCO}$ + 0.5 | V |
| $T_{STG}$ | Storage temperature (ambient) | | –65 | +150 | °C |
| $T_J$ | Junction temperature | | - | +125 | °C |

**Notes:**
1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2. Power supplies may turn on in any order.
3. $V_{IN}$ should not exceed $V_{CCO}$ by more than 3.6V over extended periods of time (e.g., longer than a day).
4. Spartan®-II device I/Os are 5V Tolerant whenever the LVTTL, LVCMOS2, or PCI33_5 signal standard has been selected. With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5V or 10 mA, and undershoot must be limited to either –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to +7.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
5. Without 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either $V_{CCO}$ + 0.5V or 10 mA, and undershoot must be limited to –0.5V or 10 mA, whichever is easier to achieve. The Maximum AC conditions are as follows: The device pins may undershoot to –2.0V or overshoot to $V_{CCO}$ + 2.0V, provided this over/undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
6. For soldering guidelines, see the Packaging Information on the Xilinx® web site.

*Table 36:* **Spartan-II Family Package Options**

| Package | Leads | Type | Maximum I/O | Lead Pitch (mm) | Footprint Area (mm) | Height (mm) | Mass[1] (g) |
|---|---|---|---|---|---|---|---|
| VQ100 / VQG100 | 100 | Very Thin Quad Flat Pack (VQFP) | 60 | 0.5 | 16 x 16 | 1.20 | 0.6 |
| TQ144 / TQG144 | 144 | Thin Quad Flat Pack (TQFP) | 92 | 0.5 | 22 x 22 | 1.60 | 1.4 |
| CS144 / CSG144 | 144 | Chip Scale Ball Grid Array (CSBGA) | 92 | 0.8 | 12 x 12 | 1.20 | 0.3 |
| PQ208 / PQG208 | 208 | Plastic Quad Flat Pack (PQFP) | 140 | 0.5 | 30.6 x 30.6 | 3.70 | 5.3 |
| FG256 / FGG256 | 256 | Fine-pitch Ball Grid Array (FBGA) | 176 | 1.0 | 17 x 17 | 2.00 | 0.9 |
| FG456 / FGG456 | 456 | Fine-pitch Ball Grid Array (FBGA) | 284 | 1.0 | 23 x 23 | 2.60 | 2.2 |

**Notes:**

1. Package mass is ±10%.

Note: Some early versions of Spartan-II devices, including the XC2S15 and XC2S30 ES devices and the XC2S150 with date code 0045 or earlier, included a power-down pin. For more information, see Answer Record 10500.

## VCCO Banks

Some of the I/O standards require specific $V_{CCO}$ voltages. These voltages are externally connected to device pins that serve groups of IOBs, called banks. Eight I/O banks result from separating each edge of the FPGA into two banks (see Figure 3 in Module 2). Each bank has multiple $V_{CCO}$ pins which must be connected to the same voltage. In the smaller packages, the $V_{CCO}$ pins are connected between banks, effectively reducing the number of independent banks available (see Table 37). These interconnected banks are shown in the Pinout Tables with $V_{CCO}$ pads for multiple banks connected to the same pin.

*Table 37:* **Independent VCCO Banks Available**

| Package | VQ100 PQ208 | CS144 TQ144 | FG256 FG456 |
|---|---|---|---|
| Independent Banks | 1 | 4 | 8 |

## Package Overview

Table 36 shows the six low-cost, space-saving production package styles for the Spartan-II family.

Each package style is available in an environmentally friendly lead-free (Pb-free) option. The Pb-free packages include an extra ‘G’ in the package style name. For example, the standard “CS144” package becomes “CSG144” when ordered as the Pb-free option. Leaded (non-Pb-free) packages may be available for selected devices, with the same pin-out and without the "G" in the ordering code; contact Xilinx sales for more information. The mechanical dimensions of the standard and Pb-free packages are similar, as shown in the mechanical drawings provided in Table 38.

For additional package information, see UG112: *Device Package User Guide*.

## Mechanical Drawings

Detailed mechanical drawings for each package type are available from the Xilinx web site at the specified location in Table 38.

Material Declaration Data Sheets (MDDS) are also available on the Xilinx web site for each package.

*Table 38:* **Xilinx Package Documentation**

| Package | Drawing | MDDS |
|---|---|---|
| VQ100 | Package Drawing | PK173_VQ100 |
| VQG100 | | PK130_VQG100 |
| TQ144 | Package Drawing | PK169_TQ144 |
| TQG144 | | PK126_TQG144 |
| CS144 | Package Drawing | PK149_CS144 |
| CSG144 | | PK103_CSG144 |
| PQ208 | Package Drawing | PK166_PQ208 |
| PQG208 | | PK123_PQG208 |
| FG256 | Package Drawing | PK151_FG256 |
| FGG256 | | PK105_FGG256 |
| FG456 | Package Drawing | PK154_FG456 |
| FGG456 | | PK109_FGG456 |

## XC2S50 Device Pinouts

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| GND | - | P143 | P1 | GND* | - |
| TMS | - | P142 | P2 | D3 | - |
| I/O | 7 | P141 | P3 | C2 | 149 |
| I/O | 7 | - | - | A2 | 152 |
| I/O | 7 | P140 | P4 | B1 | 155 |
| I/O | 7 | - | - | E3 | 158 |
| I/O | 7 | - | P5 | D2 | 161 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 7 | P139 | P6 | C1 | 164 |
| I/O | 7 | - | P7 | F3 | 167 |
| I/O | 7 | - | - | E2 | 170 |
| I/O | 7 | P138 | P8 | E4 | 173 |
| I/O | 7 | P137 | P9 | D1 | 176 |
| I/O | 7 | P136 | P10 | E1 | 179 |
| GND | - | P135 | P11 | GND* | - |
| $V_{CCO}$ | 7 | - | P12 | $V_{CCO}$ Bank 7* | - |
| $V_{CCINT}$ | - | - | P13 | $V_{CCINT}$* | - |
| I/O | 7 | P134 | P14 | F2 | 182 |
| I/O | 7 | P133 | P15 | G3 | 185 |
| I/O | 7 | - | - | F1 | 188 |
| I/O | 7 | - | P16 | F4 | 191 |
| I/O | 7 | - | P17 | F5 | 194 |
| I/O | 7 | - | P18 | G2 | 197 |
| GND | - | - | P19 | GND* | - |
| I/O, $V_{REF}$ | 7 | P132 | P20 | H3 | 200 |
| I/O | 7 | P131 | P21 | G4 | 203 |
| I/O | 7 | - | - | H2 | 206 |
| I/O | 7 | P130 | P22 | G5 | 209 |
| I/O | 7 | - | P23 | H4 | 212 |
| I/O, IRDY(1) | 7 | P129 | P24 | G1 | 215 |
| GND | - | P128 | P25 | GND* | - |
| $V_{CCO}$ | 7 | P127 | P26 | $V_{CCO}$ Bank 7* | - |
| $V_{CCO}$ | 6 | P127 | P26 | $V_{CCO}$ Bank 6* | - |
| I/O, TRDY(1) | 6 | P126 | P27 | J2 | 218 |
| $V_{CCINT}$ | - | P125 | P28 | $V_{CCINT}$* | - |
| I/O | 6 | P124 | P29 | H1 | 224 |
| I/O | 6 | - | - | J4 | 227 |
| I/O | 6 | P123 | P30 | J1 | 230 |
| I/O, $V_{REF}$ | 6 | P122 | P31 | J3 | 233 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| GND | - | - | P32 | GND* | - |
| I/O | 6 | - | P33 | K5 | 236 |
| I/O | 6 | - | P34 | K2 | 239 |
| I/O | 6 | - | P35 | K1 | 242 |
| I/O | 6 | - | - | K3 | 245 |
| I/O | 6 | P121 | P36 | L1 | 248 |
| I/O | 6 | P120 | P37 | L2 | 251 |
| $V_{CCINT}$ | - | - | P38 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 6 | - | P39 | $V_{CCO}$ Bank 6* | - |
| GND | - | P119 | P40 | GND* | - |
| I/O | 6 | P118 | P41 | K4 | 254 |
| I/O | 6 | P117 | P42 | M1 | 257 |
| I/O | 6 | P116 | P43 | L4 | 260 |
| I/O | 6 | - | - | M2 | 263 |
| I/O | 6 | - | P44 | L3 | 266 |
| I/O, $V_{REF}$ | 6 | P115 | P45 | N1 | 269 |
| GND | - | - | - | GND* | - |
| I/O | 6 | - | P46 | P1 | 272 |
| I/O | 6 | - | - | L5 | 275 |
| I/O | 6 | P114 | P47 | N2 | 278 |
| I/O | 6 | - | - | M4 | 281 |
| I/O | 6 | P113 | P48 | R1 | 284 |
| I/O | 6 | P112 | P49 | M3 | 287 |
| M1 | - | P111 | P50 | P2 | 290 |
| GND | - | P110 | P51 | GND* | - |
| M0 | - | P109 | P52 | N3 | 291 |
| $V_{CCO}$ | 6 | P108 | P53 | $V_{CCO}$ Bank 6* | - |
| $V_{CCO}$ | 5 | P107 | P53 | $V_{CCO}$ Bank 5* | - |
| M2 | - | P106 | P54 | R3 | 292 |
| I/O | 5 | - | - | N5 | 299 |
| I/O | 5 | P103 | P57 | T2 | 302 |
| I/O | 5 | - | - | P5 | 305 |
| I/O | 5 | - | P58 | T3 | 308 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 5 | P102 | P59 | T4 | 311 |
| I/O | 5 | - | P60 | M6 | 314 |
| I/O | 5 | - | - | T5 | 317 |
| I/O | 5 | P101 | P61 | N6 | 320 |
| I/O | 5 | P100 | P62 | R5 | 323 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | TQ144 | PQ208 | FG256 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 5 | P99 | P63 | P6 | 326 |
| GND | - | P98 | P64 | GND* | - |
| $V_{CCO}$ | 5 | - | P65 | $V_{CCO}$ Bank 5* | - |
| $V_{CCINT}$ | - | P97 | P66 | $V_{CCINT}$* | - |
| I/O | 5 | P96 | P67 | R6 | 329 |
| I/O | 5 | P95 | P68 | M7 | 332 |
| I/O | 5 | - | P69 | N7 | 338 |
| I/O | 5 | - | P70 | T6 | 341 |
| I/O | 5 | - | P71 | P7 | 344 |
| GND | - | - | P72 | GND* | - |
| I/O, $V_{REF}$ | 5 | P94 | P73 | P8 | 347 |
| I/O | 5 | - | P74 | R7 | 350 |
| I/O | 5 | - | - | T7 | 353 |
| I/O | 5 | P93 | P75 | T8 | 356 |
| $V_{CCINT}$ | - | P92 | P76 | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P91 | P77 | R8 | 365 |
| $V_{CCO}$ | 5 | P90 | P78 | $V_{CCO}$ Bank 5* | - |
| $V_{CCO}$ | 4 | P90 | P78 | $V_{CCO}$ Bank 4* | - |
| GND | - | P89 | P79 | GND* | - |
| I, GCK0 | 4 | P88 | P80 | N8 | 366 |
| I/O | 4 | P87 | P81 | N9 | 370 |
| I/O | 4 | P86 | P82 | R9 | 373 |
| I/O | 4 | - | - | N10 | 376 |
| I/O | 4 | - | P83 | T9 | 379 |
| I/O, $V_{REF}$ | 4 | P85 | P84 | P9 | 382 |
| GND | - | - | P85 | GND* | - |
| I/O | 4 | - | P86 | M10 | 385 |
| I/O | 4 | - | P87 | R10 | 388 |
| I/O | 4 | - | P88 | P10 | 391 |
| I/O | 4 | P84 | P89 | T10 | 397 |
| I/O | 4 | P83 | P90 | R11 | 400 |
| $V_{CCINT}$ | - | P82 | P91 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | - | P92 | $V_{CCO}$ Bank 4* | - |
| GND | - | P81 | P93 | GND* | - |
| I/O | 4 | P80 | P94 | M11 | 403 |
| I/O | 4 | P79 | P95 | T11 | 406 |
| I/O | 4 | P78 | P96 | N11 | 409 |
| I/O | 4 | - | - | R12 | 412 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | TQ144 | PQ208 | FG256 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 4 | - | P97 | P11 | 415 |
| I/O, $V_{REF}$ | 4 | P77 | P98 | T12 | 418 |
| GND | - | - | - | GND* | - |
| I/O | 4 | - | P99 | T13 | 421 |
| I/O | 4 | - | - | N12 | 424 |
| I/O | 4 | P76 | P100 | R13 | 427 |
| I/O | 4 | - | - | P12 | 430 |
| I/O | 4 | P75 | P101 | P13 | 433 |
| I/O | 4 | P74 | P102 | T14 | 436 |
| GND | - | P73 | P103 | GND* | - |
| DONE | 3 | P72 | P104 | R14 | 439 |
| $V_{CCO}$ | 4 | P71 | P105 | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P70 | P105 | $V_{CCO}$ Bank 3* | - |
| $\overline{PROGRAM}$ | - | P69 | P106 | P15 | 442 |
| I/O ($\overline{INIT}$) | 3 | P68 | P107 | N15 | 443 |
| I/O (D7) | 3 | P67 | P108 | N14 | 446 |
| I/O | 3 | - | - | T15 | 449 |
| I/O | 3 | P66 | P109 | M13 | 452 |
| I/O | 3 | - | - | R16 | 455 |
| I/O | 3 | - | P110 | M14 | 458 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 3 | P65 | P111 | L14 | 461 |
| I/O | 3 | - | P112 | M15 | 464 |
| I/O | 3 | - | - | L12 | 467 |
| I/O | 3 | P64 | P113 | P16 | 470 |
| I/O | 3 | P63 | P114 | L13 | 473 |
| I/O (D6) | 3 | P62 | P115 | N16 | 476 |
| GND | - | P61 | P116 | GND* | - |
| $V_{CCO}$ | 3 | - | P117 | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | - | P118 | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P60 | P119 | M16 | 479 |
| I/O | 3 | P59 | P120 | K14 | 482 |
| I/O | 3 | - | - | L16 | 485 |
| I/O | 3 | - | P121 | K13 | 488 |
| I/O | 3 | - | P122 | L15 | 491 |
| I/O | 3 | - | P123 | K12 | 494 |
| GND | - | - | P124 | GND* | - |
| I/O, $V_{REF}$ | 3 | P58 | P125 | K16 | 497 |
| I/O (D4) | 3 | P57 | P126 | J16 | 500 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| I/O | 2 | - | - | F12 | G20 | 695 |
| I/O | 2 | - | P149 | E15 | F19 | 701 |
| I/O, $V_{REF}$ | 2 | P41 | P150 | F13 | F21 | 704 |
| $V_{CCO}$ | 2 | - | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 2 | - | P151 | E14 | F20 | 707 |
| I/O | 2 | - | - | C16 | F18 | 710 |
| I/O | 2 | - | - | - | E21 | 713 |
| I/O | 2 | P40 | P152 | E13 | D22 | 716 |
| I/O | 2 | - | - | B16 | E20 | 719 |
| I/O (DIN, D0) | 2 | P39 | P153 | D14 | D20 | 725 |
| I/O (DOUT, BUSY) | 2 | P38 | P154 | C15 | C21 | 728 |
| CCLK | 2 | P37 | P155 | D15 | B22 | 731 |
| $V_{CCO}$ | 2 | P36 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| $V_{CCO}$ | 1 | P35 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P34 | P157 | B14 | A21 | - |
| GND | - | P33 | P158 | GND* | GND* | - |
| TDI | - | P32 | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P31 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P30 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | C12 | D17 | 9 |
| I/O | 1 | P29 | P162 | A14 | A19 | 12 |
| I/O | 1 | - | - | - | B18 | 15 |
| I/O | 1 | - | - | D12 | C17 | 18 |
| I/O | 1 | - | P163 | B12 | D16 | 21 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P28 | P164 | C11 | A18 | 24 |
| I/O | 1 | - | P165 | A13 | B17 | 27 |
| I/O | 1 | - | - | D11 | D15 | 33 |
| I/O | 1 | - | P166 | A12 | C16 | 36 |
| I/O | 1 | - | - | - | D14 | 39 |
| I/O, $V_{REF}$ | 1 | P27 | P167 | E11 | E14 | 42 |
| I/O | 1 | P26 | P168 | B11 | A16 | 45 |
| GND | - | P25 | P169 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|---|
| Function | Bank | | | | | |
| $V_{CCO}$ | 1 | - | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P24 | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P23 | P172 | A11 | C15 | 48 |
| I/O | 1 | P22 | P173 | C10 | B15 | 51 |
| I/O | 1 | - | - | - | F12 | 54 |
| I/O | 1 | - | P174 | B10 | C14 | 57 |
| I/O | 1 | - | P175 | D10 | D13 | 63 |
| I/O | 1 | - | P176 | A10 | C13 | 66 |
| GND | - | - | P177 | GND* | GND* | - |
| I/O, $V_{REF}$ | 1 | P21 | P178 | B9 | B13 | 69 |
| I/O | 1 | - | P179 | E10 | E12 | 72 |
| I/O | 1 | - | - | A9 | B12 | 75 |
| I/O | 1 | P20 | P180 | D9 | D12 | 78 |
| I/O | 1 | P19 | P181 | A8 | D11 | 84 |
| I, GCK2 | 1 | P18 | P182 | C9 | A11 | 90 |
| GND | - | P17 | P183 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P16 | P184 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P16 | P184 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P15 | P185 | B8 | C11 | 91 |
| $V_{CCINT}$ | - | P14 | P186 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 0 | P13 | P187 | A7 | A10 | 101 |
| I/O | 0 | - | - | D8 | B10 | 104 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| $V_{CCO}$ | 3 | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P119 | M16 | R21 | 833 |
| I/O | 3 | P120 | K14 | P18 | 836 |
| I/O | 3 | - | - | R22 | 839 |
| I/O | 3 | - | - | P19 | 842 |
| I/O | 3 | - | L16 | P20 | 845 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P121 | K13 | P21 | 848 |
| I/O | 3 | - | - | N19 | 851 |
| I/O | 3 | - | - | P22 | 854 |
| I/O | 3 | P122 | L15 | N18 | 857 |
| I/O | 3 | P123 | K12 | N20 | 860 |
| GND | - | P124 | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P125 | K16 | N21 | 863 |
| I/O (D4) | 3 | P126 | J16 | N22 | 866 |
| I/O | 3 | - | - | M17 | 872 |
| I/O | 3 | - | J14 | M19 | 875 |
| I/O | 3 | P127 | K15 | M20 | 878 |
| I/O | 3 | - | - | M18 | 881 |
| $V_{CCINT}$ | - | P128 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P129 | J15 | M22 | 890 |
| $V_{CCO}$ | 3 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P131 | GND* | GND* | - |
| I/O, IRDY(1) | 2 | P132 | H16 | L20 | 893 |
| I/O | 2 | P133 | H14 | L17 | 896 |
| I/O | 2 | - | - | L18 | 902 |
| I/O | 2 | P134 | H15 | L21 | 905 |
| I/O | 2 | - | J13 | L22 | 908 |
| I/O | 2 | - | - | K19 | 911 |
| I/O (D3) | 2 | P135 | G16 | K20 | 917 |
| I/O, $V_{REF}$ | 2 | P136 | H13 | K21 | 920 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P137 | GND* | GND* | - |
| I/O | 2 | P138 | G14 | K22 | 923 |
| I/O | 2 | P139 | G15 | J21 | 926 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 2 | - | - | K18 | 929 |
| I/O | 2 | - | - | J20 | 932 |
| I/O | 2 | P140 | G12 | J18 | 935 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | F16 | J22 | 938 |
| I/O | 2 | - | - | J19 | 941 |
| I/O | 2 | - | - | H21 | 944 |
| I/O | 2 | P141 | G13 | H19 | 947 |
| I/O (D2) | 2 | P142 | F15 | H20 | 950 |
| $V_{CCINT}$ | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P146 | E16 | H22 | 953 |
| I/O, $V_{REF}$ | 2 | P147 | F14 | H18 | 956 |
| I/O | 2 | - | - | G21 | 962 |
| I/O | 2 | P148 | D16 | G18 | 965 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | F12 | G20 | 968 |
| I/O | 2 | - | - | G19 | 971 |
| I/O | 2 | - | - | F22 | 974 |
| I/O | 2 | P149 | E15 | F19 | 977 |
| I/O, $V_{REF}$ | 2 | P150 | F13 | F21 | 980 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | P151 | E14 | F20 | 983 |
| I/O | 2 | - | C16 | F18 | 986 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | - | E22 | 989 |
| I/O | 2 | - | - | E21 | 995 |
| I/O, $V_{REF}$ | 2 | P152 | E13 | D22 | 998 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | B16 | E20 | 1001 |
| I/O | 2 | - | - | D21 | 1004 |
| I/O | 2 | - | - | C22 | 1007 |
| I/O (DIN, D0) | 2 | P153 | D14 | D20 | 1013 |
| I/O (DOUT, BUSY) | 2 | P154 | C15 | C21 | 1016 |
| CCLK | 2 | P155 | D15 | B22 | 1019 |
| $V_{CCO}$ | 2 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| GND | - | P198 | GND* | GND* | - |
| I/O | 0 | P199 | A5 | B7 | 188 |
| I/O, $V_{REF}$ | 0 | P200 | C6 | E8 | 191 |
| I/O | 0 | - | - | D8 | 197 |
| I/O | 0 | P201 | B5 | C7 | 200 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | D6 | D7 | 203 |
| I/O | 0 | - | - | B6 | 206 |
| I/O | 0 | - | - | A5 | 209 |
| I/O | 0 | P202 | A4 | D6 | 212 |
| I/O, $V_{REF}$ | 0 | P203 | B4 | C6 | 215 |
| $V_{CCO}$ | 0 | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | P204 | E6 | B5 | 218 |
| I/O | 0 | - | D5 | E7 | 221 |
| I/O | 0 | - | - | A4 | 224 |
| I/O | 0 | - | - | E6 | 230 |
| I/O, $V_{REF}$ | 0 | P205 | A3 | B4 | 233 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | C5 | A3 | 236 |
| I/O | 0 | - | - | B3 | 239 |
| I/O | 0 | - | - | D5 | 242 |
| I/O | 0 | P206 | B3 | C5 | 248 |
| TCK | - | P207 | C4 | C4 | - |
| $V_{CCO}$ | 0 | P208 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P208 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S200 Package Pins

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

11/02/00

**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |