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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	216
Number of Logic Elements/Cells	972
Total RAM Bits	24576
Number of I/O	92
Number of Gates	30000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s30-5tqg144i

General Overview

The Spartan-II family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-II FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes.

Spartan-II FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-II FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-II FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-II devices provide system clock rates up to 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-II FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

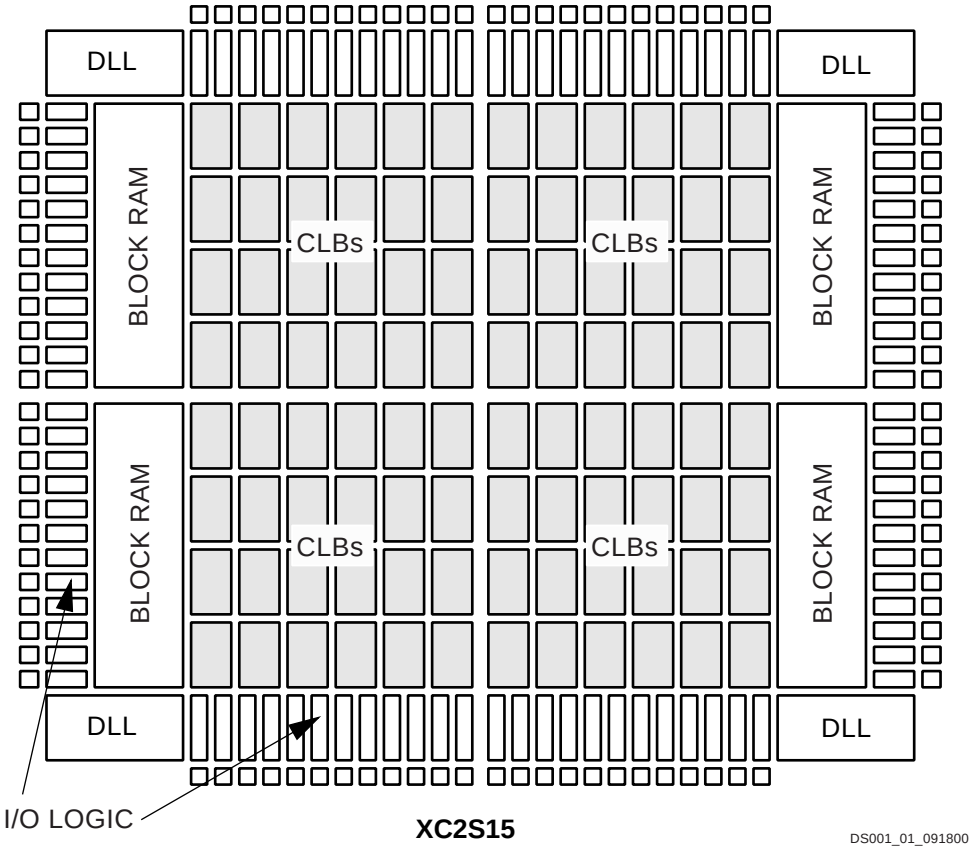


Figure 1: **Basic Spartan-II Family FPGA Block Diagram**

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

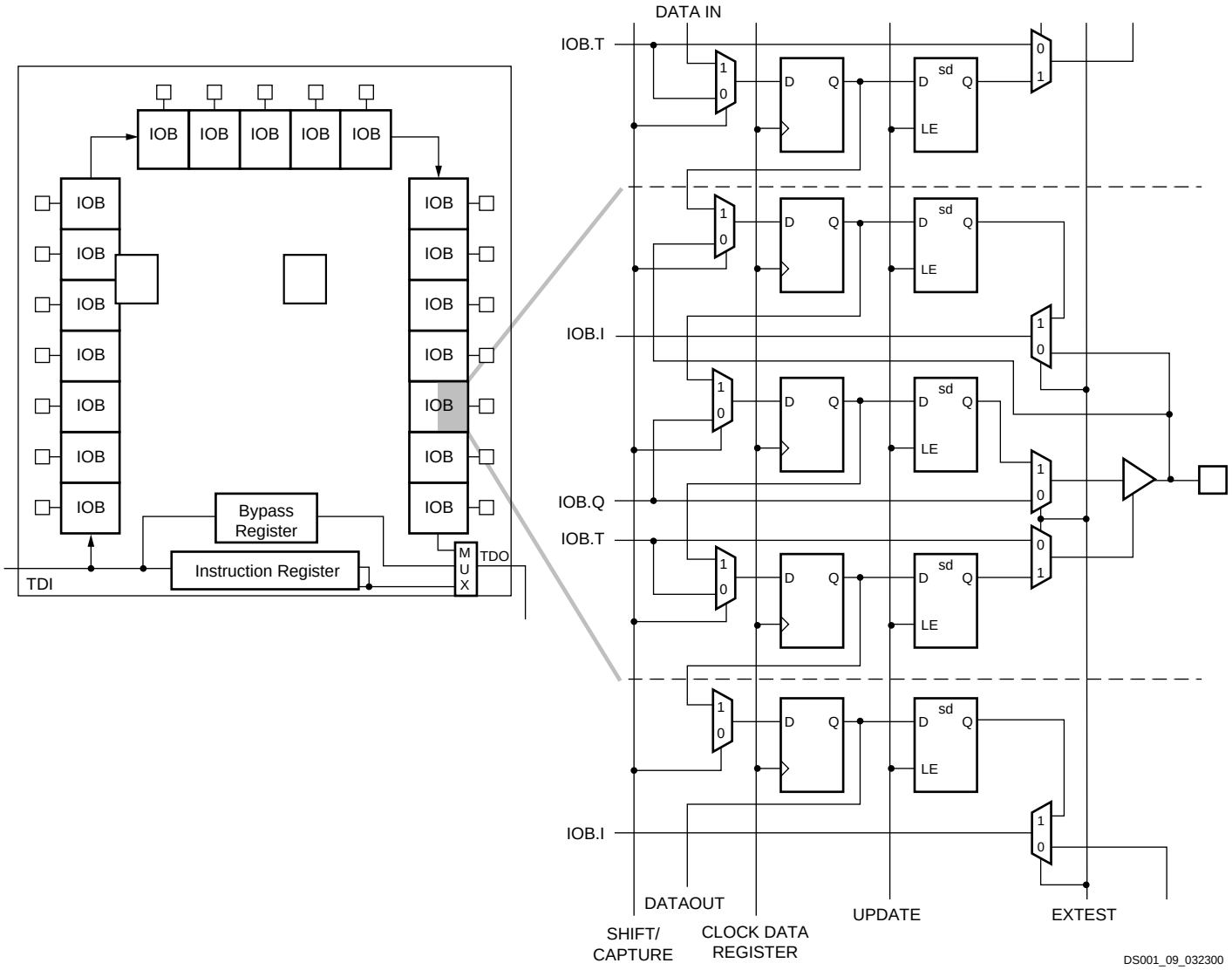


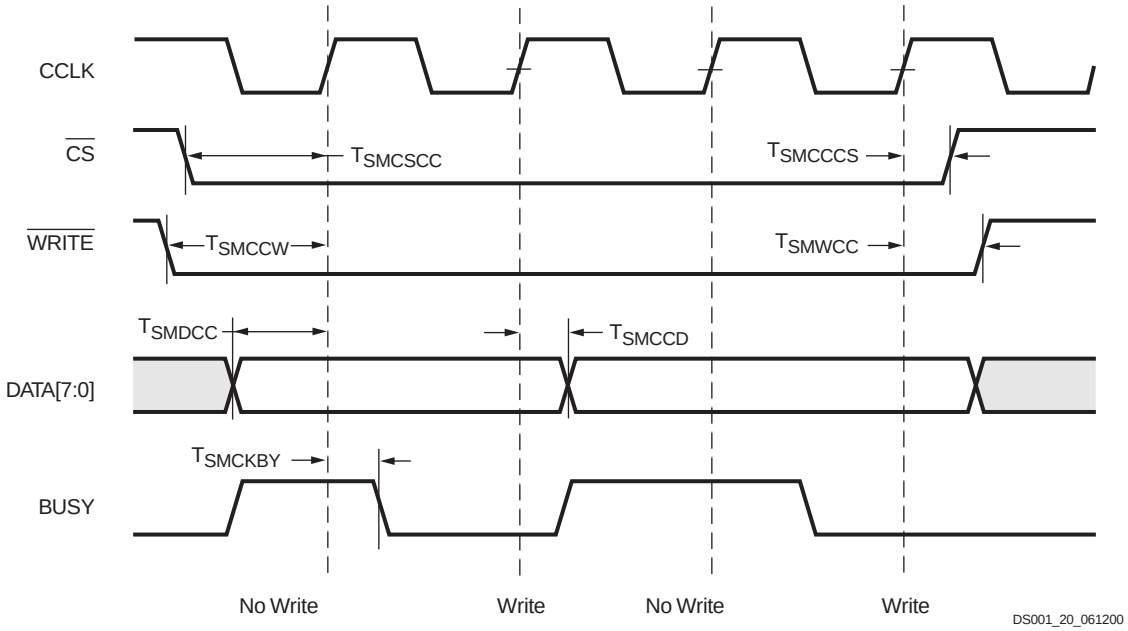
Figure 9: **Spartan-II Family Boundary Scan Logic**

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the Downloads area.



Symbol		Description		Units
T_{SMDCC}	CCLK	D0-D7 setup/hold	5	ns, min
T_{SMCCD}		D0-D7 hold	0	ns, min
T_{SMCSCC}		$\overline{CS}$ setup	7	ns, min
T_{SMCCCS}		$\overline{CS}$ hold	0	ns, min
T_{SMCCW}		$\overline{WRITE}$ setup	7	ns, min
T_{SMWCC}		$\overline{WRITE}$ hold	0	ns, min
T_{SMCKBY}		BUSY propagation delay	12	ns, max
F_{CC}		Maximum frequency	66	MHz, max
F_{CCNH}		Maximum frequency with no handshake	50	MHz, max

Figure 20: **Slave Parallel Write Timing**

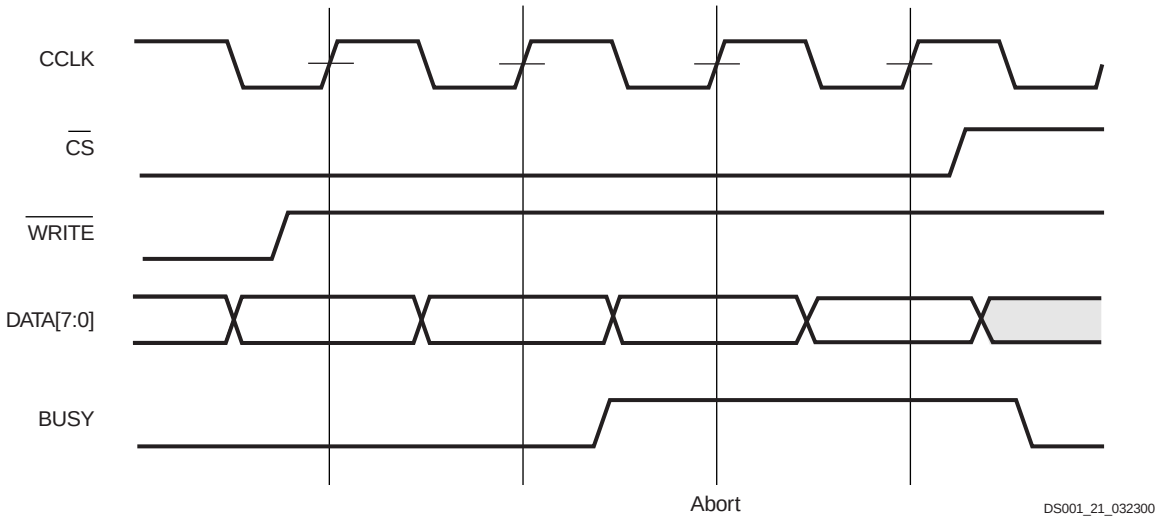


Figure 21: **Slave Parallel Write Abort Waveforms**

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF primitive names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24). The default is slew rate limited with 12 mA drive.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. Table 17 summarizes the output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 17: **Output Standards Compatibility Requirements**

Rule 1	Only outputs with standards which share compatible V_{CCO} may be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 39, typically implements 3-state outputs or bidirectional I/O.

With no extension or property specified for the generic OBUFT primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT primitive names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

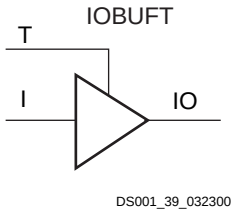


Figure 39: **3-State Output Buffer Primitive (OBUFT**

The Versatile I/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF primitive for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 40.

With no extension or property specified for the generic IOBUF primitive, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF primitive names is as follows:

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

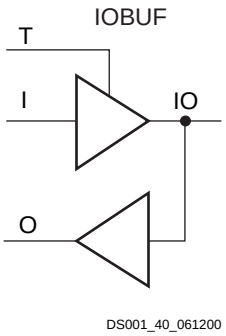


Figure 40: **Input/Output Buffer Primitiveprimitive (IOBUF)**

When the IOBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36, page 39 for a representation of the Spartan-II FPGA I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

IOB Flip-Flop/Latch Property

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified:

map -pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each Versatile I/O primitive with the location constraint LOC attached to the Versatile I/O primitive. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

LOC=A42

LOC=P37

Output Slew Rate Property

In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

Output Drive Strength Property

For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE=

property. This property could have one of the following seven values.

DRIVE=2

DRIVE=4

DRIVE=6

DRIVE=8

DRIVE=12 (Default)

DRIVE=16

DRIVE=24

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36, page 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The V_{CCO} supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined V_{CCO} supply. The TQ144 and the CS144 packages provide four independent V_{CCO} supplies. The FG256 and the FG456 provide eight independent V_{CCO} supplies.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques:

None
Series
Parallel (Shunt)
Series and Parallel (Series-Shunt)

Input termination techniques include the following:

None
Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 41.

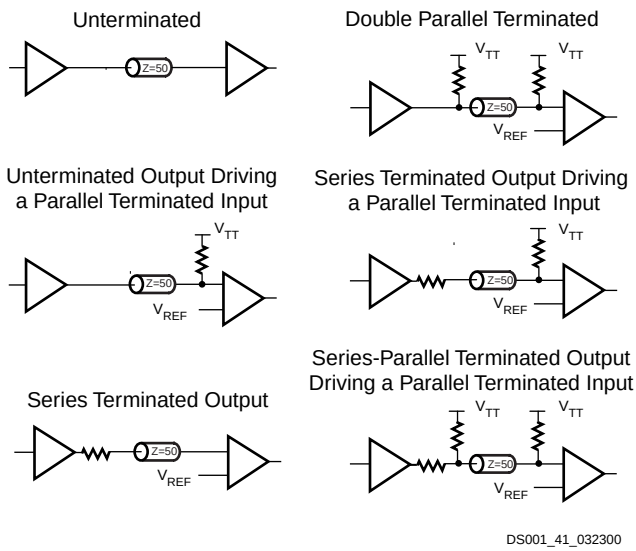


Figure 41: **Overview of Standard Input and Output Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and

ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 18 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 19 for the number of effective output power/ground pairs for each Spartan-II device and package combination.

Table 18: **Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package	
	CS, FG	PQ, TQ, VQ
LVTTL Slow Slew Rate, 2 mA drive	68	36
LVTTL Slow Slew Rate, 4 mA drive	41	20
LVTTL Slow Slew Rate, 6 mA drive	29	15
LVTTL Slow Slew Rate, 8 mA drive	22	12
LVTTL Slow Slew Rate, 12 mA drive	17	9
LVTTL Slow Slew Rate, 16 mA drive	14	7
LVTTL Slow Slew Rate, 24 mA drive	9	5
LVTTL Fast Slew Rate, 2 mA drive	40	21
LVTTL Fast Slew Rate, 4 mA drive	24	12
LVTTL Fast Slew Rate, 6 mA drive	17	9
LVTTL Fast Slew Rate, 8 mA drive	13	7
LVTTL Fast Slew Rate, 12 mA drive	10	5
LVTTL Fast Slew Rate, 16 mA drive	8	4
LVTTL Fast Slew Rate, 24 mA drive	5	3
LVCMOS2	10	5
PCI	8	4
GTL	4	4
GTL+	4	4
HSTL Class I	18	9
HSTL Class III	9	5
HSTL Class IV	5	3
SSTL2 Class I	15	8
SSTL2 Class II	10	5
SSTL3 Class I	11	6
SSTL3 Class II	7	4
CTT	14	7
AGP	9	5

Notes:
1. This analysis assumes a 35 pF load for each output.

Table 19: **Effective Output Power/Ground Pairs for Spartan-II Devices**

Pkg.	Spartan-II Devices					
	XC2S 15	XC2S 30	XC2S 50	XC2S 100	XC2S 150	XC2S 200
VQ100	8	8	-	-	-	-
CS144	12	12	-	-	-	-
TQ144	12	12	12	12	-	-
PQ208	-	16	16	16	16	16
FG256	-	-	16	16	16	16
FG456	-	-	-	48	48	48

Termination Examples

Creating a design with the Versatile I/O features requires the instantiation of the desired library primitive within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the Versatile I/O features. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 45. DC voltage specifications appear in Table 23 for the HSTL_III standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

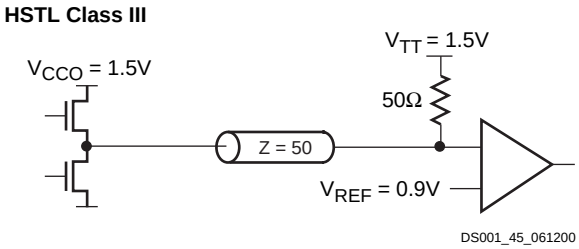


Figure 45: **Terminated HSTL Class III**

Table 23: **HSTL Class III Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Notes:

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

HSTL Class IV

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 46.DC voltage specifications appear in Table 23 for the HSTL_IV standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

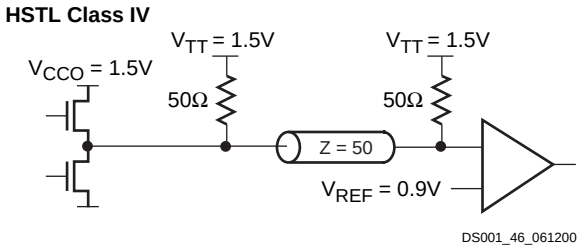


Figure 46: **Terminated HSTL Class IV**

Table 24: **HSTL Class IV Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	48	-	-

Notes:

1. Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

SSTL3 Class I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 47. DC voltage specifications appear in Table 25 for the SSTL3_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

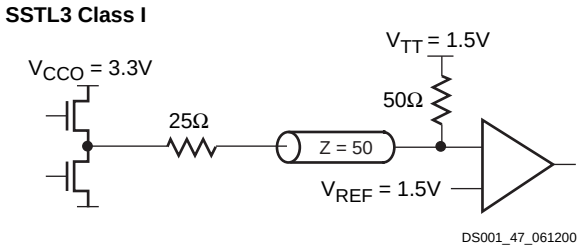


Figure 47: **Terminated SSTL3 Class I**

Table 25: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.6$	1.9	-	-
$V_{OL} \leq V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3.
2. V_{IL} minimum does not conform to the formula.

SSTL3 Class II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 48. DC voltage specifications appear in Table 26 for the SSTL3_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

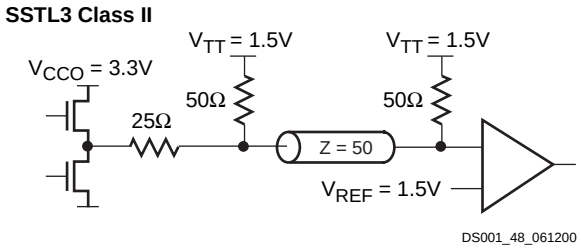


Figure 48: **Terminated SSTL3 Class II**

Table 26: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.8$	2.1	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 49. DC voltage specifications appear in Table 27 for the SSTL2_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

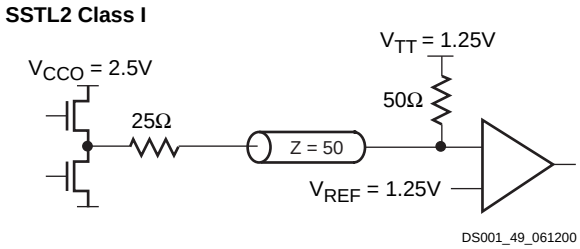


Figure 49: **Terminated SSTL2 Class I**

Table 27: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \geq V_{REF} + 0.18$	1.33	1.43	$3.0^{(2)}$
$V_{IL} \leq V_{REF} - 0.18$	$-0.3^{(3)}$	1.07	1.17
$V_{OH} \geq V_{REF} + 0.61$	1.76	-	-
$V_{OL} \leq V_{REF} - 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL} at V_{OL} (mA)	7.6	-	-

Notes:
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

SSTL2 Class II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 50. DC voltage specifications appear in Table 28 for the SSTL2_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

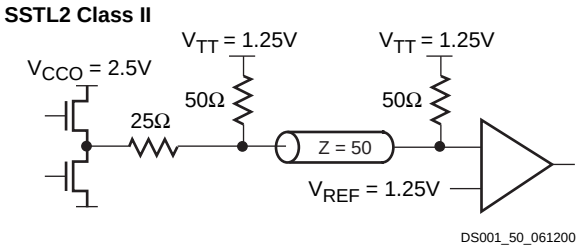


Figure 50: **Terminated SSTL2 Class II**

Table 28: **SSTL2_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \geq V_{REF} + 0.18$	1.33	1.43	$3.0^{(2)}$
$V_{IL} \leq V_{REF} - 0.18$	$-0.3^{(3)}$	1.07	1.17
$V_{OH} \geq V_{REF} + 0.8$	1.95	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T_J	Junction temperature(1)	Commercial	0	85	°C
		Industrial	–40	100	°C
V_{CCINT}	Supply voltage relative to GND(2,5)	Commercial	2.5 – 5%	2.5 + 5%	V
		Industrial	2.5 – 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND(3,5)	Commercial	1.4	3.6	V
		Industrial	1.4	3.6	V
T_{IN}	Input signal transition time(4)		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Functional operation is guaranteed down to a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} – 10%). For every 50 mV reduction in V_{CCINT} below 2.375V (nominal V_{CCINT} – 5%), all delay parameters increase by 3%.
3. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
4. Input and output measurement threshold is ~50% of V_{CCO}. See "Delay Measurement Methodology," page 60 for specific levels.
5. Supply voltages may be applied in any order desired.

DC Characteristics Over Operating Conditions

Symbol	Description			Min	Typ	Max	Units
V_{DRINT}	Data Retention V_{CCINT} voltage (below which configuration data may be lost)			2.0	-	-	V
V_{DRIO}	Data Retention V_{CCO} voltage (below which configuration data may be lost)			1.2	-	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XC2S15	Commercial	-	10	30	mA
			Industrial	-	10	60	mA
		XC2S30	Commercial	-	10	30	mA
			Industrial	-	10	60	mA
		XC2S50	Commercial	-	12	50	mA
			Industrial	-	12	100	mA
		XC2S100	Commercial	-	12	50	mA
			Industrial	-	12	100	mA
		XC2S150	Commercial	-	15	50	mA
			Industrial	-	15	100	mA
		XC2S200	Commercial	-	15	75	mA
			Industrial	-	15	150	mA
I_{CCOQ}	Quiescent V_{CCO} supply current(1)			-	-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin			-	-	20	µA
I_L	Input or output leakage current(2)			–10	-	+10	µA
C_{IN}	Input capacitance (sample tested)	VQ, CS, TQ, PQ, FG packages		-	-	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)(3)			-	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested)(3)			-	-	0.15	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. The I/O leakage current specification applies only when the V_{CCINT} and V_{CCO} supply voltages have reached their respective minimum Recommended Operating Conditions.
3. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.2	16.9	ns
T_{OLVTTL_S4}		4 mA	7.2	8.6	ns
T_{OLVTTL_S6}		6 mA	4.7	5.5	ns
T_{OLVTTL_S8}		8 mA	2.9	3.5	ns
T_{OLVTTL_S12}		12 mA	1.9	2.2	ns
T_{OLVTTL_S16}		16 mA	1.7	2.0	ns
T_{OLVTTL_S24}		24 mA	1.3	1.5	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	12.6	15.0	ns
T_{OLVTTL_F4}		4 mA	5.1	6.1	ns
T_{OLVTTL_F6}		6 mA	3.0	3.6	ns
T_{OLVTTL_F8}		8 mA	1.0	1.2	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.1	–0.1	ns
T_{OLVTTL_F24}		24 mA	–0.1	–0.2	ns
$T_{OLVCMOS2}$		LVCMOS2	0.2	0.2	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.4	2.9	ns
T_{OPCI33_5}		PCI, 33 MHz, 5.0V	2.9	3.5	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.3	–0.4	ns
T_{OGTL}		GTL	0.6	0.7	ns
T_{OGTLP}		GTL+	0.9	1.1	ns
T_{OHSTL_I}		HSTL I	–0.4	–0.5	ns
T_{OHSTL_III}		HSTL III	–0.8	–1.0	ns
T_{OHSTL_IV}		HSTL IV	–0.9	–1.1	ns
T_{OSSTL2_I}		SSTL2 I	–0.4	–0.5	ns
T_{OSSLT2_II}		SSTL2 II	–0.8	–1.0	ns
T_{OSSTL3_I}		SSTL3 I	–0.4	–0.5	ns
T_{OSSTL3_II}		SSTL3 II	–0.9	–1.1	ns
T_{OCTT}		CTT	–0.5	–0.6	ns
T_{OAGP}		AGP	–0.8	–1.0	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.

Clock Distribution Guidelines(1)

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
GCLK Clock Skew				
$T_{GSKEWIOB}$	Global clock skew between IOB flip-flops	0.13	0.14	ns

Notes:
1. These clock distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

T_{GPIO} is specified for LVTTL levels. For other standards, adjust T_{GPIO} with the values shown in "I/O Standard Global Clock Input Adjustments".

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
GCLK IOB and Buffer				
T_{GPIO}	Global clock pad to output	0.7	0.8	ns
T_{GIO}	Global clock buffer I input to O output	0.7	0.8	ns

I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Data Input Delay Adjustments					
$T_{GPLVTTL}$	Standard-specific global clock input delay adjustments	LVTTL	0	0	ns
$T_{GPLVCMOS2}$		LVCMOS2	–0.04	–0.05	ns
$T_{GPPCI33\_3}$		PCI, 33 MHz, 3.3V	–0.11	–0.13	ns
$T_{GPPCI33\_5}$		PCI, 33 MHz, 5.0V	0.26	0.30	ns
$T_{GPPCI66\_3}$		PCI, 66 MHz, 3.3V	–0.11	–0.13	ns
T_{GPGTL}		GTL	0.80	0.84	ns
T_{GPGTLP}		GTL+	0.71	0.73	ns
T_{GPHSTL}		HSTL	0.63	0.64	ns
$T_{GPSSTL2}$		SSTL2	0.52	0.51	ns
$T_{GPSSTL3}$		SSTL3	0.56	0.55	ns
T_{GPCTT}		CTT	0.62	0.62	ns
T_{GPAGP}		AGP	0.54	0.53	ns

Notes:
1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
$F_{CLKINHF}$	Input clock frequency (CLKDLLHF)	60	200	60	180	MHz
$F_{CLKINLF}$	Input clock frequency (CLKDLL)	25	100	25	90	MHz
$T_{DLLPWHF}$	Input clock pulse width (CLKDLLHF)	2.0	-	2.4	-	ns
$T_{DLLPWLF}$	Input clock pulse width (CLKDLL)	2.5	-	3.0	-	ns

DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

Figure 52, page 63, provides definitions for various parameters in the table below.

Symbol	Description	F_{CLKIN}	CLKDLLHF		CLKDLL		Units
			Min	Max	Min	Max	
T_{IPTOL}	Input clock period tolerance		-	1.0	-	1.0	ns
T_{IJITCC}	Input clock jitter tolerance (cycle-to-cycle)		-	±150	-	±300	ps
T_{LOCK}	Time required for DLL to acquire lock	> 60 MHz	-	20	-	20	µs
		50-60 MHz	-	-	-	25	µs
		40-50 MHz	-	-	-	50	µs
		30-40 MHz	-	-	-	90	µs
		25-30 MHz	-	-	-	120	µs
T_{OJITCC}	Output jitter (cycle-to-cycle) for any DLL clock output(1)		-	±60	-	±60	ps
T_{PHIO}	Phase offset between CLKIN and CLKO(2)		-	±100	-	±100	ps
T_{PHOO}	Phase offset between clock outputs on the DLL(3)		-	±140	-	±140	ps
T_{PHIOM}	Maximum phase difference between CLKIN and CLKO(4)		-	±160	-	±160	ps
T_{PHOOM}	Maximum phase difference between clock outputs on the DLL(5)		-	±200	-	±200	ps

Notes:

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

Pinout Tables

The following device-specific pinout tables include all packages available for each Spartan®-II device. They follow the pad locations around the die, and include Boundary Scan register locations.

XC2S15 Device Pinouts

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
GND	-	P1	P143	A1	-
TMS	-	P2	P142	B1	-
I/O	7	P3	P141	C2	77
I/O	7	-	P140	C1	80
I/O, V_{REF}	7	P4	P139	D4	83
I/O	7	P5	P137	D2	86
I/O	7	P6	P136	D1	89
GND	-	-	P135	E4	-
I/O	7	P7	P134	E3	92
I/O	7	-	P133	E2	95
I/O, V_{REF}	7	P8	P132	E1	98
I/O	7	P9	P131	F4	101
I/O	7	-	P130	F3	104
I/O, IRDY(1)	7	P10	P129	F2	107
GND	-	P11	P128	F1	-
V_{CCO}	7	P12	P127	G2	-
V_{CCO}	6	P12	P127	G2	-
I/O, TRDY(1)	6	P13	P126	G1	110
V_{CCINT}	-	P14	P125	G3	-
I/O	6	-	P124	G4	113
I/O	6	P15	P123	H1	116
I/O, V_{REF}	6	P16	P122	H2	119
I/O	6	-	P121	H3	122
I/O	6	P17	P120	H4	125
GND	-	-	P119	J1	-
I/O	6	P18	P118	J2	128
I/O	6	P19	P117	J3	131
I/O, V_{REF}	6	P20	P115	K1	134
I/O	6	-	P114	K2	137
I/O	6	P21	P113	K3	140
I/O	6	P22	P112	L1	143
M1	-	P23	P111	L2	146
GND	-	P24	P110	L3	-
M0	-	P25	P109	M1	147
V_{CCO}	6	P26	P108	M2	-
V_{CCO}	5	P26	P107	N1	-

XC2S15 Device Pinouts *(Continued)*

XC2S15 Pad Name		VQ100	TQ144	CS144	Bndry Scan
Function	Bank				
M2	-	P27	P106	N2	148
I/O	5	-	P103	K4	155
I/O, V_{REF}	5	P30	P102	L4	158
I/O	5	P31	P100	N4	161
I/O	5	P32	P99	K5	164
GND	-	-	P98	L5	-
V_{CCINT}	-	P33	P97	M5	-
I/O	5	-	P96	N5	167
I/O	5	-	P95	K6	170
I/O, V_{REF}	5	P34	P94	L6	173
I/O	5	-	P93	M6	176
V_{CCINT}	-	P35	P92	N6	-
I, GCK1	5	P36	P91	M7	185
V_{CCO}	5	P37	P90	N7	-
V_{CCO}	4	P37	P90	N7	-
GND	-	P38	P89	L7	-
I, GCK0	4	P39	P88	K7	186
I/O	4	P40	P87	N8	190
I/O	4	-	P86	M8	193
I/O, V_{REF}	4	P41	P85	L8	196
I/O	4	-	P84	K8	199
I/O	4	-	P83	N9	202
V_{CCINT}	-	P42	P82	M9	-
GND	-	-	P81	L9	-
I/O	4	P43	P80	K9	205
I/O	4	P44	P79	N10	208
I/O, V_{REF}	4	P45	P77	L10	211
I/O	4	-	P76	N11	214
I/O	4	P46	P75	M11	217
I/O	4	P47	P74	L11	220
GND	-	P48	P73	N12	-
DONE	3	P49	P72	M12	223
V_{CCO}	4	P50	P71	N13	-
V_{CCO}	3	P50	P70	M13	-
$\overline{PROGRAM}$	-	P51	P69	L12	226
I/O ($\overline{INIT}$)	3	P52	P68	L13	227
I/O (D7)	3	P53	P67	K10	230
I/O	3	-	P66	K11	233
I/O, V_{REF}	3	P54	P65	K12	236
I/O	3	P55	P63	J10	239
I/O (D6)	3	P56	P62	J11	242

XC2S30 Device Pinouts

XC2S30 Pad Name						
Function	Bank	VQ100	TQ144	CS144	PQ208	Bndry Scan
GND	-	P1	P143	A1	P1	-
TMS	-	P2	P142	B1	P2	-
I/O	7	P3	P141	C2	P3	113
I/O	7	-	P140	C1	P4	116
I/O	7	-	-	-	P5	119
I/O, V_{REF}	7	P4	P139	D4	P6	122
I/O	7	-	P138	D3	P8	125
I/O	7	P5	P137	D2	P9	128
I/O	7	P6	P136	D1	P10	131
GND	-	-	P135	E4	P11	-
V_{CCO}	7	-	-	-	P12	-
I/O	7	P7	P134	E3	P14	134
I/O	7	-	P133	E2	P15	137
I/O	7	-	-	-	P16	140
I/O	7	-	-	-	P17	143
I/O	7	-	-	-	P18	146
GND	-	-	-	-	P19	-
I/O, V_{REF}	7	P8	P132	E1	P20	149
I/O	7	P9	P131	F4	P21	152
I/O	7	-	P130	F3	P22	155
I/O	7	-	-	-	P23	158
I/O, IRDY(1)	7	P10	P129	F2	P24	161
GND	-	P11	P128	F1	P25	-
V_{CCO}	7	P12	P127	G2	P26	-
V_{CCO}	6	P12	P127	G2	P26	-
I/O, TRDY(1)	6	P13	P126	G1	P27	164
V_{CCINT}	-	P14	P125	G3	P28	-
I/O	6	-	P124	G4	P29	170
I/O	6	P15	P123	H1	P30	173
I/O, V_{REF}	6	P16	P122	H2	P31	176
GND	-	-	-	-	P32	-
I/O	6	-	-	-	P33	179
I/O	6	-	-	-	P34	182
I/O	6	-	-	-	P35	185
I/O	6	-	P121	H3	P36	188
I/O	6	P17	P120	H4	P37	191
V_{CCO}	6	-	-	-	P39	-
GND	-	-	P119	J1	P40	-
I/O	6	P18	P118	J2	P41	194
I/O	6	P19	P117	J3	P42	197
I/O	6	-	P116	J4	P43	200

XC2S30 Device Pinouts *(Continued)*

XC2S30 Pad Name						
Function	Bank	VQ100	TQ144	CS144	PQ208	Bndry Scan
I/O, V_{REF}	6	P20	P115	K1	P45	203
I/O	6	-	-	-	P46	206
I/O	6	-	P114	K2	P47	209
I/O	6	P21	P113	K3	P48	212
I/O	6	P22	P112	L1	P49	215
M1	-	P23	P111	L2	P50	218
GND	-	P24	P110	L3	P51	-
M0	-	P25	P109	M1	P52	219
V_{CCO}	6	P26	P108	M2	P53	-
V_{CCO}	5	P26	P107	N1	P53	-
M2	-	P27	P106	N2	P54	220
I/O	5	-	P103	K4	P57	227
I/O	5	-	-	-	P58	230
I/O, V_{REF}	5	P30	P102	L4	P59	233
I/O	5	-	P101	M4	P61	236
I/O	5	P31	P100	N4	P62	239
I/O	5	P32	P99	K5	P63	242
GND	-	-	P98	L5	P64	-
V_{CCO}	5	-	-	-	P65	-
V_{CCINT}	-	P33	P97	M5	P66	-
I/O	5	-	P96	N5	P67	245
I/O	5	-	P95	K6	P68	248
I/O	5	-	-	-	P69	251
I/O	5	-	-	-	P70	254
I/O	5	-	-	-	P71	257
GND	-	-	-	-	P72	-
I/O, V_{REF}	5	P34	P94	L6	P73	260
I/O	5	-	-	-	P74	263
I/O	5	-	P93	M6	P75	266
V_{CCINT}	-	P35	P92	N6	P76	-
I, GCK1	5	P36	P91	M7	P77	275
V_{CCO}	5	P37	P90	N7	P78	-
V_{CCO}	4	P37	P90	N7	P78	-
GND	-	P38	P89	L7	P79	-
I, GCK0	4	P39	P88	K7	P80	276
I/O	4	P40	P87	N8	P81	280
I/O	4	-	P86	M8	P82	283
I/O	4	-	-	-	P83	286
I/O, V_{REF}	4	P41	P85	L8	P84	289
GND	-	-	-	-	P85	-
I/O	4	-	-	-	P86	292

Additional XC2S100 Package Pins

TQ144

Not Connected Pins					
P104	P105	-	-	-	-

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PQ208

Not Connected Pins					
P55	P56	-	-	-	-

11/02/00

FG256

V_{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V_{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V_{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V_{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V_{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V_{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V_{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V_{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V_{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

11/02/00

FG456

V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					

Additional XC2S100 Package Pins *(Continued)*

F10	F7	F8	F9	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U10	U7	U8	U9
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A4	A5	A6	A12	A13
A14	A15	A17	B3	B6	B8
B11	B14	B16	B19	C1	C2
C8	C9	C12	C18	C22	D1
D4	D5	D10	D18	D19	D21
E4	E11	E13	E15	E16	E17
E19	E22	F4	F11	F22	G2
G3	G4	G19	G22	H1	H21
J1	J3	J4	J19	J20	K2
K18	K19	L2	L5	L18	L19
M2	M6	M17	M18	M21	N1
N5	N19	P1	P5	P19	P22
R1	R3	R20	R22	T5	T19
U3	U11	U18	V1	V2	V10
V12	V17	V3	V4	V6	V8
V20	V21	V22	W4	W5	W9
W13	W14	W15	W16	W19	Y5
Y14	Y18	Y22	AA1	AA3	AA6
AA9	AA10	AA11	AA16	AA17	AA18
AA22	AB3	AB4	AB7	AB8	AB12
AB14	AB21	-	-	-	-

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XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	1	P174	B10	C14	72
I/O	1	-	-	B14	75
I/O	1	P175	D10	D13	81
I/O	1	P176	A10	C13	84
GND	-	P177	GND*	GND*	-
V_{CCO}	1	-	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
I/O, V_{REF}	1	P178	B9	B13	87
I/O	1	P179	E10	E12	90
I/O	1	-	A9	B12	93
I/O	1	P180	D9	D12	96
I/O	1	-	-	C12	99
I/O	1	P181	A8	D11	102
I, GCK2	1	P182	C9	A11	108
GND	-	P183	GND*	GND*	-
V_{CCO}	1	P184	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
V_{CCO}	0	P184	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
I, GCK3	0	P185	B8	C11	109
V_{CCINT}	-	P186	V_{CCINT}*	V_{CCINT}*	-
I/O	0	-	-	E11	116
I/O	0	P187	A7	A10	119
I/O	0	-	D8	B10	122
I/O	0	P188	A6	C10	125
I/O, V_{REF}	0	P189	B7	A9	128
V_{CCO}	0	-	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
GND	-	P190	GND*	GND*	-
I/O	0	P191	C8	B9	131
I/O	0	P192	D7	E10	134
I/O	0	-	-	D10	140
I/O	0	P193	E7	A8	143
I/O	0	-	-	D9	146
I/O	0	-	-	B8	149
I/O	0	P194	C7	E9	155
I/O	0	P195	B6	A7	158

XC2S150 Device Pinouts *(Continued)*

XC2S150 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V_{CCINT}	-	P196	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	0	P197	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
GND	-	P198	GND*	GND*	-
I/O	0	P199	A5	B7	161
I/O, V_{REF}	0	P200	C6	E8	164
I/O	0	-	-	D8	167
I/O	0	P201	B5	C7	170
I/O	0	-	D6	D7	173
I/O	0	-	-	B6	176
I/O	0	-	-	A5	179
I/O	0	P202	A4	D6	182
I/O, V_{REF}	0	P203	B4	C6	185
V_{CCO}	0	-	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
GND	-	-	GND*	GND*	-
I/O	0	P204	E6	B5	188
I/O	0	-	D5	E7	191
I/O	0	-	-	A4	194
I/O	0	-	-	E6	197
I/O	0	P205	A3	B4	200
GND	-	-	GND*	GND*	-
I/O	0	-	C5	A3	203
I/O	0	-	-	B3	206
I/O	0	-	-	D5	209
I/O	0	P206	B3	C5	212
TCK	-	P207	C4	C4	-
V_{CCO}	0	P208	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
V_{CCO}	7	P208	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-

04/18/01

Notes:

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S150 Package Pins

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

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FG256

V_{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V_{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V_{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V_{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V_{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V_{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V_{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V_{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V_{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

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Additional XC2S150 Package Pins *(Continued)*

FG456

V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					
F7	F8	F9	F10	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U7	U8	U9	U10
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A6	A12	A13	A14	B11
B16	C2	C8	C9	D1	D4
D18	D19	E13	E17	E19	F11
G2	G22	H21	J1	J4	K2
K18	K19	L2	L19	M2	M17
M21	N1	P1	P5	P22	R3
R20	R22	U3	U18	V6	W4
W13	W15	W19	Y5	Y22	AA1
AA3	AA9	AA10	AA11	AA16	AB7
AB8	AB12	AB14	AB21	-	-

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XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	6	-	-	T2	449
I/O	6	P43	L4	U1	452
GND	-	-	GND*	GND*	-
I/O	6	-	M2	R5	455
I/O	6	-	-	V1	458
I/O	6	-	-	T5	461
I/O	6	P44	L3	U2	464
I/O, V_{REF}	6	P45	N1	T3	467
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-
I/O	6	P46	P1	T4	470
I/O	6	-	L5	W1	473
GND	-	-	GND*	GND*	-
I/O	6	-	-	V2	476
I/O	6	-	-	U4	482
I/O, V_{REF}	6	P47	N2	Y1	485
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	488
I/O	6	-	-	V3	491
I/O	6	-	-	V4	494
I/O	6	P48	R1	Y2	500
I/O	6	P49	M3	W3	503
M1	-	P50	P2	U5	506
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	507
V_{CCO}	6	P53	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
V_{CCO}	5	P53	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
M2	-	P54	R3	Y4	508
I/O	5	-	-	W5	518
I/O	5	-	-	AB3	521
I/O	5	-	N5	V7	524
GND	-	-	GND*	GND*	-
I/O, V_{REF}	5	P57	T2	Y6	527
I/O	5	-	-	AA4	530
I/O	5	-	-	AB4	536
I/O	5	-	P5	W6	539
I/O	5	P58	T3	Y7	542
GND	-	-	GND*	GND*	-

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P59	T4	AA5	545
I/O	5	P60	M6	AB5	548
I/O	5	-	-	V8	551
I/O	5	-	-	AA6	554
I/O	5	-	T5	AB6	557
GND	-	-	GND*	GND*	-
I/O	5	P61	N6	AA7	560
I/O	5	-	-	W7	563
I/O, V_{REF}	5	P62	R5	W8	569
I/O	5	P63	P6	Y8	572
GND	-	P64	GND*	GND*	-
V_{CCO}	5	P65	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCINT}	-	P66	V_{CCINT}*	V_{CCINT}*	-
I/O	5	P67	R6	AA8	575
I/O	5	P68	M7	V9	578
I/O	5	-	-	AB8	581
I/O	5	-	-	W9	584
I/O	5	-	-	AB9	587
GND	-	-	GND*	GND*	-
I/O	5	P69	N7	Y9	590
I/O	5	-	-	V10	593
I/O	5	-	-	AA9	596
I/O	5	P70	T6	W10	599
I/O	5	P71	P7	AB10	602
GND	-	P72	GND*	GND*	-
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P73	P8	Y10	605
I/O	5	P74	R7	V11	608
I/O	5	-	-	AA10	614
I/O	5	-	T7	W11	617
I/O	5	P75	T8	AB11	620
I/O	5	-	-	U11	623
V_{CCINT}	-	P76	V_{CCINT}*	V_{CCINT}*	-
I, GCK1	5	P77	R8	Y11	635
V_{CCO}	5	P78	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCO}	4	P78	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-