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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 972 |
| Total RAM Bits | 24576 |
| Number of I/O | 60 |
| Number of Gates | 30000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-VQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s30-5vqg100i |

## Spartan-II Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination. The four global clock pins are usable as additional user I/Os when not used as a global clock pin. These pins are not included in user I/O counts.

*Table 2:* **Spartan-II FPGA User I/O Chart(1)**

| Device | Maximum User I/O | Available User I/O According to Package Type | | | | | |
|---|---|---|---|---|---|---|---|
| | | VQ100 VQG100 | TQ144 TQG144 | CS144 CSG144 | PQ208 PQG208 | FG256 FGG256 | FG456 FGG456 |
| XC2S15 | 86 | 60 | 86 | (Note 2) | - | - | - |
| XC2S30 | 92 | 60 | 92 | 92 | (Note 2) | - | - |
| XC2S50 | 176 | - | 92 | - | 140 | 176 | - |
| XC2S100 | 176 | - | 92 | - | 140 | 176 | (Note 2) |
| XC2S150 | 260 | - | - | - | 140 | 176 | 260 |
| XC2S200 | 284 | - | - | - | 140 | 176 | 284 |

**Notes:**
1. All user I/O counts do not include the four global clock/user input pins.
2. Discontinued by PDN2004-01.

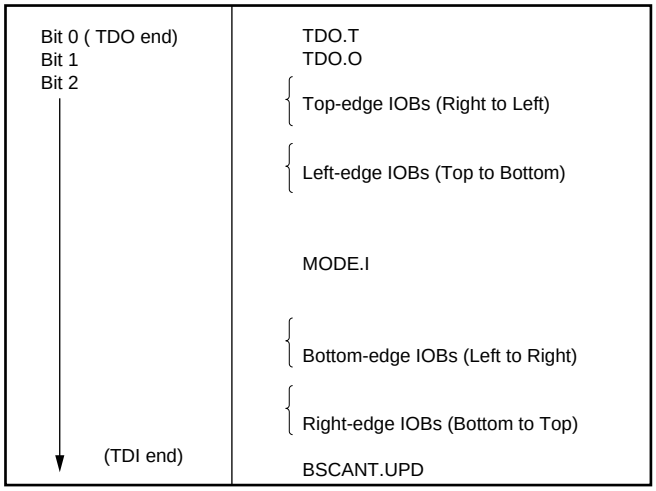



*Figure 10:* **Boundary Scan Bit Sequence**

## Development System

Spartan-II FPGAs are supported by the Xilinx ISE® development tools. The basic methodology for Spartan-II FPGA design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation, while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under a single graphical interface, providing designers with a common user interface regardless of their choice of entry and verification tools. The software simplifies the selection of implementation options with pull-down menus and on-line help.

For HDL design entry, the Xilinx FPGA development system provides interfaces to several synthesis design environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-II FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The design environment supports hierarchical design entry. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

### Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

### Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, the development system includes a download cable, which connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can read back the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

## Signals

There are two kinds of pins that are used to configure Spartan-II devices: Dedicated pins perform only specific configuration-related functions; the other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{PROGRAM}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a $V_{CCO}$ of 3.3V to drive an LVTTL signal or 2.5V to drive an LVCMOS signal. All the relevant pins fall in banks 2 or 3. The $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$ pins for Slave Parallel mode are located in bank 1.

For a more detailed description than that given below, see "Pinout Tables" in Module 4 and XAPP176, *Spartan-II FPGA Series Configuration and Readback*.

## The Process

The sequence of steps necessary to configure Spartan-II devices are shown in Figure 11. The overall flow can be divided into three different phases.

- Initiating Configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

### *Initiating Configuration*

There are two different ways to initiate the configuration process: applying power to the device or asserting the $\overline{\text{PROGRAM}}$ input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown in Figure 12, page 19. Before configuration can begin, $V_{CCO}$ Bank 2 must be greater than 1.0V. Furthermore, all $V_{CCINT}$ power pins must be connected to a 2.5V supply. For more information on delaying configuration, see "Clearing Configuration Memory," page 19.

Once in user operation, the device can be re-configured simply by pulling the $\overline{\text{PROGRAM}}$ pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase.

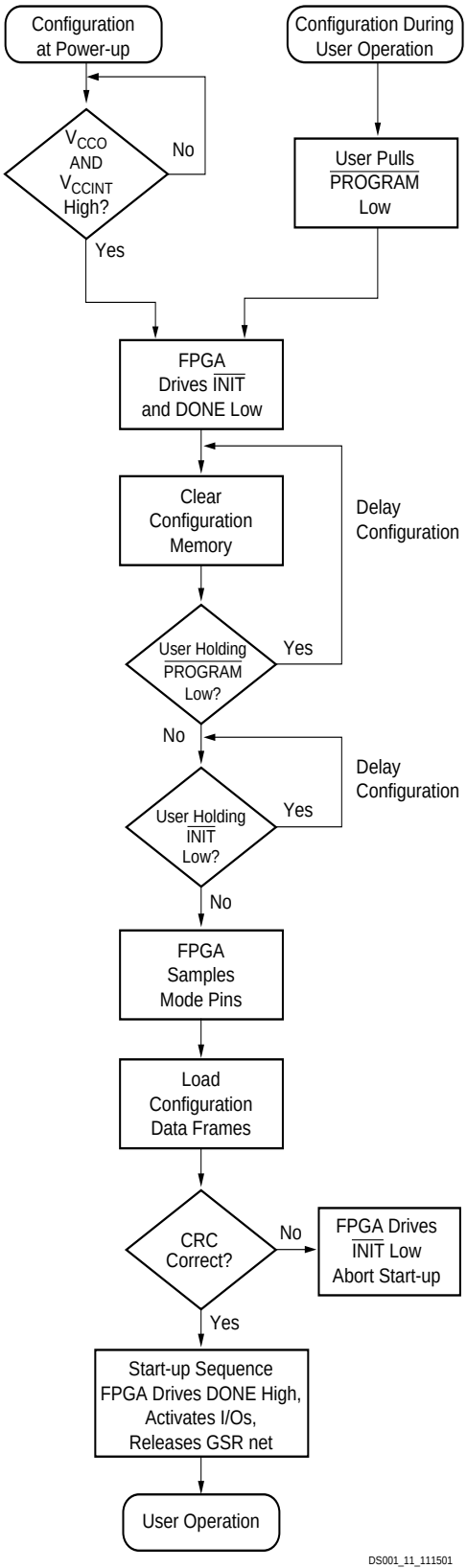
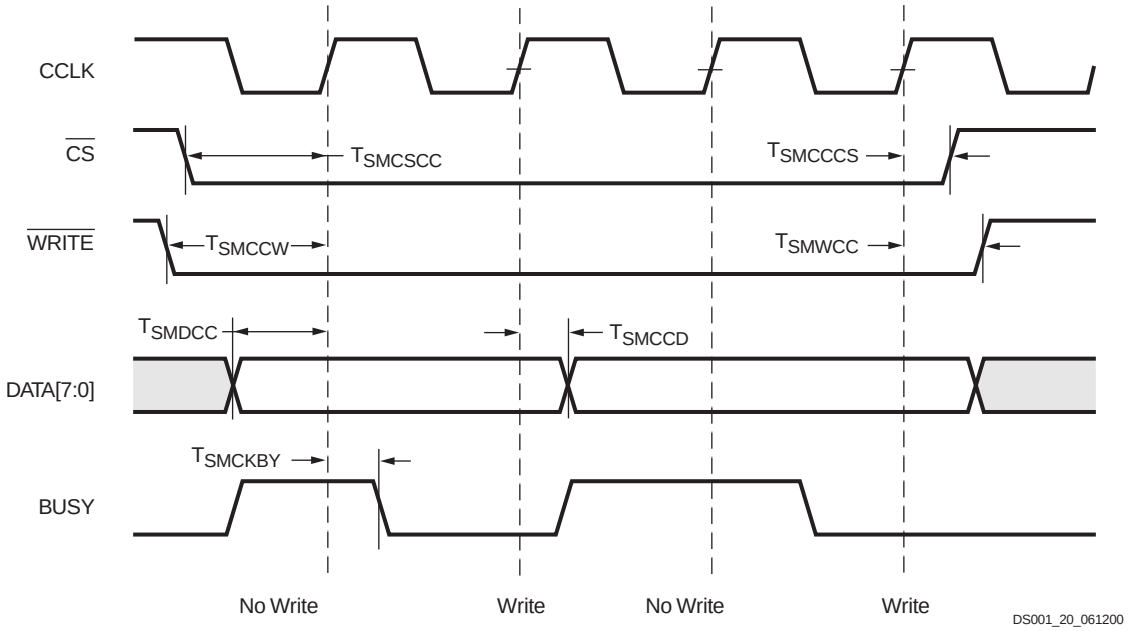



*Figure 11:* **Configuration Flow Diagram**




| Symbol | | Description | | Units |
|---|---|---|---|---|
| $T_{SMDCC}$ | CCLK | D0-D7 setup/hold | 5 | ns, min |
| $T_{SMCCD}$ | | D0-D7 hold | 0 | ns, min |
| $T_{SMCSCC}$ | | $\overline{CS}$ setup | 7 | ns, min |
| $T_{SMCCCS}$ | | $\overline{CS}$ hold | 0 | ns, min |
| $T_{SMCCW}$ | | $\overline{WRITE}$ setup | 7 | ns, min |
| $T_{SMWCC}$ | | $\overline{WRITE}$ hold | 0 | ns, min |
| $T_{SMCKBY}$ | | BUSY propagation delay | 12 | ns, max |
| $F_{CC}$ | | Maximum frequency | 66 | MHz, max |
| $F_{CCNH}$ | | Maximum frequency with no handshake | 50 | MHz, max |

*Figure 20:* **Slave Parallel Write Timing**

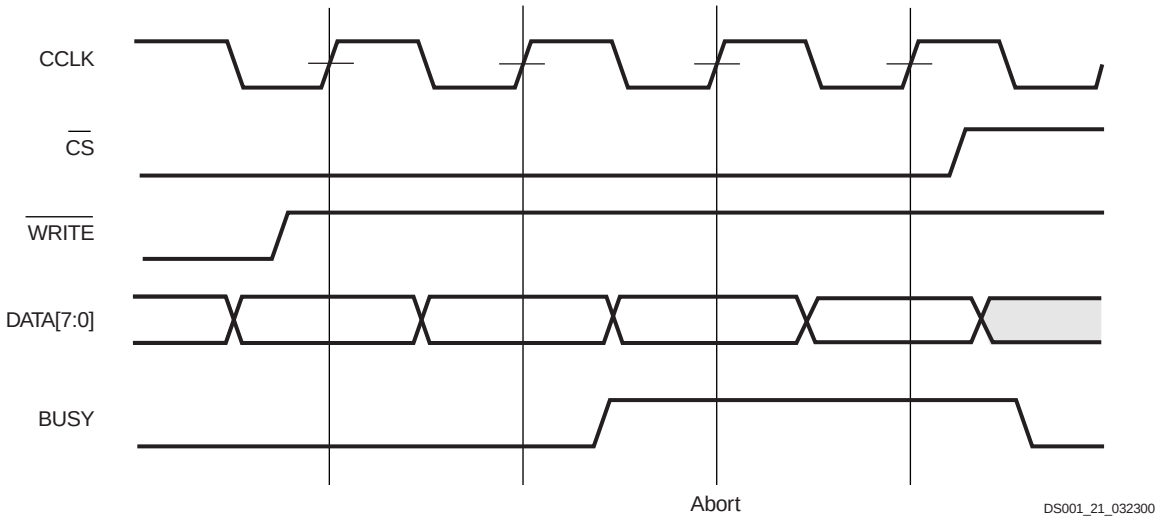



*Figure 21:* **Slave Parallel Write Abort Waveforms**

At the third rising edge of CLKA, the $T_{BCCS}$ parameter is violated with two writes to memory location 0x0F. The DOA and DOB busses reflect the contents of the DIA and DIB busses, but the stored value at 0x7E is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the $T_{BCCS}$ parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

### Initialization

The block RAM memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 14. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

### Initialization in VHDL

The block RAM structures may be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization.

### Initialization in Verilog

The block RAM structures may be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization.

### Block Memory Generation

The CORE Generator™ software generates memory structures using the block RAM features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

*Table 14:* **RAM Initialization Properties**

| Property | Memory Cells |
|---|---|
| INIT_00 | 255 to 0 |
| INIT_01 | 511 to 256 |
| INIT_02 | 767 to 512 |
| INIT_03 | 1023 to 768 |
| INIT_04 | 1279 to 1024 |
| INIT_05 | 1535 to 1280 |
| INIT_06 | 1791 to 1536 |
| INIT_07 | 2047 to 1792 |
| INIT_08 | 2303 to 2048 |
| INIT_09 | 2559 to 2304 |
| INIT_0a | 2815 to 2560 |
| INIT_0b | 3071 to 2816 |
| INIT_0c | 3327 to 3072 |
| INIT_0d | 3583 to 3328 |
| INIT_0e | 3839 to 3584 |
| INIT_0f | 4095 to 3840 |

For design examples and more information on using the Block RAM, see XAPP173, *Using Block SelectRAM+ Memory in Spartan-II FPGAs*.

## Using Versatile I/O

The Spartan-II FPGA family includes a highly configurable, high-performance I/O resource called Versatile I/O to provide support for a wide variety of I/O standards. The Versatile I/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and Versatile I/O features and the design considerations described in this document can improve and simplify system level design.

### Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high-performance I/O becomes more important. While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. Versatile I/O, the revolutionary input/output resources of Spartan-II devices, has resolved this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. The Spartan-II FPGA Versatile I/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each Versatile I/O block can support up to 16 I/O standards. Supporting such a variety of I/O standards allows the

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

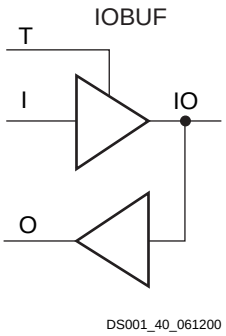



*Figure 40:* **Input/Output Buffer Primitiveprimitive (IOBUF)**

When the IOBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the $V_{CCO}$ for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard ($V_{CCO}$ < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 36, page 39 for a representation of the Spartan-II FPGA I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given $V_{CCO}$ bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

## Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

### *Input Delay Properties*

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

### *IOB Flip-Flop/Latch Property*

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified:

map -pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

### *Location Constraints*

Specify the location of each Versatile I/O primitive with the location constraint LOC attached to the Versatile I/O primitive. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

LOC=A42

LOC=P37

### *Output Slew Rate Property*

In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

### *Output Drive Strength Property*

For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE=

### HSTL Class III

A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 45. DC voltage specifications appear in Table 23 for the HSTL_III standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

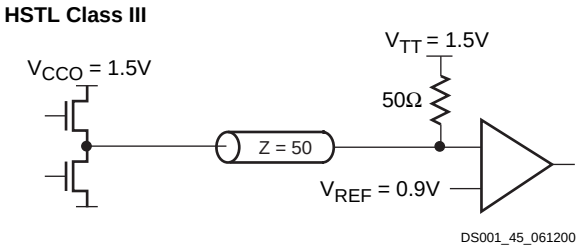



*Figure 45:* **Terminated HSTL Class III**

*Table 23:* **HSTL Class III Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ (1) | - | 0.90 | - |
| $V_{TT}$ | - | $V_{CCO}$ | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 | - | - |

**Notes:**

1. Per EIA/JESD8-6, "The value of $V_{REF}$ is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

### HSTL Class IV

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 46.DC voltage specifications appear in Table 23 for the HSTL_IV standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

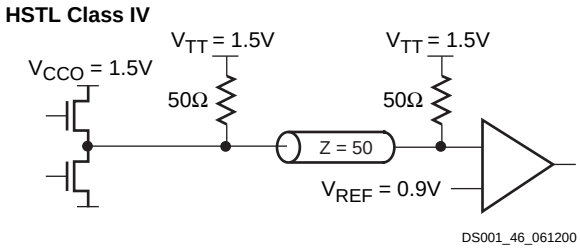



*Figure 46:* **Terminated HSTL Class IV**

*Table 24:* **HSTL Class IV Voltage Specification**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.40 | 1.50 | 1.60 |
| $V_{REF}$ | - | 0.90 | - |
| $V_{TT}$ | - | $V_{CCO}$ | - |
| $V_{IH}$ | $V_{REF}$ + 0.1 | - | - |
| $V_{IL}$ | - | - | $V_{REF}$ – 0.1 |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 48 | - | - |

**Notes:**

1. Per EIA/JESD8-6, "The value of $V_{REF}$ is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

## IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol | Description | Standard | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -6 | -5 | |
| **Output Delay Adjustments (Adj)** | | | | | |
| $T_{OLVTTL\_S2}$ | Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, $C_{SL}$) | LVTTL, Slow, 2 mA | 14.2 | 16.9 | ns |
| $T_{OLVTTL\_S4}$ | | 4 mA | 7.2 | 8.6 | ns |
| $T_{OLVTTL\_S6}$ | | 6 mA | 4.7 | 5.5 | ns |
| $T_{OLVTTL\_S8}$ | | 8 mA | 2.9 | 3.5 | ns |
| $T_{OLVTTL\_S12}$ | | 12 mA | 1.9 | 2.2 | ns |
| $T_{OLVTTL\_S16}$ | | 16 mA | 1.7 | 2.0 | ns |
| $T_{OLVTTL\_S24}$ | | 24 mA | 1.3 | 1.5 | ns |
| $T_{OLVTTL\_F2}$ | | LVTTL, Fast, 2 mA | 12.6 | 15.0 | ns |
| $T_{OLVTTL\_F4}$ | | 4 mA | 5.1 | 6.1 | ns |
| $T_{OLVTTL\_F6}$ | | 6 mA | 3.0 | 3.6 | ns |
| $T_{OLVTTL\_F8}$ | | 8 mA | 1.0 | 1.2 | ns |
| $T_{OLVTTL\_F12}$ | | 12 mA | 0 | 0 | ns |
| $T_{OLVTTL\_F16}$ | | 16 mA | –0.1 | –0.1 | ns |
| $T_{OLVTTL\_F24}$ | | 24 mA | –0.1 | –0.2 | ns |
| $T_{OLVCMOS2}$ | | LVCMOS2 | 0.2 | 0.2 | ns |
| $T_{OPCI33\_3}$ | | PCI, 33 MHz, 3.3V | 2.4 | 2.9 | ns |
| $T_{OPCI33\_5}$ | | PCI, 33 MHz, 5.0V | 2.9 | 3.5 | ns |
| $T_{OPCI66\_3}$ | | PCI, 66 MHz, 3.3V | –0.3 | –0.4 | ns |
| $T_{OGTL}$ | | GTL | 0.6 | 0.7 | ns |
| $T_{OGTLP}$ | | GTL+ | 0.9 | 1.1 | ns |
| $T_{OHSTL\_I}$ | | HSTL I | –0.4 | –0.5 | ns |
| $T_{OHSTL\_III}$ | | HSTL III | –0.8 | –1.0 | ns |
| $T_{OHSTL\_IV}$ | | HSTL IV | –0.9 | –1.1 | ns |
| $T_{OSSTL2\_I}$ | | SSTL2 I | –0.4 | –0.5 | ns |
| $T_{OSSLT2\_II}$ | | SSTL2 II | –0.8 | –1.0 | ns |
| $T_{OSSTL3\_I}$ | | SSTL3 I | –0.4 | –0.5 | ns |
| $T_{OSSTL3\_II}$ | | SSTL3 II | –0.9 | –1.1 | ns |
| $T_{OCTT}$ | | CTT | –0.5 | –0.6 | ns |
| $T_{OAGP}$ | | AGP | –0.8 | –1.0 | ns |

**Notes:**

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.

## Calculation of $T_{IOOP}$ as a Function of Capacitance

$T_{IOOP}$ is the propagation delay from the O Input of the IOB to the pad. The values for $T_{IOOP}$ are based on the standard capacitive load ($C_{SL}$) for each I/O standard as listed in the table "Constants for Calculating TIOOP", below.

For other capacitive loads, use the formulas below to calculate an adjusted propagation delay, $T_{IOOP1}$.

$$T_{IOOP1} = T_{IOOP} + Adj + (C_{LOAD} - C_{SL}) * F_L$$

Where:

- Adj is selected from "IOB Output Delay Adjustments for Different Standards", page 59, according to the I/O standard used
- $C_{LOAD}$ is the capacitive load for the design
- $F_L$ is the capacitance scaling factor

## Delay Measurement Methodology

| Standard | $V_L$ (1) | $V_H$ (1) | Meas. Point | $V_{REF}$ Typ (2) |
|---|---|---|---|---|
| LVTTL | 0 | 3 | 1.4 | - |
| LVCMOS2 | 0 | 2.5 | 1.125 | - |
| PCI33_5 | Per PCI Spec | | | - |
| PCI33_3 | Per PCI Spec | | | - |
| PCI66_3 | Per PCI Spec | | | - |
| GTL | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 0.80 |
| GTL+ | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 1.0 |
| HSTL Class I | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.75 |
| HSTL Class III | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| HSTL Class IV | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.90 |
| SSTL3 I and II | $V_{REF}$ – 1.0 | $V_{REF}$ + 1.0 | $V_{REF}$ | 1.5 |
| SSTL2 I and II | $V_{REF}$ – 0.75 | $V_{REF}$ + 0.75 | $V_{REF}$ | 1.25 |
| CTT | $V_{REF}$ – 0.2 | $V_{REF}$ + 0.2 | $V_{REF}$ | 1.5 |
| AGP | $V_{REF}$ – (0.2x$V_{CCO}$) | $V_{REF}$ + (0.2x$V_{CCO}$) | $V_{REF}$ | Per AGP Spec |

**Notes:**
1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at $V_{REF}$ Typ, Maximum, and Minimum. Worst-case values are reported.
3. I/O parameter measurements are made with the capacitance values shown in the table, "Constants for Calculating TIOOP". See Xilinx application note XAPP179 for the appropriate terminations.
4. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## Constants for Calculating $T_{IOOP}$

| Standard | $C_{SL}$ (1) (pF) | $F_L$ (ns/pF) |
|---|---|---|
| LVTTL Fast Slew Rate, 2 mA drive | 35 | 0.41 |
| LVTTL Fast Slew Rate, 4 mA drive | 35 | 0.20 |
| LVTTL Fast Slew Rate, 6 mA drive | 35 | 0.13 |
| LVTTL Fast Slew Rate, 8 mA drive | 35 | 0.079 |
| LVTTL Fast Slew Rate, 12 mA drive | 35 | 0.044 |
| LVTTL Fast Slew Rate, 16 mA drive | 35 | 0.043 |
| LVTTL Fast Slew Rate, 24 mA drive | 35 | 0.033 |
| LVTTL Slow Slew Rate, 2 mA drive | 35 | 0.41 |
| LVTTL Slow Slew Rate, 4 mA drive | 35 | 0.20 |
| LVTTL Slow Slew Rate, 6 mA drive | 35 | 0.100 |
| LVTTL Slow Slew Rate, 8 mA drive | 35 | 0.086 |
| LVTTL Slow Slew Rate, 12 mA drive | 35 | 0.058 |
| LVTTL Slow Slew Rate, 16 mA drive | 35 | 0.050 |
| LVTTL Slow Slew Rate, 24 mA drive | 35 | 0.048 |
| LVCMOS2 | 35 | 0.041 |
| PCI 33 MHz 5V | 50 | 0.050 |
| PCI 33 MHZ 3.3V | 10 | 0.050 |
| PCI 66 MHz 3.3V | 10 | 0.033 |
| GTL | 0 | 0.014 |
| GTL+ | 0 | 0.017 |
| HSTL Class I | 20 | 0.022 |
| HSTL Class III | 20 | 0.016 |
| HSTL Class IV | 20 | 0.014 |
| SSTL2 Class I | 30 | 0.028 |
| SSTL2 Class II | 30 | 0.016 |
| SSTL3 Class I | 30 | 0.029 |
| SSTL3 Class II | 30 | 0.016 |
| CTT | 20 | 0.035 |
| AGP | 10 | 0.037 |

**Notes:**
1. I/O parameter measurements are made with the capacitance values shown above. See Xilinx application note XAPP179 for the appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| **Combinatorial Delays** | | | | | | |
| $T_{ILO}$ | 4-input function: F/G inputs to X/Y outputs | - | 0.6 | - | 0.7 | ns |
| $T_{IF5}$ | 5-input function: F/G inputs to F5 output | - | 0.7 | - | 0.9 | ns |
| $T_{IF5X}$ | 5-input function: F/G inputs to X output | - | 0.9 | - | 1.1 | ns |
| $T_{IF6Y}$ | 6-input function: F/G inputs to Y output via F6 MUX | - | 1.0 | - | 1.1 | ns |
| $T_{F5INY}$ | 6-input function: F5IN input to Y output | - | 0.4 | - | 0.4 | ns |
| $T_{IFNCTL}$ | Incremental delay routing through transparent latch to XQ/YQ outputs | - | 0.7 | - | 0.9 | ns |
| $T_{BYYB}$ | BY input to YB output | - | 0.6 | - | 0.7 | ns |
| **Sequential Delays** | | | | | | |
| $T_{CKO}$ | FF clock CLK to XQ/YQ outputs | - | 1.1 | - | 1.3 | ns |
| $T_{CKLO}$ | Latch clock CLK to XQ/YQ outputs | - | 1.2 | - | 1.5 | ns |
| **Setup/Hold Times with Respect to Clock CLK (1)** | | | | | | |
| $T_{ICK}$ / $T_{CKI}$ | 4-input function: F/G inputs | 1.3 / 0 | - | 1.4 / 0 | - | ns |
| $T_{IF5CK}$ / $T_{CKIF5}$ | 5-input function: F/G inputs | 1.6 / 0 | - | 1.8 / 0 | - | ns |
| $T_{F5INCK}$ / $T_{CKF5IN}$ | 6-input function: F5IN input | 1.0 / 0 | - | 1.1 / 0 | - | ns |
| $T_{IF6CK}$ / $T_{CKIF6}$ | 6-input function: F/G inputs via F6 MUX | 1.6 / 0 | - | 1.8 / 0 | - | ns |
| $T_{DICK}$ / $T_{CKDI}$ | BX/BY inputs | 0.8 / 0 | - | 0.8 / 0 | - | ns |
| $T_{CECK}$ / $T_{CKCE}$ | CE input | 0.9 / 0 | - | 0.9 / 0 | - | ns |
| $T_{RCK}$ / $T_{CKR}$ | SR/BY inputs (synchronous) | 0.8 / 0 | - | 0.8 / 0 | - | ns |
| **Clock CLK** | | | | | | |
| $T_{CH}$ | Minimum pulse width, High | - | 1.9 | - | 1.9 | ns |
| $T_{CL}$ | Minimum pulse width, Low | - | 1.9 | - | 1.9 | ns |
| **Set/Reset** | | | | | | |
| $T_{RPW}$ | Minimum pulse width, SR/BY inputs | 3.1 | - | 3.1 | - | ns |
| $T_{RQ}$ | Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | - | 1.1 | - | 1.3 | ns |
| $T_{IOGSRQ}$ | Delay from GSR to XQ/YQ outputs | - | 9.9 | - | 11.7 | ns |
| $F_{TOG}$ | Toggle frequency (for export control) | - | 263 | - | 263 | MHz |

**Notes:**
1. A zero hold time listing indicates no hold time or a negative hold time.

## Package Thermal Characteristics

Table 39 provides the thermal characteristics for the various Spartan-II FPGA package offerings. This information is also available using the Thermal Query tool on xilinx.com (www.xilinx.com/cgi-bin/thermal/thermal.pl).

The junction-to-case thermal resistance ($\theta_{JC}$) indicates the difference between the temperature measured on the package body (case) and the die junction temperature per watt of power consumption. The junction-to-board ($\theta_{JB}$) value similarly reports the difference between the board and junction temperature. The junction-to-ambient ($\theta_{JA}$) value reports the temperature difference between the ambient environment and the junction temperature. The $\theta_{JA}$ value is reported at different air velocities, measured in linear feet per minute (LFM). The "Still Air (0 LFM)" column shows the $\theta_{JA}$ value in a system without a fan. The thermal resistance drops with increasing air flow.

*Table 39:* **Spartan-II Package Thermal Characteristics**

| Package | Device | Junction-to-Case ($\theta_{JC}$) | Junction-to-Board ($\theta_{JB}$) | Junction-to-Ambient ($\theta_{JA}$) at Different Air Flows | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | | Still Air (0 LFM) | 250 LFM | 500 LFM | 750 LFM | |
| VQ100 VQG100 | XC2S15 | 11.3 | N/A | 44.1 | 36.7 | 34.2 | 33.3 | °C/Watt |
| | XC2S30 | 10.1 | N/A | 40.7 | 33.9 | 31.5 | 30.8 | °C/Watt |
| TQ144 TQG144 | XC2S15 | 7.3 | N/A | 38.6 | 30.0 | 25.7 | 24.1 | °C/Watt |
| | XC2S30 | 6.7 | N/A | 34.7 | 27.0 | 23.1 | 21.7 | °C/Watt |
| | XC2S50 | 5.8 | N/A | 32.2 | 25.1 | 21.4 | 20.1 | °C/Watt |
| | XC2S100 | 5.3 | N/A | 31.4 | 24.4 | 20.9 | 19.6 | °C/Watt |
| CS144 CSG144 | XC2S30 | 2.8 | N/A | 34.0 | 26.0 | 23.9 | 23.2 | °C/Watt |
| PQ208 PQG208 | XC2S50 | 6.7 | N/A | 25.2 | 18.6 | 16.4 | 15.2 | °C/Watt |
| | XC2S100 | 5.9 | N/A | 24.6 | 18.1 | 16.0 | 14.9 | °C/Watt |
| | XC2S150 | 5.0 | N/A | 23.8 | 17.6 | 15.6 | 14.4 | °C/Watt |
| | XC2S200 | 4.1 | N/A | 23.0 | 17.0 | 15.0 | 13.9 | °C/Watt |
| FG256 FGG256 | XC2S50 | 7.1 | 17.6 | 27.2 | 21.4 | 20.3 | 19.8 | °C/Watt |
| | XC2S100 | 5.8 | 15.1 | 25.1 | 19.5 | 18.3 | 17.8 | °C/Watt |
| | XC2S150 | 4.6 | 12.7 | 23.0 | 17.6 | 16.3 | 15.8 | °C/Watt |
| | XC2S200 | 3.5 | 10.7 | 21.4 | 16.1 | 14.7 | 14.2 | °C/Watt |
| FG456 FGG456 | XC2S150 | 2.0 | N/A | 21.9 | 17.3 | 15.8 | 15.2 | °C/Watt |
| | XC2S200 | 2.0 | N/A | 21.0 | 16.6 | 15.1 | 14.5 | °C/Watt |

## XC2S50 Device Pinouts

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| GND | - | P143 | P1 | GND* | - |
| TMS | - | P142 | P2 | D3 | - |
| I/O | 7 | P141 | P3 | C2 | 149 |
| I/O | 7 | - | - | A2 | 152 |
| I/O | 7 | P140 | P4 | B1 | 155 |
| I/O | 7 | - | - | E3 | 158 |
| I/O | 7 | - | P5 | D2 | 161 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 7 | P139 | P6 | C1 | 164 |
| I/O | 7 | - | P7 | F3 | 167 |
| I/O | 7 | - | - | E2 | 170 |
| I/O | 7 | P138 | P8 | E4 | 173 |
| I/O | 7 | P137 | P9 | D1 | 176 |
| I/O | 7 | P136 | P10 | E1 | 179 |
| GND | - | P135 | P11 | GND* | - |
| $V_{CCO}$ | 7 | - | P12 | $V_{CCO}$ Bank 7* | - |
| $V_{CCINT}$ | - | - | P13 | $V_{CCINT}$* | - |
| I/O | 7 | P134 | P14 | F2 | 182 |
| I/O | 7 | P133 | P15 | G3 | 185 |
| I/O | 7 | - | - | F1 | 188 |
| I/O | 7 | - | P16 | F4 | 191 |
| I/O | 7 | - | P17 | F5 | 194 |
| I/O | 7 | - | P18 | G2 | 197 |
| GND | - | - | P19 | GND* | - |
| I/O, $V_{REF}$ | 7 | P132 | P20 | H3 | 200 |
| I/O | 7 | P131 | P21 | G4 | 203 |
| I/O | 7 | - | - | H2 | 206 |
| I/O | 7 | P130 | P22 | G5 | 209 |
| I/O | 7 | - | P23 | H4 | 212 |
| I/O, IRDY(1) | 7 | P129 | P24 | G1 | 215 |
| GND | - | P128 | P25 | GND* | - |
| $V_{CCO}$ | 7 | P127 | P26 | $V_{CCO}$ Bank 7* | - |
| $V_{CCO}$ | 6 | P127 | P26 | $V_{CCO}$ Bank 6* | - |
| I/O, TRDY(1) | 6 | P126 | P27 | J2 | 218 |
| $V_{CCINT}$ | - | P125 | P28 | $V_{CCINT}$* | - |
| I/O | 6 | P124 | P29 | H1 | 224 |
| I/O | 6 | - | - | J4 | 227 |
| I/O | 6 | P123 | P30 | J1 | 230 |
| I/O, $V_{REF}$ | 6 | P122 | P31 | J3 | 233 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| GND | - | - | P32 | GND* | - |
| I/O | 6 | - | P33 | K5 | 236 |
| I/O | 6 | - | P34 | K2 | 239 |
| I/O | 6 | - | P35 | K1 | 242 |
| I/O | 6 | - | - | K3 | 245 |
| I/O | 6 | P121 | P36 | L1 | 248 |
| I/O | 6 | P120 | P37 | L2 | 251 |
| $V_{CCINT}$ | - | - | P38 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 6 | - | P39 | $V_{CCO}$ Bank 6* | - |
| GND | - | P119 | P40 | GND* | - |
| I/O | 6 | P118 | P41 | K4 | 254 |
| I/O | 6 | P117 | P42 | M1 | 257 |
| I/O | 6 | P116 | P43 | L4 | 260 |
| I/O | 6 | - | - | M2 | 263 |
| I/O | 6 | - | P44 | L3 | 266 |
| I/O, $V_{REF}$ | 6 | P115 | P45 | N1 | 269 |
| GND | - | - | - | GND* | - |
| I/O | 6 | - | P46 | P1 | 272 |
| I/O | 6 | - | - | L5 | 275 |
| I/O | 6 | P114 | P47 | N2 | 278 |
| I/O | 6 | - | - | M4 | 281 |
| I/O | 6 | P113 | P48 | R1 | 284 |
| I/O | 6 | P112 | P49 | M3 | 287 |
| M1 | - | P111 | P50 | P2 | 290 |
| GND | - | P110 | P51 | GND* | - |
| M0 | - | P109 | P52 | N3 | 291 |
| $V_{CCO}$ | 6 | P108 | P53 | $V_{CCO}$ Bank 6* | - |
| $V_{CCO}$ | 5 | P107 | P53 | $V_{CCO}$ Bank 5* | - |
| M2 | - | P106 | P54 | R3 | 292 |
| I/O | 5 | - | - | N5 | 299 |
| I/O | 5 | P103 | P57 | T2 | 302 |
| I/O | 5 | - | - | P5 | 305 |
| I/O | 5 | - | P58 | T3 | 308 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 5 | P102 | P59 | T4 | 311 |
| I/O | 5 | - | P60 | M6 | 314 |
| I/O | 5 | - | - | T5 | 317 |
| I/O | 5 | P101 | P61 | N6 | 320 |
| I/O | 5 | P100 | P62 | R5 | 323 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| I/O | 3 | - | - | J14 | 503 |
| I/O | 3 | P56 | P127 | K15 | 506 |
| $V_{CCINT}$ | - | P55 | P128 | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P54 | P129 | J15 | 512 |
| $V_{CCO}$ | 3 | P53 | P130 | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P53 | P130 | $V_{CCO}$ Bank 2* | - |
| GND | - | P52 | P131 | GND* | - |
| I/O, IRDY(1) | 2 | P51 | P132 | H16 | 515 |
| I/O | 2 | - | P133 | H14 | 518 |
| I/O | 2 | P50 | P134 | H15 | 521 |
| I/O | 2 | - | - | J13 | 524 |
| I/O (D3) | 2 | P49 | P135 | G16 | 527 |
| I/O, $V_{REF}$ | 2 | P48 | P136 | H13 | 530 |
| GND | - | - | P137 | GND* | - |
| I/O | 2 | - | P138 | G14 | 533 |
| I/O | 2 | - | P139 | G15 | 536 |
| I/O | 2 | - | P140 | G12 | 539 |
| I/O | 2 | - | - | F16 | 542 |
| I/O | 2 | P47 | P141 | G13 | 545 |
| I/O (D2) | 2 | P46 | P142 | F15 | 548 |
| $V_{CCINT}$ | - | - | P143 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | - | P144 | $V_{CCO}$ Bank 2* | - |
| GND | - | P45 | P145 | GND* | - |
| I/O (D1) | 2 | P44 | P146 | E16 | 551 |
| I/O | 2 | P43 | P147 | F14 | 554 |
| I/O | 2 | P42 | P148 | D16 | 557 |
| I/O | 2 | - | - | F12 | 560 |
| I/O | 2 | - | P149 | E15 | 563 |
| I/O, $V_{REF}$ | 2 | P41 | P150 | F13 | 566 |
| GND | - | - | - | GND* | - |
| I/O | 2 | - | P151 | E14 | 569 |
| I/O | 2 | - | - | C16 | 572 |
| I/O | 2 | P40 | P152 | E13 | 575 |
| I/O | 2 | - | - | B16 | 578 |
| I/O (DIN, D0) | 2 | P39 | P153 | D14 | 581 |
| I/O (DOUT, BUSY) | 2 | P38 | P154 | C15 | 584 |
| CCLK | 2 | P37 | P155 | D15 | 587 |
| $V_{CCO}$ | 2 | P36 | P156 | $V_{CCO}$ Bank 2* | - |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| $V_{CCO}$ | 1 | P35 | P156 | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P34 | P157 | B14 | - |
| GND | - | P33 | P158 | GND* | - |
| TDI | - | P32 | P159 | A15 | - |
| I/O ($\overline{CS}$) | 1 | P31 | P160 | B13 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P30 | P161 | C13 | 3 |
| I/O | 1 | - | - | C12 | 6 |
| I/O | 1 | P29 | P162 | A14 | 9 |
| I/O | 1 | - | - | D12 | 12 |
| I/O | 1 | - | P163 | B12 | 15 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 1 | P28 | P164 | C11 | 18 |
| I/O | 1 | - | P165 | A13 | 21 |
| I/O | 1 | - | - | D11 | 24 |
| I/O | 1 | - | P166 | A12 | 27 |
| I/O | 1 | P27 | P167 | E11 | 30 |
| I/O | 1 | P26 | P168 | B11 | 33 |
| GND | - | P25 | P169 | GND* | - |
| $V_{CCO}$ | 1 | - | P170 | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P24 | P171 | $V_{CCINT}$* | - |
| I/O | 1 | P23 | P172 | A11 | 36 |
| I/O | 1 | P22 | P173 | C10 | 39 |
| I/O | 1 | - | P174 | B10 | 45 |
| I/O | 1 | - | P175 | D10 | 48 |
| I/O | 1 | - | P176 | A10 | 51 |
| GND | - | - | P177 | GND* | - |
| I/O, $V_{REF}$ | 1 | P21 | P178 | B9 | 54 |
| I/O | 1 | - | P179 | E10 | 57 |
| I/O | 1 | - | - | A9 | 60 |
| I/O | 1 | P20 | P180 | D9 | 63 |
| I/O | 1 | P19 | P181 | A8 | 66 |
| I, GCK2 | 1 | P18 | P182 | C9 | 72 |
| GND | - | P17 | P183 | GND* | - |
| $V_{CCO}$ | 1 | P16 | P184 | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P16 | P184 | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P15 | P185 | B8 | 73 |
| $V_{CCINT}$ | - | P14 | P186 | $V_{CCINT}$* | - |
| I/O | 0 | P13 | P187 | A7 | 80 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O, $V_{REF}$ | 4 | P79 | P95 | T11 | AB16 | 502 |
| I/O | 4 | - | - | - | AB17 | 505 |
| I/O | 4 | P78 | P96 | N11 | V15 | 508 |
| I/O | 4 | - | - | R12 | Y16 | 511 |
| I/O | 4 | - | P97 | P11 | AB18 | 517 |
| I/O, $V_{REF}$ | 4 | P77 | P98 | T12 | AB19 | 520 |
| $V_{CCO}$ | 4 | - | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 4 | - | P99 | T13 | Y17 | 523 |
| I/O | 4 | - | - | N12 | V16 | 526 |
| I/O | 4 | - | - | - | W17 | 529 |
| I/O | 4 | P76 | P100 | R13 | AB20 | 532 |
| I/O | 4 | - | - | P12 | AA19 | 535 |
| I/O | 4 | P75 | P101 | P13 | AA20 | 541 |
| I/O | 4 | P74 | P102 | T14 | W18 | 544 |
| GND | - | P73 | P103 | GND* | GND* | - |
| DONE | 3 | P72 | P104 | R14 | Y19 | 547 |
| $V_{CCO}$ | 4 | P71 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P70 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{PROGRAM}$ | - | P69 | P106 | P15 | W20 | 550 |
| I/O ($\overline{INIT}$) | 3 | P68 | P107 | N15 | V19 | 551 |
| I/O (D7) | 3 | P67 | P108 | N14 | Y21 | 554 |
| I/O | 3 | - | - | T15 | W21 | 560 |
| I/O | 3 | P66 | P109 | M13 | U20 | 563 |
| I/O | 3 | - | - | - | U19 | 566 |
| I/O | 3 | - | - | R16 | T18 | 569 |
| I/O | 3 | - | P110 | M14 | W22 | 572 |
| GND | - | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P65 | P111 | L14 | U21 | 575 |
| I/O | 3 | - | P112 | M15 | T20 | 578 |
| I/O | 3 | - | - | L12 | T21 | 584 |
| I/O | 3 | P64 | P113 | P16 | R18 | 587 |
| I/O | 3 | - | - | - | U22 | 590 |
| I/O, $V_{REF}$ | 3 | P63 | P114 | L13 | R19 | 593 |
| I/O (D6) | 3 | P62 | P115 | N16 | T22 | 596 |
| GND | - | P61 | P116 | GND* | GND* | - |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| $V_{CCO}$ | 3 | - | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P60 | P119 | M16 | R21 | 599 |
| I/O | 3 | P59 | P120 | K14 | P18 | 602 |
| I/O | 3 | - | - | L16 | P20 | 605 |
| I/O | 3 | - | P121 | K13 | P21 | 608 |
| I/O | 3 | - | P122 | L15 | N18 | 614 |
| I/O | 3 | - | P123 | K12 | N20 | 617 |
| GND | - | - | P124 | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P58 | P125 | K16 | N21 | 620 |
| I/O (D4) | 3 | P57 | P126 | J16 | N22 | 623 |
| I/O | 3 | - | - | J14 | M19 | 626 |
| I/O | 3 | P56 | P127 | K15 | M20 | 629 |
| $V_{CCINT}$ | - | P55 | P128 | E5 | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P54 | P129 | J15 | M22 | 638 |
| $V_{CCO}$ | 3 | P53 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P53 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P52 | P131 | GND* | GND* | - |
| I/O, IRDY(1) | 2 | P51 | P132 | H16 | L20 | 641 |
| I/O | 2 | - | P133 | H14 | L17 | 644 |
| I/O | 2 | P50 | P134 | H15 | L21 | 650 |
| I/O | 2 | - | - | J13 | L22 | 653 |
| I/O (D3) | 2 | P49 | P135 | G16 | K20 | 656 |
| I/O, $V_{REF}$ | 2 | P48 | P136 | H13 | K21 | 659 |
| GND | - | - | P137 | GND* | GND* | - |
| I/O | 2 | - | P138 | G14 | K22 | 662 |
| I/O | 2 | - | P139 | G15 | J21 | 665 |
| I/O | 2 | - | P140 | G12 | J18 | 671 |
| I/O | 2 | - | - | F16 | J22 | 674 |
| I/O | 2 | P47 | P141 | G13 | H19 | 677 |
| I/O (D2) | 2 | P46 | P142 | F15 | H20 | 680 |
| $V_{CCINT}$ | - | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | - | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P45 | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P44 | P146 | E16 | H22 | 683 |
| I/O, $V_{REF}$ | 2 | P43 | P147 | F14 | H18 | 686 |
| I/O | 2 | - | - | - | G21 | 689 |
| I/O | 2 | P42 | P148 | D16 | G18 | 692 |

## XC2S100 Device Pinouts *(Continued)*

| XC2S100 Pad Name | | | | | | |
|---|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 0 | - | P188 | A6 | C10 | 107 |
| I/O, $V_{REF}$ | 0 | P12 | P189 | B7 | A9 | 110 |
| GND | - | - | P190 | GND* | GND* | - |
| I/O | 0 | - | P191 | C8 | B9 | 113 |
| I/O | 0 | - | P192 | D7 | E10 | 116 |
| I/O | 0 | - | P193 | E7 | A8 | 122 |
| I/O | 0 | - | - | - | D9 | 125 |
| I/O | 0 | P11 | P194 | C7 | E9 | 128 |
| I/O | 0 | P10 | P195 | B6 | A7 | 131 |
| $V_{CCINT}$ | - | P9 | P196 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 0 | - | P197 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | P8 | P198 | GND* | GND* | - |
| I/O | 0 | P7 | P199 | A5 | B7 | 134 |
| I/O, $V_{REF}$ | 0 | P6 | P200 | C6 | E8 | 137 |
| I/O | 0 | - | - | - | D8 | 140 |
| I/O | 0 | - | P201 | B5 | C7 | 143 |
| I/O | 0 | - | - | D6 | D7 | 146 |
| I/O | 0 | - | P202 | A4 | D6 | 152 |
| I/O, $V_{REF}$ | 0 | P5 | P203 | B4 | C6 | 155 |
| $V_{CCO}$ | 0 | - | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | - | - | GND* | GND* | - |
| I/O | 0 | - | P204 | E6 | B5 | 158 |
| I/O | 0 | - | - | D5 | E7 | 161 |
| I/O | 0 | - | - | - | E6 | 164 |
| I/O | 0 | P4 | P205 | A3 | B4 | 167 |
| I/O | 0 | - | - | C5 | A3 | 170 |
| I/O | 0 | P3 | P206 | B3 | C5 | 176 |
| TCK | - | P2 | P207 | C4 | C4 | - |
| $V_{CCO}$ | 0 | P1 | P208 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P144 | P208 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 4 | P90 | R11 | AA15 | 595 |
| $V_{CCINT}$ | - | P91 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | P92 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P93 | GND* | GND* | - |
| I/O | 4 | P94 | M11 | Y15 | 598 |
| I/O, $V_{REF}$ | 4 | P95 | T11 | AB16 | 601 |
| I/O | 4 | - | - | AB17 | 604 |
| I/O | 4 | P96 | N11 | V15 | 607 |
| I/O | 4 | - | R12 | Y16 | 610 |
| I/O | 4 | - | - | AA17 | 613 |
| I/O | 4 | - | - | W16 | 616 |
| I/O | 4 | P97 | P11 | AB18 | 619 |
| I/O, $V_{REF}$ | 4 | P98 | T12 | AB19 | 622 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | P99 | T13 | Y17 | 625 |
| I/O | 4 | - | N12 | V16 | 628 |
| I/O | 4 | - | - | AA18 | 631 |
| I/O | 4 | - | - | W17 | 634 |
| I/O | 4 | P100 | R13 | AB20 | 637 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | P12 | AA19 | 640 |
| I/O | 4 | - | - | V17 | 643 |
| I/O | 4 | - | - | Y18 | 646 |
| I/O | 4 | P101 | P13 | AA20 | 649 |
| I/O | 4 | P102 | T14 | W18 | 652 |
| GND | - | P103 | GND* | GND* | - |
| DONE | 3 | P104 | R14 | Y19 | 655 |
| $V_{CCO}$ | 4 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{PROGRAM}$ | - | P106 | P15 | W20 | 658 |
| I/O ($\overline{INIT}$) | 3 | P107 | N15 | V19 | 659 |
| I/O (D7) | 3 | P108 | N14 | Y21 | 662 |
| I/O | 3 | - | - | V20 | 665 |
| I/O | 3 | - | - | AA22 | 668 |
| I/O | 3 | - | T15 | W21 | 671 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P109 | M13 | U20 | 674 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | PQ208 | FG256 | FG456 | Bndry Scan |
| I/O | 3 | - | - | U19 | 677 |
| I/O | 3 | - | - | V21 | 680 |
| I/O | 3 | - | R16 | T18 | 683 |
| I/O | 3 | P110 | M14 | W22 | 686 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P111 | L14 | U21 | 689 |
| I/O | 3 | P112 | M15 | T20 | 692 |
| I/O | 3 | - | - | T19 | 695 |
| I/O | 3 | - | - | V22 | 698 |
| I/O | 3 | - | L12 | T21 | 701 |
| I/O | 3 | P113 | P16 | R18 | 704 |
| I/O | 3 | - | - | U22 | 707 |
| I/O, $V_{REF}$ | 3 | P114 | L13 | R19 | 710 |
| I/O (D6) | 3 | P115 | N16 | T22 | 713 |
| GND | - | P116 | GND* | GND* | - |
| $V_{CCO}$ | 3 | P117 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | P118 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P119 | M16 | R21 | 716 |
| I/O | 3 | P120 | K14 | P18 | 719 |
| I/O | 3 | - | - | P19 | 725 |
| I/O | 3 | - | L16 | P20 | 728 |
| I/O | 3 | P121 | K13 | P21 | 731 |
| I/O | 3 | - | - | N19 | 734 |
| I/O | 3 | P122 | L15 | N18 | 740 |
| I/O | 3 | P123 | K12 | N20 | 743 |
| GND | - | P124 | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P125 | K16 | N21 | 746 |
| I/O (D4) | 3 | P126 | J16 | N22 | 749 |
| I/O | 3 | - | J14 | M19 | 752 |
| I/O | 3 | P127 | K15 | M20 | 755 |
| I/O | 3 | - | - | M18 | 758 |
| $V_{CCINT}$ | - | P128 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O, TRDY(1) | 3 | P129 | J15 | M22 | 764 |
| $V_{CCO}$ | 3 | P130 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $V_{CCO}$ | 2 | P130 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P131 | GND* | GND* | - |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O, IRDY(1) | 2 | P132 | H16 | L20 | 767 |
| I/O | 2 | P133 | H14 | L17 | 770 |
| I/O | 2 | - | - | L18 | 773 |
| I/O | 2 | P134 | H15 | L21 | 776 |
| I/O | 2 | - | J13 | L22 | 779 |
| I/O (D3) | 2 | P135 | G16 | K20 | 782 |
| I/O, $V_{REF}$ | 2 | P136 | H13 | K21 | 785 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P137 | GND* | GND* | - |
| I/O | 2 | P138 | G14 | K22 | 788 |
| I/O | 2 | P139 | G15 | J21 | 791 |
| I/O | 2 | - | - | J20 | 797 |
| I/O | 2 | P140 | G12 | J18 | 800 |
| I/O | 2 | - | F16 | J22 | 803 |
| I/O | 2 | - | - | J19 | 806 |
| I/O | 2 | P141 | G13 | H19 | 812 |
| I/O (D2) | 2 | P142 | F15 | H20 | 815 |
| $V_{CCINT}$ | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P146 | E16 | H22 | 818 |
| I/O, $V_{REF}$ | 2 | P147 | F14 | H18 | 821 |
| I/O | 2 | - | - | G21 | 824 |
| I/O | 2 | P148 | D16 | G18 | 827 |
| I/O | 2 | - | F12 | G20 | 830 |
| I/O | 2 | - | - | G19 | 833 |
| I/O | 2 | - | - | F22 | 836 |
| I/O | 2 | P149 | E15 | F19 | 839 |
| I/O, $V_{REF}$ | 2 | P150 | F13 | F21 | 842 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | P151 | E14 | F20 | 845 |
| I/O | 2 | - | C16 | F18 | 848 |
| I/O | 2 | - | - | E22 | 851 |
| I/O | 2 | - | - | E21 | 854 |
| I/O | 2 | P152 | E13 | D22 | 857 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | B16 | E20 | 860 |
| I/O | 2 | - | - | D21 | 863 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 2 | - | - | C22 | 866 |
| I/O (DIN, D0) | 2 | P153 | D14 | D20 | 869 |
| I/O (DOUT, BUSY) | 2 | P154 | C15 | C21 | 872 |
| CCLK | 2 | P155 | D15 | B22 | 875 |
| $V_{CCO}$ | 2 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| $V_{CCO}$ | 1 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P157 | B14 | A21 | - |
| GND | - | P158 | GND* | GND* | - |
| TDI | - | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | B19 | 6 |
| I/O | 1 | - | - | C18 | 9 |
| I/O | 1 | - | C12 | D17 | 12 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P162 | A14 | A19 | 15 |
| I/O | 1 | - | - | B18 | 18 |
| I/O | 1 | - | - | E16 | 21 |
| I/O | 1 | - | D12 | C17 | 24 |
| I/O | 1 | P163 | B12 | D16 | 27 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P164 | C11 | A18 | 30 |
| I/O | 1 | P165 | A13 | B17 | 33 |
| I/O | 1 | - | - | E15 | 36 |
| I/O | 1 | - | - | A17 | 39 |
| I/O | 1 | - | D11 | D15 | 42 |
| I/O | 1 | P166 | A12 | C16 | 45 |
| I/O | 1 | - | - | D14 | 48 |
| I/O, $V_{REF}$ | 1 | P167 | E11 | E14 | 51 |
| I/O | 1 | P168 | B11 | A16 | 54 |
| GND | - | P169 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P172 | A11 | C15 | 57 |
| I/O | 1 | P173 | C10 | B15 | 60 |
| I/O | 1 | - | - | A15 | 66 |
| I/O | 1 | - | - | F12 | 69 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I, GCK0 | 4 | P80 | N8 | W12 | 636 |
| I/O | 4 | P81 | N9 | U12 | 640 |
| I/O | 4 | - | - | V12 | 646 |
| I/O | 4 | P82 | R9 | Y12 | 649 |
| I/O | 4 | - | N10 | AA12 | 652 |
| I/O | 4 | - | - | W13 | 655 |
| I/O | 4 | P83 | T9 | AB13 | 661 |
| I/O, $V_{REF}$ | 4 | P84 | P9 | AA13 | 664 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P85 | GND* | GND* | - |
| I/O | 4 | P86 | M10 | Y13 | 667 |
| I/O | 4 | P87 | R10 | V13 | 670 |
| I/O | 4 | - | - | AB14 | 673 |
| I/O | 4 | - | - | W14 | 676 |
| I/O | 4 | P88 | P10 | AA14 | 679 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | - | V14 | 682 |
| I/O | 4 | - | - | Y14 | 685 |
| I/O | 4 | - | - | W15 | 688 |
| I/O | 4 | P89 | T10 | AB15 | 691 |
| I/O | 4 | P90 | R11 | AA15 | 694 |
| $V_{CCINT}$ | - | P91 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | P92 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P93 | GND* | GND* | - |
| I/O | 4 | P94 | M11 | Y15 | 697 |
| I/O, $V_{REF}$ | 4 | P95 | T11 | AB16 | 700 |
| I/O | 4 | - | - | AB17 | 706 |
| I/O | 4 | P96 | N11 | V15 | 709 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | R12 | Y16 | 712 |
| I/O | 4 | - | - | AA17 | 715 |
| I/O | 4 | - | - | W16 | 718 |
| I/O | 4 | P97 | P11 | AB18 | 721 |
| I/O, $V_{REF}$ | 4 | P98 | T12 | AB19 | 724 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | P99 | T13 | Y17 | 727 |
| I/O | 4 | - | N12 | V16 | 730 |
| I/O | 4 | - | - | AA18 | 733 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 4 | - | - | W17 | 739 |
| I/O, $V_{REF}$ | 4 | P100 | R13 | AB20 | 742 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | P12 | AA19 | 745 |
| I/O | 4 | - | - | V17 | 748 |
| I/O | 4 | - | - | Y18 | 751 |
| I/O | 4 | P101 | P13 | AA20 | 757 |
| I/O | 4 | P102 | T14 | W18 | 760 |
| GND | - | P103 | GND* | GND* | - |
| DONE | 3 | P104 | R14 | Y19 | 763 |
| $V_{CCO}$ | 4 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{\text{PROGRAM}}$ | - | P106 | P15 | W20 | 766 |
| I/O ($\overline{\text{INIT}}$) | 3 | P107 | N15 | V19 | 767 |
| I/O (D7) | 3 | P108 | N14 | Y21 | 770 |
| I/O | 3 | - | - | V20 | 776 |
| I/O | 3 | - | - | AA22 | 779 |
| I/O | 3 | - | T15 | W21 | 782 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P109 | M13 | U20 | 785 |
| I/O | 3 | - | - | U19 | 788 |
| I/O | 3 | - | - | V21 | 794 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | - | R16 | T18 | 797 |
| I/O | 3 | P110 | M14 | W22 | 800 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P111 | L14 | U21 | 803 |
| I/O | 3 | P112 | M15 | T20 | 806 |
| I/O | 3 | - | - | T19 | 809 |
| I/O | 3 | - | - | V22 | 812 |
| I/O | 3 | - | L12 | T21 | 815 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P113 | P16 | R18 | 818 |
| I/O | 3 | - | - | U22 | 821 |
| I/O, $V_{REF}$ | 3 | P114 | L13 | R19 | 827 |
| I/O (D6) | 3 | P115 | N16 | T22 | 830 |
| GND | - | P116 | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| $V_{CCO}$ | 1 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P157 | B14 | A21 | - |
| GND | - | P158 | GND* | GND* | - |
| TDI | - | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | B19 | 9 |
| I/O | 1 | - | - | C18 | 12 |
| I/O | 1 | - | C12 | D17 | 15 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 1 | P162 | A14 | A19 | 18 |
| I/O | 1 | - | - | B18 | 21 |
| I/O | 1 | - | - | E16 | 27 |
| I/O | 1 | - | D12 | C17 | 30 |
| I/O | 1 | P163 | B12 | D16 | 33 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P164 | C11 | A18 | 36 |
| I/O | 1 | P165 | A13 | B17 | 39 |
| I/O | 1 | - | - | E15 | 42 |
| I/O | 1 | - | - | A17 | 45 |
| I/O | 1 | - | D11 | D15 | 48 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P166 | A12 | C16 | 51 |
| I/O | 1 | - | - | D14 | 54 |
| I/O, $V_{REF}$ | 1 | P167 | E11 | E14 | 60 |
| I/O | 1 | P168 | B11 | A16 | 63 |
| GND | - | P169 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P172 | A11 | C15 | 66 |
| I/O | 1 | P173 | C10 | B15 | 69 |
| I/O | 1 | - | - | E13 | 72 |
| I/O | 1 | - | - | A15 | 75 |
| I/O | 1 | - | - | F12 | 78 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P174 | B10 | C14 | 81 |
| I/O | 1 | - | - | B14 | 84 |
| I/O | 1 | - | - | A14 | 87 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 1 | P175 | D10 | D13 | 90 |
| I/O | 1 | P176 | A10 | C13 | 93 |
| GND | - | P177 | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P178 | B9 | B13 | 96 |
| I/O | 1 | P179 | E10 | E12 | 99 |
| I/O | 1 | - | - | A13 | 105 |
| I/O | 1 | - | A9 | B12 | 108 |
| I/O | 1 | P180 | D9 | D12 | 111 |
| I/O | 1 | - | - | C12 | 114 |
| I/O | 1 | P181 | A8 | D11 | 120 |
| I, GCK2 | 1 | P182 | C9 | A11 | 126 |
| GND | - | P183 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P184 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCO}$ | 0 | P184 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| I, GCK3 | 0 | P185 | B8 | C11 | 127 |
| $V_{CCINT}$ | - | P186 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 0 | - | - | E11 | 137 |
| I/O | 0 | P187 | A7 | A10 | 140 |
| I/O | 0 | - | D8 | B10 | 143 |
| I/O | 0 | - | - | F11 | 146 |
| I/O | 0 | P188 | A6 | C10 | 152 |
| I/O, $V_{REF}$ | 0 | P189 | B7 | A9 | 155 |
| $V_{CCO}$ | 0 | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | P190 | GND* | GND* | - |
| I/O | 0 | P191 | C8 | B9 | 158 |
| I/O | 0 | P192 | D7 | E10 | 161 |
| I/O | 0 | - | - | C9 | 164 |
| I/O | 0 | - | - | D10 | 167 |
| I/O | 0 | P193 | E7 | A8 | 170 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | - | D9 | 173 |
| I/O | 0 | - | - | B8 | 176 |
| I/O | 0 | - | - | C8 | 179 |
| I/O | 0 | P194 | C7 | E9 | 182 |
| I/O | 0 | P195 | B6 | A7 | 185 |
| $V_{CCINT}$ | - | P196 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 0 | P197 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |

## Additional XC2S200 Package Pins *(Continued)*

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**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| F7 | F8 | F9 | F10 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U7 | U8 | U9 | U10 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |

## Additional XC2S200 Package Pins *(Continued)*

| G6 | H6 | J6 | K6 | K7 | L7 |
|---|---|---|---|---|---|
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A6 | A12 | B11 | B16 | C2 |
| D1 | D4 | D18 | D19 | E17 | E19 |
| G2 | G22 | L2 | L19 | M2 | M21 |
| R3 | R20 | U3 | U18 | V6 | W4 |
| W19 | Y5 | Y22 | AA1 | AA3 | AA11 |
| AA16 | AB7 | AB12 | AB21 | - | - |

11/02/00

# Revision History

| Version No. | Date | Description |
|---|---|---|
| 2.0 | 09/18/00 | Sectioned the Spartan-II Family data sheet into four modules. Corrected all known errors in the pinout tables. |
| 2.1 | 10/04/00 | Added notes requiring $\overline{PWDN}$ to be tied to $V_{CCINT}$ when unused. |
| 2.2 | 11/02/00 | Removed the Power Down feature. |
| 2.3 | 03/05/01 | Added notes on pinout tables for IRDY and TRDY. |
| 2.4 | 04/30/01 | Reinstated XC2S50 $V_{CCO}$ Bank 7, GND, and "not connected" pins missing in version 2.3. |
| 2.5 | 09/03/03 | Added caution about Not Connected Pins to XC2S30 pinout tables on page 76. |
| 2.8 | 06/13/08 | Added "Package Overview" section. Added notes to clarify shared $V_{CCO}$ banks. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |