# AMD Xilinx - XC2S30-6CS144C Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | 216 |
| Number of Logic Elements/Cells | 972 |
| Total RAM Bits | 24576 |
| Number of I/O | 92 |
| Number of Gates | 30000 |
| Voltage - Supply | 2.375V ~ 2.625V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-TFBGA, CSPBGA |
| Supplier Device Package | 144-LCSBGA (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xc2s30-6cs144c |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## Spartan-II Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination. The four global clock pins are usable as additional user I/Os when not used as a global clock pin. These pins are not included in user I/O counts.

*Table 2:* **Spartan-II FPGA User I/O Chart**(1)

| | | Available User I/O According to Package Type | | | | | |
|---|---|---|---|---|---|---|---|
| **Device** | **Maximum User I/O** | **VQ100 VQG100** | **TQ144 TQG144** | **CS144 CSG144** | **PQ208 PQG208** | **FG256 FGG256** | **FG456 FGG456** |
| XC2S15 | 86 | 60 | 86 | (Note 2) | - | - | - |
| XC2S30 | 92 | 60 | 92 | 92 | (Note 2) | - | - |
| XC2S50 | 176 | - | 92 | - | 140 | 176 | - |
| XC2S100 | 176 | - | 92 | - | 140 | 176 | (Note 2) |
| XC2S150 | 260 | - | - | - | 140 | 176 | 260 |
| XC2S200 | 284 | - | - | - | 140 | 176 | 284 |

**Notes:**
1. All user I/O counts do not include the four global clock/user input pins.
2. Discontinued by PDN2004-01.

## Revision History

| Date | Version No. | Description |
|---|---|---|
| 09/18/00 | 2.0 | Sectioned the Spartan-II Family data sheet into four modules. Added industrial temperature range information. |
| 10/31/00 | 2.1 | Removed Power down feature. |
| 03/05/01 | 2.2 | Added statement on PROMs. |
| 11/01/01 | 2.3 | Updated Product Availability chart. Minor text edits. |
| 09/03/03 | 2.4 | Added device part marking. |
| 08/02/04 | 2.5 | Added information on Pb-free packaging options and removed discontinued options. |
| 06/13/08 | 2.8 | Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |

PN 011311

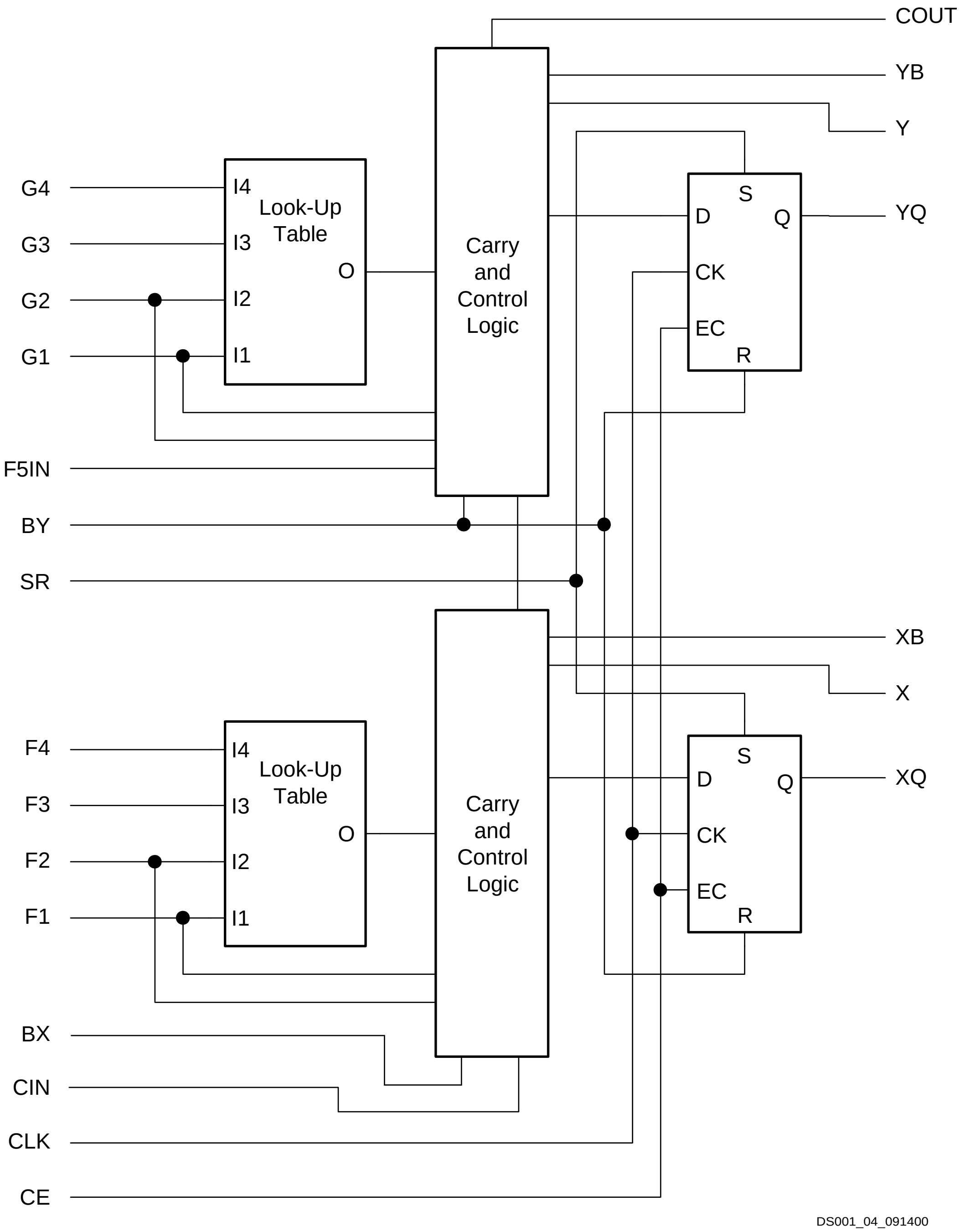

*Figure 4:* **Spartan-II CLB Slice** (two identical slices in each CLB)

## *Storage Elements*

Storage elements in the Spartan-II FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

## *Additional Logic*

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

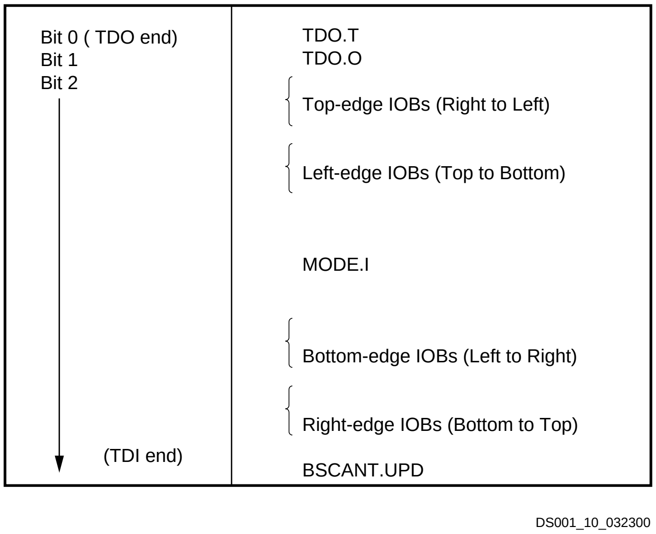

*Figure 10:* **Boundary Scan Bit Sequence**

# Development System

Spartan-II FPGAs are supported by the Xilinx ISE® development tools. The basic methodology for Spartan-II FPGA design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation, while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under a single graphical interface, providing designers with a common user interface regardless of their choice of entry and verification tools. The software simplifies the selection of implementation options with pull-down menus and on-line help.

For HDL design entry, the Xilinx FPGA development system provides interfaces to several synthesis design environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-II FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The design environment supports hierarchical design entry. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

## Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

## Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, the development system includes a download cable, which connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can read back the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

*Table 11:* **Available Library Primitives**

| Primitive | Port A Width | Port B Width |
|---|---|---|
| RAMB4_S4<br>RAMB4_S4_S4<br>RAMB4_S4_S8<br>RAMB4_S4_S16 | 4 | N/A<br>4<br>8<br>16 |
| RAMB4_S8<br>RAMB4_S8_S8<br>RAMB4_S8_S16 | 8 | N/A<br>8<br>16 |
| RAMB4_S16<br>RAMB4_S16_S16 | 16 | N/A<br>16 |

## Port Signals

Each block RAM port operates independently of the others while accessing the same set of 4096 memory cells.

Table 12 describes the depth and width aspect ratios for the block RAM memory.

*Table 12:* **Block RAM Port Aspect Ratios**

| Width | Depth | ADDR Bus | Data Bus |
|---|---|---|---|
| 1 | 4096 | ADDR<11:0> | DATA<0> |
| 2 | 2048 | ADDR<10:0> | DATA<1:0> |
| 4 | 1024 | ADDR<9:0> | DATA<3:0> |
| 8 | 512 | ADDR<8:0> | DATA<7:0> |
| 16 | 256 | ADDR<7:0> | DATA<15:0> |

### *Clock—CLK[A|B]*

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

### *Enable—EN[A|B]*

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

### *Write Enable—WE[A|B]*

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

### Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

### *Address Bus—ADDR[A|B]<#:0>*

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 12.

### *Data In Bus—DI[A|B]<#:0>*

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 12.

### *Data Output Bus—DO[A|B]<#:0>*

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 12.

## Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

## Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$\text{Start} = ([\text{ADDR}_{\text{port}} + 1] * \text{Width}_{\text{port}}) - 1$$

$$\text{End} = \text{ADDR}_{\text{port}} * \text{Width}_{\text{port}}$$

Table 13 shows low order address mapping for each port width.

*Table 13:* **Port Address Mapping**

| Port Width | Port Addresses | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 4095... | 15 | 14 | 13 | 12 | 11 | 10 | 09 | 08 | 07 | 06 | 05 | 04 | 03 | 02 | 01 | 00 |
| 2 | 2047... | 07 | | 06 | | 05 | | 04 | | 03 | | 02 | | 01 | | 00 | |
| 4 | 1023... | 03 | | | | 02 | | | | 01 | | | | 00 | | | |
| 8 | 511... | 01 | | | | | | | | 00 | | | | | | | |
| 16 | 255... | 00 | | | | | | | | | | | | | | | |

## Creating Larger RAM Structures

The block RAM columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

## Location Constraints

Block RAM instances can have LOC properties attached to them to constrain the placement. The block RAM placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form:

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

## Conflict Resolution

The block RAM memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
    - The write succeeds
    - The data out on the writing port accurately reflects the data written.
    - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

### *Single Port Timing*

Figure 33 shows a timing diagram for a single port of a block RAM memory. The block RAM AC switching characteristics are specified in the data sheet. The block RAM memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the block RAM memory is now disabled. The DO bus retains the last value.

### *Dual Port Timing*

Figure 34 shows a timing diagram for a true dual-port read/write block RAM memory. The clock on port A has a longer period than the clock on Port B. The timing parameter $T_{BCCS}$, (clock-to-clock setup) is shown on this diagram. The parameter, $T_{BCCS}$ is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

$T_{BCCS}$ is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location will be invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory will be correct, but the read port will have invalid data. At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the $T_{BCCS}$ parameter and the DOB reflects the new memory values written by Port A.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF primitive names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24). The default is slew rate limited with 12 mA drive.

OBUF placement restrictions require that within a given $V_{CCO}$ bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within any $V_{CCO}$ bank. Table 17 summarizes the output compatibility requirements. The LOC property can specify a location for the OBUF.

*Table 17:* **Output Standards Compatibility Requirements**

| | |
|---|---|
| Rule 1 | Only outputs with standards which share compatible $V_{CCO}$ may be used within the same bank. |
| Rule 2 | There are no placement restrictions for outputs with standards that do not require a $V_{CCO}$. |
| $V_{CCO}$ | Compatible Standards |
| 3.3 | LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3 |
| 2.5 | SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+ |
| 1.5 | HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+ |

### *OBUFT*

The generic 3-state output buffer OBUFT, shown in Figure 39, typically implements 3-state outputs or bidirectional I/O.

With no extension or property specified for the generic OBUFT primitive, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT primitive names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

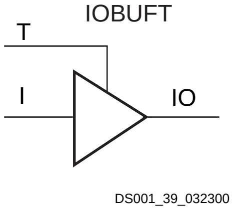

*Figure 39:* **3-State Output Buffer Primitive (OBUFT**

The Versatile I/O OBUFT placement restrictions require that within a given $V_{CCO}$ bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a $V_{REF}$ have automatic placement of a $V_{REF}$ in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding $V_{REF}$) are explicitly placed.

The LOC property can specify a location for the OBUFT.

### *IOBUF*

Use the IOBUF primitive for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 40.

With no extension or property specified for the generic IOBUF primitive, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF primitive names is as follows:

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

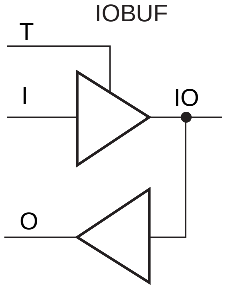

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*Figure 40:* **Input/Output Buffer Primitiveprimitive (IOBUF)**

When the IOBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the $V_{CCO}$ for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard ($V_{CCO}$ < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 36, page 39 for a representation of the Spartan-II FPGA I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given $V_{CCO}$ bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

## Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

### *Input Delay Properties*

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

### *IOB Flip-Flop/Latch Property*

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified:

```
map -pr b <filename>
```

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

### *Location Constraints*

Specify the location of each Versatile I/O primitive with the location constraint LOC attached to the Versatile I/O primitive. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

LOC=A42

LOC=P37

### *Output Slew Rate Property*

In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

### *Output Drive Strength Property*

For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE=

## Revision History

| Date | Version | Description |
|---|---|---|
| 09/18/00 | 2.0 | Sectioned the Spartan-II Family data sheet into four modules. Corrected banking description. |
| 03/05/01 | 2.1 | Clarified guidelines for applying power to $V_{CCINT}$ and $V_{CCO}$ |
| 09/03/03 | 2.2 | The following changes were made:<br>• "Serial Modes," page 20 cautions about toggling $\overline{\text{WRITE}}$ during serial configuration.<br>• Maximum $V_{IH}$ values in Table 32 and Table 33 changed to 5.5V.<br>• In "Boundary Scan," page 13, removed sentence about lack of INTEST support.<br>• In Table 9, page 17, added note about the state of I/Os after power-on.<br>• In "Slave Parallel Mode," page 23, explained configuration bit alignment to SelectMap port. |
| 06/13/08 | 2.8 | Added note that TDI, TMS, and TCK have a default pull-up resistor. Added note on maximum daisy chain limit. Updated Figure 15 and Figure 18 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated DLL section. Recommended using property or attribute instead of primitive to define I/O properties. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |

## IOB Output Delay Adjustments for Different Standards[1]

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

| Symbol | Description | Standard | Speed Grade | | Units |
|---|---|---|---|---|---|
| | | | -6 | -5 | |
| **Output Delay Adjustments (Adj)** | | | | | |
| $T_{OLVTTL\_S2}$ | Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, $C_{SL}$) | LVTTL, Slow, 2 mA | 14.2 | 16.9 | ns |
| $T_{OLVTTL\_S4}$ | | 4 mA | 7.2 | 8.6 | ns |
| $T_{OLVTTL\_S6}$ | | 6 mA | 4.7 | 5.5 | ns |
| $T_{OLVTTL\_S8}$ | | 8 mA | 2.9 | 3.5 | ns |
| $T_{OLVTTL\_S12}$ | | 12 mA | 1.9 | 2.2 | ns |
| $T_{OLVTTL\_S16}$ | | 16 mA | 1.7 | 2.0 | ns |
| $T_{OLVTTL\_S24}$ | | 24 mA | 1.3 | 1.5 | ns |
| $T_{OLVTTL\_F2}$ | | LVTTL, Fast, 2 mA | 12.6 | 15.0 | ns |
| $T_{OLVTTL\_F4}$ | | 4 mA | 5.1 | 6.1 | ns |
| $T_{OLVTTL\_F6}$ | | 6 mA | 3.0 | 3.6 | ns |
| $T_{OLVTTL\_F8}$ | | 8 mA | 1.0 | 1.2 | ns |
| $T_{OLVTTL\_F12}$ | | 12 mA | 0 | 0 | ns |
| $T_{OLVTTL\_F16}$ | | 16 mA | –0.1 | –0.1 | ns |
| $T_{OLVTTL\_F24}$ | | 24 mA | –0.1 | –0.2 | ns |
| $T_{OLVCMOS2}$ | | LVCMOS2 | 0.2 | 0.2 | ns |
| $T_{OPCI33\_3}$ | | PCI, 33 MHz, 3.3V | 2.4 | 2.9 | ns |
| $T_{OPCI33\_5}$ | | PCI, 33 MHz, 5.0V | 2.9 | 3.5 | ns |
| $T_{OPCI66\_3}$ | | PCI, 66 MHz, 3.3V | –0.3 | –0.4 | ns |
| $T_{OGTL}$ | | GTL | 0.6 | 0.7 | ns |
| $T_{OGTLP}$ | | GTL+ | 0.9 | 1.1 | ns |
| $T_{OHSTL\_I}$ | | HSTL I | –0.4 | –0.5 | ns |
| $T_{OHSTL\_III}$ | | HSTL III | –0.8 | –1.0 | ns |
| $T_{OHSTL\_IV}$ | | HSTL IV | –0.9 | –1.1 | ns |
| $T_{OSSTL2\_I}$ | | SSTL2 I | –0.4 | –0.5 | ns |
| $T_{OSSLT2\_II}$ | | SSTL2 II | –0.8 | –1.0 | ns |
| $T_{OSSTL3\_I}$ | | SSTL3 I | –0.4 | –0.5 | ns |
| $T_{OSSTL3\_II}$ | | SSTL3 II | –0.9 | –1.1 | ns |
| $T_{OCTT}$ | | CTT | –0.5 | –0.6 | ns |
| $T_{OAGP}$ | | AGP | –0.8 | –1.0 | ns |

**Notes:**

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.

## DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

| Symbol | Description | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | -6 | | -5 | | |
| | | Min | Max | Min | Max | |
| $F_{CLKINHF}$ | Input clock frequency (CLKDLLHF) | 60 | 200 | 60 | 180 | MHz |
| $F_{CLKINLF}$ | Input clock frequency (CLKDLL) | 25 | 100 | 25 | 90 | MHz |
| $T_{DLLPWHF}$ | Input clock pulse width (CLKDLLHF) | 2.0 | - | 2.4 | - | ns |
| $T_{DLLPWLF}$ | Input clock pulse width (CLKDLL) | 2.5 | - | 3.0 | - | ns |

## DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications were determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers. Figure 52, page 63, provides definitions for various parameters in the table below.

| Symbol | Description | $F_{CLKIN}$ | CLKDLLHF | | CLKDLL | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $T_{IPTOL}$ | Input clock period tolerance | | - | 1.0 | - | 1.0 | ns |
| $T_{IJITCC}$ | Input clock jitter tolerance (cycle-to-cycle) | | - | ±150 | - | ±300 | ps |
| $T_{LOCK}$ | Time required for DLL to acquire lock | > 60 MHz | - | 20 | - | 20 | µs |
| | | 50-60 MHz | - | - | - | 25 | µs |
| | | 40-50 MHz | - | - | - | 50 | µs |
| | | 30-40 MHz | - | - | - | 90 | µs |
| | | 25-30 MHz | - | - | - | 120 | µs |
| $T_{OJITCC}$ | Output jitter (cycle-to-cycle) for any DLL clock output(1) | | - | ±60 | - | ±60 | ps |
| $T_{PHIO}$ | Phase offset between CLKIN and CLKO(2) | | - | ±100 | - | ±100 | ps |
| $T_{PHOO}$ | Phase offset between clock outputs on the DLL(3) | | - | ±140 | - | ±140 | ps |
| $T_{PHIOM}$ | Maximum phase difference between CLKIN and CLKO(4) | | - | ±160 | - | ±160 | ps |
| $T_{PHOOM}$ | Maximum phase difference between clock outputs on the DLL(5) | | - | ±200 | - | ±200 | ps |

**Notes:**

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* output jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase Difference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges due to DLL alone (*excluding* input clock jitter).

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | TQ144 | PQ208 | FG256 | Bndry Scan |
|---|---|---|---|---|---|
| **Function** | **Bank** | | | | |
| I/O | 5 | P99 | P63 | P6 | 326 |
| GND | - | P98 | P64 | GND* | - |
| $V_{CCO}$ | 5 | - | P65 | $V_{CCO}$ Bank 5* | - |
| $V_{CCINT}$ | - | P97 | P66 | $V_{CCINT}$* | - |
| I/O | 5 | P96 | P67 | R6 | 329 |
| I/O | 5 | P95 | P68 | M7 | 332 |
| I/O | 5 | - | P69 | N7 | 338 |
| I/O | 5 | - | P70 | T6 | 341 |
| I/O | 5 | - | P71 | P7 | 344 |
| GND | - | - | P72 | GND* | - |
| I/O, $V_{REF}$ | 5 | P94 | P73 | P8 | 347 |
| I/O | 5 | - | P74 | R7 | 350 |
| I/O | 5 | - | - | T7 | 353 |
| I/O | 5 | P93 | P75 | T8 | 356 |
| $V_{CCINT}$ | - | P92 | P76 | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P91 | P77 | R8 | 365 |
| $V_{CCO}$ | 5 | P90 | P78 | $V_{CCO}$ Bank 5* | - |
| $V_{CCO}$ | 4 | P90 | P78 | $V_{CCO}$ Bank 4* | - |
| GND | - | P89 | P79 | GND* | - |
| I, GCK0 | 4 | P88 | P80 | N8 | 366 |
| I/O | 4 | P87 | P81 | N9 | 370 |
| I/O | 4 | P86 | P82 | R9 | 373 |
| I/O | 4 | - | - | N10 | 376 |
| I/O | 4 | - | P83 | T9 | 379 |
| I/O, $V_{REF}$ | 4 | P85 | P84 | P9 | 382 |
| GND | - | - | P85 | GND* | - |
| I/O | 4 | - | P86 | M10 | 385 |
| I/O | 4 | - | P87 | R10 | 388 |
| I/O | 4 | - | P88 | P10 | 391 |
| I/O | 4 | P84 | P89 | T10 | 397 |
| I/O | 4 | P83 | P90 | R11 | 400 |
| $V_{CCINT}$ | - | P82 | P91 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | - | P92 | $V_{CCO}$ Bank 4* | - |
| GND | - | P81 | P93 | GND* | - |
| I/O | 4 | P80 | P94 | M11 | 403 |
| I/O | 4 | P79 | P95 | T11 | 406 |
| I/O | 4 | P78 | P96 | N11 | 409 |
| I/O | 4 | - | - | R12 | 412 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | TQ144 | PQ208 | FG256 | Bndry Scan |
|---|---|---|---|---|---|
| **Function** | **Bank** | | | | |
| I/O | 4 | - | P97 | P11 | 415 |
| I/O, $V_{REF}$ | 4 | P77 | P98 | T12 | 418 |
| GND | - | - | - | GND* | - |
| I/O | 4 | - | P99 | T13 | 421 |
| I/O | 4 | - | - | N12 | 424 |
| I/O | 4 | P76 | P100 | R13 | 427 |
| I/O | 4 | - | - | P12 | 430 |
| I/O | 4 | P75 | P101 | P13 | 433 |
| I/O | 4 | P74 | P102 | T14 | 436 |
| GND | - | P73 | P103 | GND* | - |
| DONE | 3 | P72 | P104 | R14 | 439 |
| $V_{CCO}$ | 4 | P71 | P105 | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P70 | P105 | $V_{CCO}$ Bank 3* | - |
| $\overline{\text{PROGRAM}}$ | - | P69 | P106 | P15 | 442 |
| I/O ($\overline{\text{INIT}}$) | 3 | P68 | P107 | N15 | 443 |
| I/O (D7) | 3 | P67 | P108 | N14 | 446 |
| I/O | 3 | - | - | T15 | 449 |
| I/O | 3 | P66 | P109 | M13 | 452 |
| I/O | 3 | - | - | R16 | 455 |
| I/O | 3 | - | P110 | M14 | 458 |
| GND | - | - | - | GND* | - |
| I/O, $V_{REF}$ | 3 | P65 | P111 | L14 | 461 |
| I/O | 3 | - | P112 | M15 | 464 |
| I/O | 3 | - | - | L12 | 467 |
| I/O | 3 | P64 | P113 | P16 | 470 |
| I/O | 3 | P63 | P114 | L13 | 473 |
| I/O (D6) | 3 | P62 | P115 | N16 | 476 |
| GND | - | P61 | P116 | GND* | - |
| $V_{CCO}$ | 3 | - | P117 | $V_{CCO}$ Bank 3* | - |
| $V_{CCINT}$ | - | - | P118 | $V_{CCINT}$* | - |
| I/O (D5) | 3 | P60 | P119 | M16 | 479 |
| I/O | 3 | P59 | P120 | K14 | 482 |
| I/O | 3 | - | - | L16 | 485 |
| I/O | 3 | - | P121 | K13 | 488 |
| I/O | 3 | - | P122 | L15 | 491 |
| I/O | 3 | - | P123 | K12 | 494 |
| GND | - | - | P124 | GND* | - |
| I/O, $V_{REF}$ | 3 | P58 | P125 | K16 | 497 |
| I/O (D4) | 3 | P57 | P126 | J16 | 500 |

## XC2S50 Device Pinouts *(Continued)*

| XC2S50 Pad Name | | | | | |
|---|---|---|---|---|---|
| Function | Bank | TQ144 | PQ208 | FG256 | Bndry Scan |
| I/O | 0 | - | - | D8 | 83 |
| I/O | 0 | - | P188 | A6 | 86 |
| I/O, $V_{REF}$ | 0 | P12 | P189 | B7 | 89 |
| GND | - | - | P190 | GND* | - |
| I/O | 0 | - | P191 | C8 | 92 |
| I/O | 0 | - | P192 | D7 | 95 |
| I/O | 0 | - | P193 | E7 | 98 |
| I/O | 0 | P11 | P194 | C7 | 104 |
| I/O | 0 | P10 | P195 | B6 | 107 |
| $V_{CCINT}$ | - | P9 | P196 | $V_{CCINT}$* | - |
| $V_{CCO}$ | 0 | - | P197 | $V_{CCO}$ Bank 0* | - |
| GND | - | P8 | P198 | GND* | - |
| I/O | 0 | P7 | P199 | A5 | 110 |
| I/O | 0 | P6 | P200 | C6 | 113 |
| I/O | 0 | - | P201 | B5 | 116 |
| I/O | 0 | - | - | D6 | 119 |
| I/O | 0 | - | P202 | A4 | 122 |
| I/O, $V_{REF}$ | 0 | P5 | P203 | B4 | 125 |
| GND | - | - | - | GND* | - |
| I/O | 0 | - | P204 | E6 | 128 |
| I/O | 0 | - | - | D5 | 131 |
| I/O | 0 | P4 | P205 | A3 | 134 |
| I/O | 0 | - | - | C5 | 137 |
| I/O | 0 | P3 | P206 | B3 | 140 |
| TCK | - | P2 | P207 | C4 | - |
| $V_{CCO}$ | 0 | P1 | P208 | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P144 | P208 | $V_{CCO}$ Bank 7* | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S50 Package Pins

**TQ144**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P104 | P105 | - | - | - | - |

11/02/00

## XC2S150 Device Pinouts

| XC2S150 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| GND | - | P1 | GND* | GND* | - |
| TMS | - | P2 | D3 | D3 | - |
| I/O | 7 | P3 | C2 | B1 | 221 |
| I/O | 7 | - | - | E4 | 224 |
| I/O | 7 | - | - | C1 | 227 |
| I/O | 7 | - | A2 | F5 | 230 |
| GND | - | - | GND* | GND* | - |
| I/O | 7 | P4 | B1 | D2 | 233 |
| I/O | 7 | - | - | E3 | 236 |
| I/O | 7 | - | - | F4 | 239 |
| I/O | 7 | - | E3 | G5 | 242 |
| I/O | 7 | P5 | D2 | F3 | 245 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 7 | - | $V_{CCO}$<br>Bank 7* | $V_{CCO}$<br>Bank 7* | - |
| I/O, $V_{REF}$ | 7 | P6 | C1 | E2 | 248 |
| I/O | 7 | P7 | F3 | E1 | 251 |
| I/O | 7 | - | - | G4 | 254 |
| I/O | 7 | - | - | G3 | 257 |
| I/O | 7 | - | E2 | H5 | 260 |
| I/O | 7 | P8 | E4 | F2 | 263 |
| I/O | 7 | - | - | F1 | 266 |
| I/O, $V_{REF}$ | 7 | P9 | D1 | H4 | 269 |
| I/O | 7 | P10 | E1 | G1 | 272 |
| GND | - | P11 | GND* | GND* | - |
| $V_{CCO}$ | 7 | P12 | $V_{CCO}$<br>Bank 7* | $V_{CCO}$<br>Bank 7* | - |
| $V_{CCINT}$ | - | P13 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 7 | P14 | F2 | H3 | 275 |
| I/O | 7 | P15 | G3 | H2 | 278 |
| I/O | 7 | - | - | H1 | 284 |
| I/O | 7 | - | F1 | J5 | 287 |
| I/O | 7 | P16 | F4 | J2 | 290 |
| I/O | 7 | - | - | J3 | 293 |
| I/O | 7 | P17 | F5 | K5 | 299 |
| I/O | 7 | P18 | G2 | K1 | 302 |
| GND | - | P19 | GND* | GND* | - |
| $V_{CCO}$ | 7 | - | $V_{CCO}$<br>Bank 7* | $V_{CCO}$<br>Bank 7* | - |
| I/O, $V_{REF}$ | 7 | P20 | H3 | K3 | 305 |
| I/O | 7 | P21 | G4 | K4 | 308 |
| I/O | 7 | - | H2 | L6 | 311 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 7 | P22 | G5 | L1 | 314 |
| I/O | 7 | - | - | L5 | 317 |
| I/O | 7 | P23 | H4 | L4 | 320 |
| I/O, IRDY(1) | 7 | P24 | G1 | L3 | 323 |
| GND | - | P25 | GND* | GND* | - |
| $V_{CCO}$ | 7 | P26 | $V_{CCO}$<br>Bank 7* | $V_{CCO}$<br>Bank 7* | - |
| $V_{CCO}$ | 6 | P26 | $V_{CCO}$<br>Bank 6* | $V_{CCO}$<br>Bank 6* | - |
| I/O, TRDY(1) | 6 | P27 | J2 | M1 | 326 |
| $V_{CCINT}$ | - | P28 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 6 | - | - | M6 | 332 |
| I/O | 6 | P29 | H1 | M3 | 335 |
| I/O | 6 | - | J4 | M4 | 338 |
| I/O | 6 | P30 | J1 | M5 | 341 |
| I/O, $V_{REF}$ | 6 | P31 | J3 | N2 | 344 |
| $V_{CCO}$ | 6 | - | $V_{CCO}$<br>Bank 6* | $V_{CCO}$<br>Bank 6* | - |
| GND | - | P32 | GND* | GND* | - |
| I/O | 6 | P33 | K5 | N3 | 347 |
| I/O | 6 | P34 | K2 | N4 | 350 |
| I/O | 6 | - | - | N5 | 356 |
| I/O | 6 | P35 | K1 | P2 | 359 |
| I/O | 6 | - | K3 | P4 | 362 |
| I/O | 6 | - | - | R1 | 365 |
| I/O | 6 | P36 | L1 | P3 | 371 |
| I/O | 6 | P37 | L2 | R2 | 374 |
| $V_{CCINT}$ | - | P38 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 6 | P39 | $V_{CCO}$<br>Bank 6* | $V_{CCO}$<br>Bank 6* | - |
| GND | - | P40 | GND* | GND* | - |
| I/O | 6 | P41 | K4 | T1 | 377 |
| I/O, $V_{REF}$ | 6 | P42 | M1 | R4 | 380 |
| I/O | 6 | - | - | T2 | 383 |
| I/O | 6 | P43 | L4 | U1 | 386 |
| I/O | 6 | - | M2 | R5 | 389 |
| I/O | 6 | - | - | V1 | 392 |
| I/O | 6 | - | - | T5 | 395 |
| I/O | 6 | P44 | L3 | U2 | 398 |
| I/O, $V_{REF}$ | 6 | P45 | N1 | T3 | 401 |
| $V_{CCO}$ | 6 | - | $V_{CCO}$<br>Bank 6* | $V_{CCO}$<br>Bank 6* | - |
| GND | - | - | GND* | GND* | - |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 6 | P46 | P1 | T4 | 404 |
| I/O | 6 | - | L5 | W1 | 407 |
| I/O | 6 | - | - | V2 | 410 |
| I/O | 6 | - | - | U4 | 413 |
| I/O | 6 | P47 | N2 | Y1 | 416 |
| GND | - | - | GND* | GND* | - |
| I/O | 6 | - | M4 | W2 | 419 |
| I/O | 6 | - | - | V3 | 422 |
| I/O | 6 | - | - | V4 | 425 |
| I/O | 6 | P48 | R1 | Y2 | 428 |
| I/O | 6 | P49 | M3 | W3 | 431 |
| M1 | - | P50 | P2 | U5 | 434 |
| GND | - | P51 | GND* | GND* | - |
| M0 | - | P52 | N3 | AB2 | 435 |
| $V_{CCO}$ | 6 | P53 | $V_{CCO}$ Bank 6* | $V_{CCO}$ Bank 6* | - |
| $V_{CCO}$ | 5 | P53 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| M2 | - | P54 | R3 | Y4 | 436 |
| I/O | 5 | - | - | W5 | 443 |
| I/O | 5 | - | - | AB3 | 446 |
| I/O | 5 | - | N5 | V7 | 449 |
| GND | - | - | GND* | GND* | - |
| I/O | 5 | P57 | T2 | Y6 | 452 |
| I/O | 5 | - | - | AA4 | 455 |
| I/O | 5 | - | - | AB4 | 458 |
| I/O | 5 | - | P5 | W6 | 461 |
| I/O | 5 | P58 | T3 | Y7 | 464 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P59 | T4 | AA5 | 467 |
| I/O | 5 | P60 | M6 | AB5 | 470 |
| I/O | 5 | - | - | V8 | 473 |
| I/O | 5 | - | - | AA6 | 476 |
| I/O | 5 | - | T5 | AB6 | 479 |
| I/O | 5 | P61 | N6 | AA7 | 482 |
| I/O | 5 | - | - | W7 | 485 |
| I/O, $V_{REF}$ | 5 | P62 | R5 | W8 | 488 |
| I/O | 5 | P63 | P6 | Y8 | 491 |
| GND | - | P64 | GND* | GND* | - |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| $V_{CCO}$ | 5 | P65 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCINT}$ | - | P66 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 5 | P67 | R6 | AA8 | 494 |
| I/O | 5 | P68 | M7 | V9 | 497 |
| I/O | 5 | - | - | W9 | 503 |
| I/O | 5 | - | - | AB9 | 506 |
| I/O | 5 | P69 | N7 | Y9 | 509 |
| I/O | 5 | - | - | V10 | 512 |
| I/O | 5 | P70 | T6 | W10 | 518 |
| I/O | 5 | P71 | P7 | AB10 | 521 |
| GND | - | P72 | GND* | GND* | - |
| $V_{CCO}$ | 5 | - | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| I/O, $V_{REF}$ | 5 | P73 | P8 | Y10 | 524 |
| I/O | 5 | P74 | R7 | V11 | 527 |
| I/O | 5 | - | T7 | W11 | 530 |
| I/O | 5 | P75 | T8 | AB11 | 533 |
| I/O | 5 | - | - | U11 | 536 |
| $V_{CCINT}$ | - | P76 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I, GCK1 | 5 | P77 | R8 | Y11 | 545 |
| $V_{CCO}$ | 5 | P78 | $V_{CCO}$ Bank 5* | $V_{CCO}$ Bank 5* | - |
| $V_{CCO}$ | 4 | P78 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P79 | GND* | GND* | - |
| I, GCK0 | 4 | P80 | N8 | W12 | 546 |
| I/O | 4 | P81 | N9 | U12 | 550 |
| I/O | 4 | - | - | V12 | 553 |
| I/O | 4 | P82 | R9 | Y12 | 556 |
| I/O | 4 | - | N10 | AA12 | 559 |
| I/O | 4 | P83 | T9 | AB13 | 562 |
| I/O, $V_{REF}$ | 4 | P84 | P9 | AA13 | 565 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P85 | GND* | GND* | - |
| I/O | 4 | P86 | M10 | Y13 | 568 |
| I/O | 4 | P87 | R10 | V13 | 571 |
| I/O | 4 | - | - | W14 | 577 |
| I/O | 4 | P88 | P10 | AA14 | 580 |
| I/O | 4 | - | - | V14 | 583 |
| I/O | 4 | - | - | Y14 | 586 |
| I/O | 4 | P89 | T10 | AB15 | 592 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| **Function** | **Bank** | **PQ208** | **FG256** | **FG456** | **Bndry Scan** |
| I/O, IRDY(1) | 2 | P132 | H16 | L20 | 767 |
| I/O | 2 | P133 | H14 | L17 | 770 |
| I/O | 2 | - | - | L18 | 773 |
| I/O | 2 | P134 | H15 | L21 | 776 |
| I/O | 2 | - | J13 | L22 | 779 |
| I/O (D3) | 2 | P135 | G16 | K20 | 782 |
| I/O, $V_{REF}$ | 2 | P136 | H13 | K21 | 785 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P137 | GND* | GND* | - |
| I/O | 2 | P138 | G14 | K22 | 788 |
| I/O | 2 | P139 | G15 | J21 | 791 |
| I/O | 2 | - | - | J20 | 797 |
| I/O | 2 | P140 | G12 | J18 | 800 |
| I/O | 2 | - | F16 | J22 | 803 |
| I/O | 2 | - | - | J19 | 806 |
| I/O | 2 | P141 | G13 | H19 | 812 |
| I/O (D2) | 2 | P142 | F15 | H20 | 815 |
| $V_{CCINT}$ | - | P143 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 2 | P144 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | P145 | GND* | GND* | - |
| I/O (D1) | 2 | P146 | E16 | H22 | 818 |
| I/O, $V_{REF}$ | 2 | P147 | F14 | H18 | 821 |
| I/O | 2 | - | - | G21 | 824 |
| I/O | 2 | P148 | D16 | G18 | 827 |
| I/O | 2 | - | F12 | G20 | 830 |
| I/O | 2 | - | - | G19 | 833 |
| I/O | 2 | - | - | F22 | 836 |
| I/O | 2 | P149 | E15 | F19 | 839 |
| I/O, $V_{REF}$ | 2 | P150 | F13 | F21 | 842 |
| $V_{CCO}$ | 2 | - | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | P151 | E14 | F20 | 845 |
| I/O | 2 | - | C16 | F18 | 848 |
| I/O | 2 | - | - | E22 | 851 |
| I/O | 2 | - | - | E21 | 854 |
| I/O | 2 | P152 | E13 | D22 | 857 |
| GND | - | - | GND* | GND* | - |
| I/O | 2 | - | B16 | E20 | 860 |
| I/O | 2 | - | - | D21 | 863 |

## XC2S150 Device Pinouts *(Continued)*

| XC2S150 Pad Name | | | | | |
|---|---|---|---|---|---|
| **Function** | **Bank** | **PQ208** | **FG256** | **FG456** | **Bndry Scan** |
| I/O | 2 | - | - | C22 | 866 |
| I/O (DIN, D0) | 2 | P153 | D14 | D20 | 869 |
| I/O (DOUT, BUSY) | 2 | P154 | C15 | C21 | 872 |
| CCLK | 2 | P155 | D15 | B22 | 875 |
| $V_{CCO}$ | 2 | P156 | $V_{CCO}$ Bank 2* | $V_{CCO}$ Bank 2* | - |
| $V_{CCO}$ | 1 | P156 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| TDO | 2 | P157 | B14 | A21 | - |
| GND | - | P158 | GND* | GND* | - |
| TDI | - | P159 | A15 | B20 | - |
| I/O ($\overline{CS}$) | 1 | P160 | B13 | C19 | 0 |
| I/O ($\overline{WRITE}$) | 1 | P161 | C13 | A20 | 3 |
| I/O | 1 | - | - | B19 | 6 |
| I/O | 1 | - | - | C18 | 9 |
| I/O | 1 | - | C12 | D17 | 12 |
| GND | - | - | GND* | GND* | - |
| I/O | 1 | P162 | A14 | A19 | 15 |
| I/O | 1 | - | - | B18 | 18 |
| I/O | 1 | - | - | E16 | 21 |
| I/O | 1 | - | D12 | C17 | 24 |
| I/O | 1 | P163 | B12 | D16 | 27 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 1 | - | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| I/O, $V_{REF}$ | 1 | P164 | C11 | A18 | 30 |
| I/O | 1 | P165 | A13 | B17 | 33 |
| I/O | 1 | - | - | E15 | 36 |
| I/O | 1 | - | - | A17 | 39 |
| I/O | 1 | - | D11 | D15 | 42 |
| I/O | 1 | P166 | A12 | C16 | 45 |
| I/O | 1 | - | - | D14 | 48 |
| I/O, $V_{REF}$ | 1 | P167 | E11 | E14 | 51 |
| I/O | 1 | P168 | B11 | A16 | 54 |
| GND | - | P169 | GND* | GND* | - |
| $V_{CCO}$ | 1 | P170 | $V_{CCO}$ Bank 1* | $V_{CCO}$ Bank 1* | - |
| $V_{CCINT}$ | - | P171 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| I/O | 1 | P172 | A11 | C15 | 57 |
| I/O | 1 | P173 | C10 | B15 | 60 |
| I/O | 1 | - | - | A15 | 66 |
| I/O | 1 | - | - | F12 | 69 |

## Additional XC2S150 Package Pins

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

11/02/00

**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

11/02/00

## Additional XC2S150 Package Pins *(Continued)*

**FG456**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| F7 | F8 | F9 | F10 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U7 | U8 | U9 | U10 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A6 | A12 | A13 | A14 | B11 |
| B16 | C2 | C8 | C9 | D1 | D4 |
| D18 | D19 | E13 | E17 | E19 | F11 |
| G2 | G22 | H21 | J1 | J4 | K2 |
| K18 | K19 | L2 | L19 | M2 | M17 |
| M21 | N1 | P1 | P5 | P22 | R3 |
| R20 | R22 | U3 | U18 | V6 | W4 |
| W13 | W15 | W19 | Y5 | Y22 | AA1 |
| AA3 | AA9 | AA10 | AA11 | AA16 | AB7 |
| AB8 | AB12 | AB14 | AB21 | - | - |

11/02/00

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I, GCK0 | 4 | P80 | N8 | W12 | 636 |
| I/O | 4 | P81 | N9 | U12 | 640 |
| I/O | 4 | - | - | V12 | 646 |
| I/O | 4 | P82 | R9 | Y12 | 649 |
| I/O | 4 | - | N10 | AA12 | 652 |
| I/O | 4 | - | - | W13 | 655 |
| I/O | 4 | P83 | T9 | AB13 | 661 |
| I/O, $V_{REF}$ | 4 | P84 | P9 | AA13 | 664 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P85 | GND* | GND* | - |
| I/O | 4 | P86 | M10 | Y13 | 667 |
| I/O | 4 | P87 | R10 | V13 | 670 |
| I/O | 4 | - | - | AB14 | 673 |
| I/O | 4 | - | - | W14 | 676 |
| I/O | 4 | P88 | P10 | AA14 | 679 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | - | V14 | 682 |
| I/O | 4 | - | - | Y14 | 685 |
| I/O | 4 | - | - | W15 | 688 |
| I/O | 4 | P89 | T10 | AB15 | 691 |
| I/O | 4 | P90 | R11 | AA15 | 694 |
| $V_{CCINT}$ | - | P91 | $V_{CCINT}$* | $V_{CCINT}$* | - |
| $V_{CCO}$ | 4 | P92 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | P93 | GND* | GND* | - |
| I/O | 4 | P94 | M11 | Y15 | 697 |
| I/O, $V_{REF}$ | 4 | P95 | T11 | AB16 | 700 |
| I/O | 4 | - | - | AB17 | 706 |
| I/O | 4 | P96 | N11 | V15 | 709 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | R12 | Y16 | 712 |
| I/O | 4 | - | - | AA17 | 715 |
| I/O | 4 | - | - | W16 | 718 |
| I/O | 4 | P97 | P11 | AB18 | 721 |
| I/O, $V_{REF}$ | 4 | P98 | T12 | AB19 | 724 |
| $V_{CCO}$ | 4 | - | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | P99 | T13 | Y17 | 727 |
| I/O | 4 | - | N12 | V16 | 730 |
| I/O | 4 | - | - | AA18 | 733 |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | PQ208 | FG256 | FG456 | Bndry Scan |
|---|---|---|---|---|---|
| Function | Bank | | | | |
| I/O | 4 | - | - | W17 | 739 |
| I/O, $V_{REF}$ | 4 | P100 | R13 | AB20 | 742 |
| GND | - | - | GND* | GND* | - |
| I/O | 4 | - | P12 | AA19 | 745 |
| I/O | 4 | - | - | V17 | 748 |
| I/O | 4 | - | - | Y18 | 751 |
| I/O | 4 | P101 | P13 | AA20 | 757 |
| I/O | 4 | P102 | T14 | W18 | 760 |
| GND | - | P103 | GND* | GND* | - |
| DONE | 3 | P104 | R14 | Y19 | 763 |
| $V_{CCO}$ | 4 | P105 | $V_{CCO}$ Bank 4* | $V_{CCO}$ Bank 4* | - |
| $V_{CCO}$ | 3 | P105 | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| $\overline{\text{PROGRAM}}$ | - | P106 | P15 | W20 | 766 |
| I/O ($\overline{\text{INIT}}$) | 3 | P107 | N15 | V19 | 767 |
| I/O (D7) | 3 | P108 | N14 | Y21 | 770 |
| I/O | 3 | - | - | V20 | 776 |
| I/O | 3 | - | - | AA22 | 779 |
| I/O | 3 | - | T15 | W21 | 782 |
| GND | - | - | GND* | GND* | - |
| I/O, $V_{REF}$ | 3 | P109 | M13 | U20 | 785 |
| I/O | 3 | - | - | U19 | 788 |
| I/O | 3 | - | - | V21 | 794 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | - | R16 | T18 | 797 |
| I/O | 3 | P110 | M14 | W22 | 800 |
| GND | - | - | GND* | GND* | - |
| $V_{CCO}$ | 3 | - | $V_{CCO}$ Bank 3* | $V_{CCO}$ Bank 3* | - |
| I/O, $V_{REF}$ | 3 | P111 | L14 | U21 | 803 |
| I/O | 3 | P112 | M15 | T20 | 806 |
| I/O | 3 | - | - | T19 | 809 |
| I/O | 3 | - | - | V22 | 812 |
| I/O | 3 | - | L12 | T21 | 815 |
| GND | - | - | GND* | GND* | - |
| I/O | 3 | P113 | P16 | R18 | 818 |
| I/O | 3 | - | - | U22 | 821 |
| I/O, $V_{REF}$ | 3 | P114 | L13 | R19 | 827 |
| I/O (D6) | 3 | P115 | N16 | T22 | 830 |
| GND | - | P116 | GND* | GND* | - |

## XC2S200 Device Pinouts *(Continued)*

| XC2S200 Pad Name | | | | | |
|---|---|---|---|---|---|
| **Function** | **Bank** | **PQ208** | **FG256** | **FG456** | **Bndry Scan** |
| GND | - | P198 | GND* | GND* | - |
| I/O | 0 | P199 | A5 | B7 | 188 |
| I/O, $V_{REF}$ | 0 | P200 | C6 | E8 | 191 |
| I/O | 0 | - | - | D8 | 197 |
| I/O | 0 | P201 | B5 | C7 | 200 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | D6 | D7 | 203 |
| I/O | 0 | - | - | B6 | 206 |
| I/O | 0 | - | - | A5 | 209 |
| I/O | 0 | P202 | A4 | D6 | 212 |
| I/O, $V_{REF}$ | 0 | P203 | B4 | C6 | 215 |
| $V_{CCO}$ | 0 | - | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | P204 | E6 | B5 | 218 |
| I/O | 0 | - | D5 | E7 | 221 |
| I/O | 0 | - | - | A4 | 224 |
| I/O | 0 | - | - | E6 | 230 |
| I/O, $V_{REF}$ | 0 | P205 | A3 | B4 | 233 |
| GND | - | - | GND* | GND* | - |
| I/O | 0 | - | C5 | A3 | 236 |
| I/O | 0 | - | - | B3 | 239 |
| I/O | 0 | - | - | D5 | 242 |
| I/O | 0 | P206 | B3 | C5 | 248 |
| TCK | - | P207 | C4 | C4 | - |
| $V_{CCO}$ | 0 | P208 | $V_{CCO}$ Bank 0* | $V_{CCO}$ Bank 0* | - |
| $V_{CCO}$ | 7 | P208 | $V_{CCO}$ Bank 7* | $V_{CCO}$ Bank 7* | - |

04/18/01

**Notes:**

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, $V_{CCINT}$*, $V_{CCO}$ Bank 0*, $V_{CCO}$ Bank 1*, $V_{CCO}$ Bank 2*, $V_{CCO}$ Bank 3*, $V_{CCO}$ Bank 4*, $V_{CCO}$ Bank 5*, $V_{CCO}$ Bank 6*, $V_{CCO}$ Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on $V_{CCO}$ banking.

## Additional XC2S200 Package Pins

**PQ208**

| Not Connected Pins | | | | | |
|---|---|---|---|---|---|
| P55 | P56 | - | - | - | - |

11/02/00

**FG256**

| $V_{CCINT}$ Pins | | | | | |
|---|---|---|---|---|---|
| C3 | C14 | D4 | D13 | E5 | E12 |
| M5 | M12 | N4 | N13 | P3 | P14 |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| E8 | F8 | - | - | - | - |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| E9 | F9 | - | - | - | - |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| H11 | H12 | - | - | - | - |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| J11 | J12 | - | - | - | - |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| L9 | M9 | - | - | - | - |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| L8 | M8 | - | - | - | - |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| J5 | J6 | - | - | - | - |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| H5 | H6 | - | - | - | - |
| **GND Pins** | | | | | |
| A1 | A16 | B2 | B15 | F6 | F7 |
| F10 | F11 | G6 | G7 | G8 | G9 |
| G10 | G11 | H7 | H8 | H9 | H10 |
| J7 | J8 | J9 | J10 | K6 | K7 |
| K8 | K9 | K10 | K11 | L6 | L7 |
| L10 | L11 | R2 | R15 | T1 | T16 |
| **Not Connected Pins** | | | | | |
| P4 | R4 | - | - | - | - |

## Additional XC2S200 Package Pins *(Continued)*

11/02/00

**FG456**

| | | | | | |
|---|---|---|---|---|---|
| **$V_{CCINT}$ Pins** | | | | | |
| E5 | E18 | F6 | F17 | G7 | G8 |
| G9 | G14 | G15 | G16 | H7 | H16 |
| J7 | J16 | P7 | P16 | R7 | R16 |
| T7 | T8 | T9 | T14 | T15 | T16 |
| U6 | U17 | V5 | V18 | - | - |
| **$V_{CCO}$ Bank 0 Pins** | | | | | |
| F7 | F8 | F9 | F10 | G10 | G11 |
| **$V_{CCO}$ Bank 1 Pins** | | | | | |
| F13 | F14 | F15 | F16 | G12 | G13 |
| **$V_{CCO}$ Bank 2 Pins** | | | | | |
| G17 | H17 | J17 | K16 | K17 | L16 |
| **$V_{CCO}$ Bank 3 Pins** | | | | | |
| M16 | N16 | N17 | P17 | R17 | T17 |
| **$V_{CCO}$ Bank 4 Pins** | | | | | |
| T12 | T13 | U13 | U14 | U15 | U16 |
| **$V_{CCO}$ Bank 5 Pins** | | | | | |
| T10 | T11 | U7 | U8 | U9 | U10 |
| **$V_{CCO}$ Bank 6 Pins** | | | | | |
| M7 | N6 | N7 | P6 | R6 | T6 |
| **$V_{CCO}$ Bank 7 Pins** | | | | | |
| G6 | H6 | J6 | K6 | K7 | L7 |
| **GND Pins** | | | | | |
| A1 | A22 | B2 | B21 | C3 | C20 |
| J9 | J10 | J11 | J12 | J13 | J14 |
| K9 | K10 | K11 | K12 | K13 | K14 |
| L9 | L10 | L11 | L12 | L13 | L14 |
| M9 | M10 | M11 | M12 | M13 | M14 |
| N9 | N10 | N11 | N12 | N13 | N14 |
| P9 | P10 | P11 | P12 | P13 | P14 |
| Y3 | Y20 | AA2 | AA21 | AB1 | AB22 |
| **Not Connected Pins** | | | | | |
| A2 | A6 | A12 | B11 | B16 | C2 |
| D1 | D4 | D18 | D19 | E17 | E19 |
| G2 | G22 | L2 | L19 | M2 | M21 |
| R3 | R20 | U3 | U18 | V6 | W4 |
| W19 | Y5 | Y22 | AA1 | AA3 | AA11 |
| AA16 | AB7 | AB12 | AB21 | - | - |

11/02/00

## Revision History

| Version No. | Date | Description |
|---|---|---|
| 2.0 | 09/18/00 | Sectioned the Spartan-II Family data sheet into four modules. Corrected all known errors in the pinout tables. |
| 2.1 | 10/04/00 | Added notes requiring $\overline{\text{PWDN}}$ to be tied to $V_{CCINT}$ when unused. |
| 2.2 | 11/02/00 | Removed the Power Down feature. |
| 2.3 | 03/05/01 | Added notes on pinout tables for IRDY and TRDY. |
| 2.4 | 04/30/01 | Reinstated XC2S50 $V_{CCO}$ Bank 7, GND, and "not connected" pins missing in version 2.3. |
| 2.5 | 09/03/03 | Added caution about Not Connected Pins to XC2S30 pinout tables on page 76. |
| 2.8 | 06/13/08 | Added "Package Overview" section. Added notes to clarify shared $V_{CCO}$ banks. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8. |