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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	216
Number of Logic Elements/Cells	972
Total RAM Bits	24576
Number of I/O	92
Number of Gates	30000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s30-6tqg144c

General Overview

The Spartan-II family of FPGAs have a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs). There are four Delay-Locked Loops (DLLs), one at each corner of the die. Two columns of block RAM lie on opposite sides of the die, between the CLBs and the IOB columns. These functional elements are interconnected by a powerful hierarchy of versatile routing channels (see Figure 1).

Spartan-II FPGAs are customized by loading configuration data into internal static memory cells. Unlimited reprogramming cycles are possible with this approach. Stored values in these cells determine logic functions and interconnections implemented in the FPGA. Configuration data can be read from an external serial PROM (master serial mode), or written into the FPGA in slave serial, slave parallel, or Boundary Scan modes.

Spartan-II FPGAs are typically used in high-volume applications where the versatility of a fast programmable solution adds benefits. Spartan-II FPGAs are ideal for shortening product development cycles while offering a cost-effective solution for high volume production.

Spartan-II FPGAs achieve high-performance, low-cost operation through advanced architecture and semiconductor technology. Spartan-II devices provide system clock rates up to 200 MHz. In addition to the conventional benefits of high-volume programmable logic solutions, Spartan-II FPGAs also offer on-chip synchronous single-port and dual-port RAM (block and distributed form), DLL clock drivers, programmable set and reset on all flip-flops, fast carry logic, and many other features.

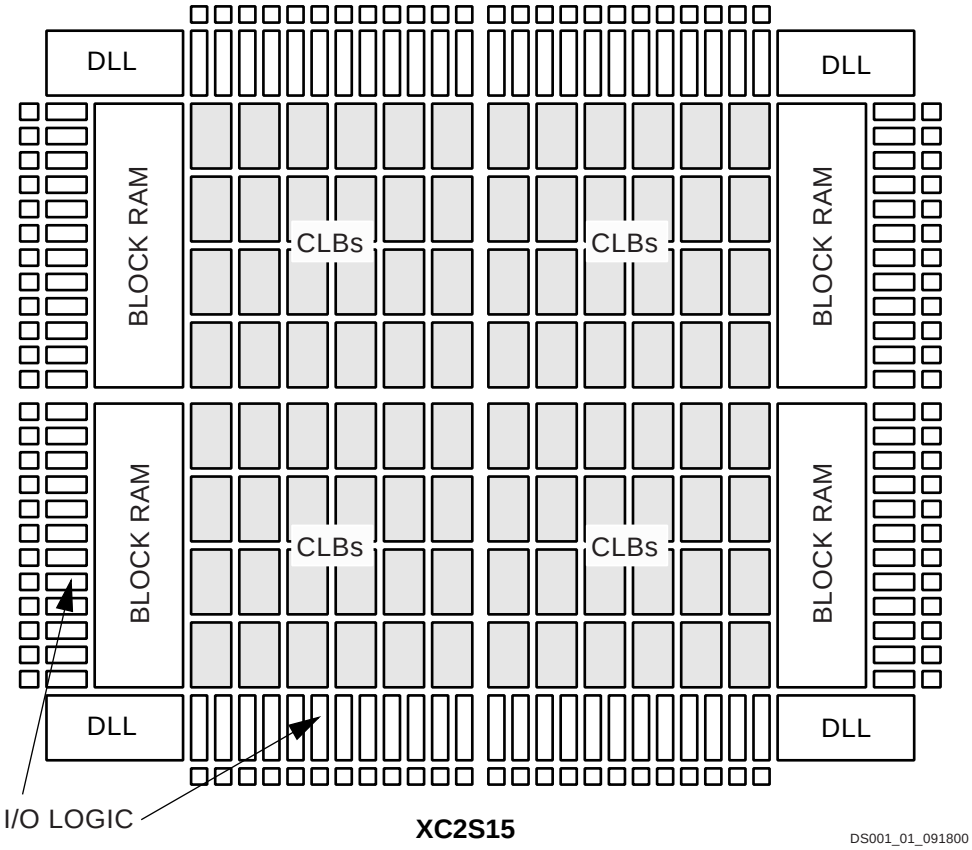

Figure 1: **Basic Spartan-II Family FPGA Block Diagram**

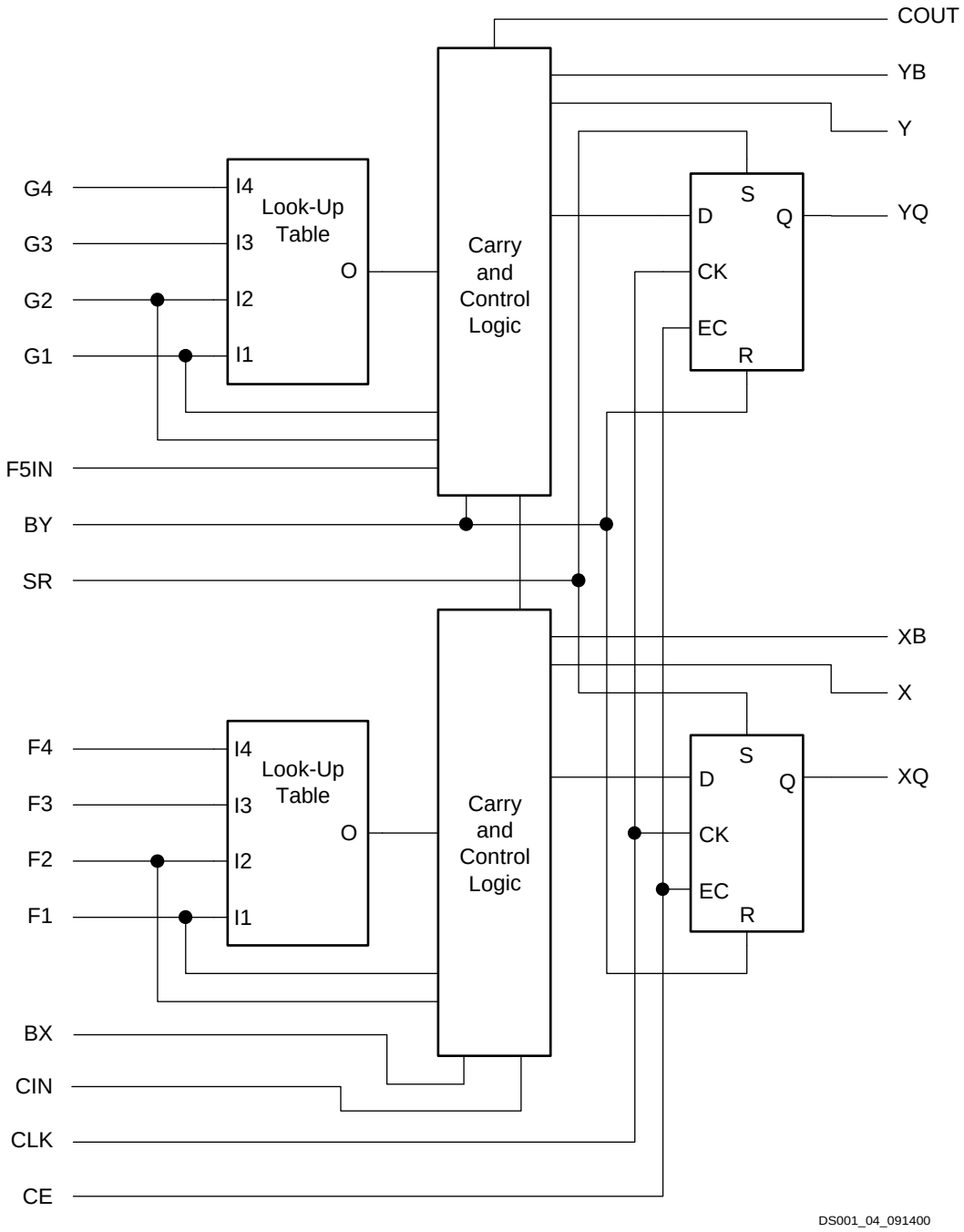

Figure 4: **Spartan-II CLB Slice** (two identical slices in each CLB)

Storage Elements

Storage elements in the Spartan-II FPGA slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

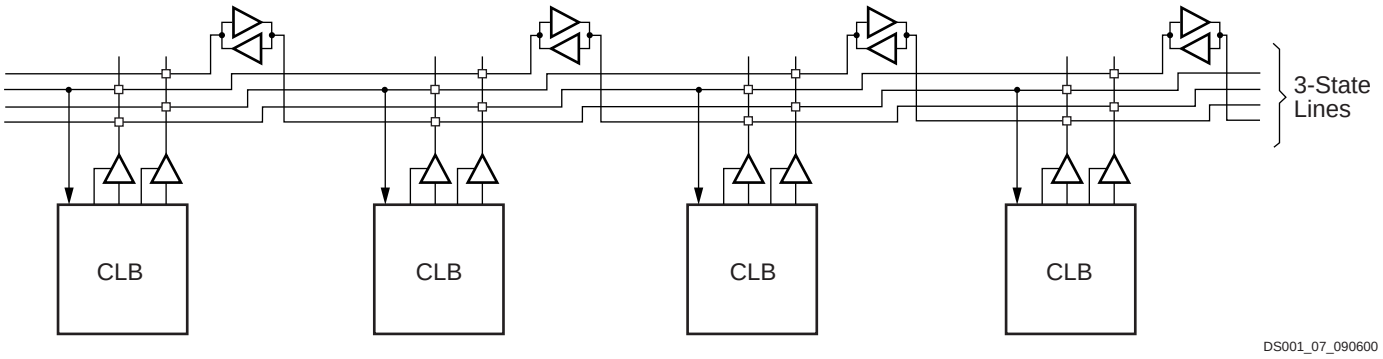

Figure 7: **BUFT Connections to Dedicated Horizontal Bus Lines**

Clock Distribution

The Spartan-II family provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 8.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing. Global clock pins do not have the option for internal, weak pull-up resistors.

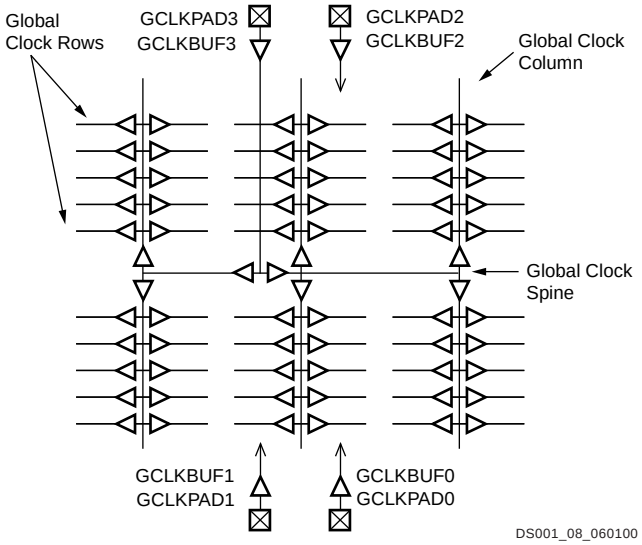

Figure 8: **Global Clock Distribution Network**

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks. The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-II devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

Boundary Scan

Spartan-II devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}. TDI, TMS, and TCK have a default internal weak pull-up resistor, and TDO has no default resistor. Bitstream options allow setting any of the four TAP pins to have an internal pull-up, pull-down, or neither.

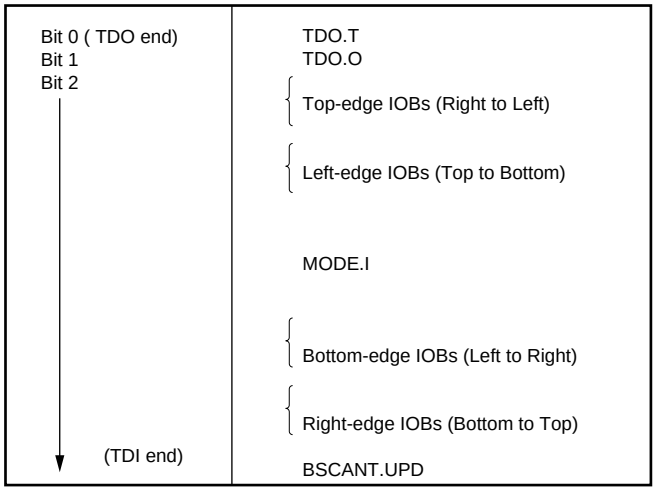

Figure 10: **Boundary Scan Bit Sequence**

Development System

Spartan-II FPGAs are supported by the Xilinx ISE® development tools. The basic methodology for Spartan-II FPGA design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation, while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under a single graphical interface, providing designers with a common user interface regardless of their choice of entry and verification tools. The software simplifies the selection of implementation options with pull-down menus and on-line help.

For HDL design entry, the Xilinx FPGA development system provides interfaces to several synthesis design environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-II FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The design environment supports hierarchical design entry. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the static timing analyzer.

For in-circuit debugging, the development system includes a download cable, which connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can read back the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

division factor N except for non-integer division in High Frequency (HF) mode. For division factor 1.5 the duty cycle in the HF mode is 33.3% High and 66.7% Low. For division factor 2.5, the duty cycle in the HF mode is 40.0% High and 60.0% Low.

1x Clock Outputs — CLK[0|90|180|270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 degree phase-shifted version. The relationship between phase shift and the corresponding period shift appears in Table 10.

The timing diagrams in Figure 26 illustrate the DLL clock output characteristics.

Table 10: **Relationship of Phase-Shifted Output Clock to Period Shift**

Phase (degrees)	Period Shift (percent)
0	0%
90	25%
180	50%
270	75%

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL primitive. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

Locked Output — LOCKED

In order to achieve lock, the DLL may need to sample several thousand clock cycles. After the DLL achieves lock the LOCKED signal activates. The "DLL Timing Parameters" section of Module 3 provides estimates for locking times.

In order to guarantee that the system clock is established prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement. In particular the CLK2X output will appear as a 1x clock with a 25/75 duty cycle.

DLL Properties

Properties provide access to some of the Spartan-II family DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, such that they exhibit a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL primitive.

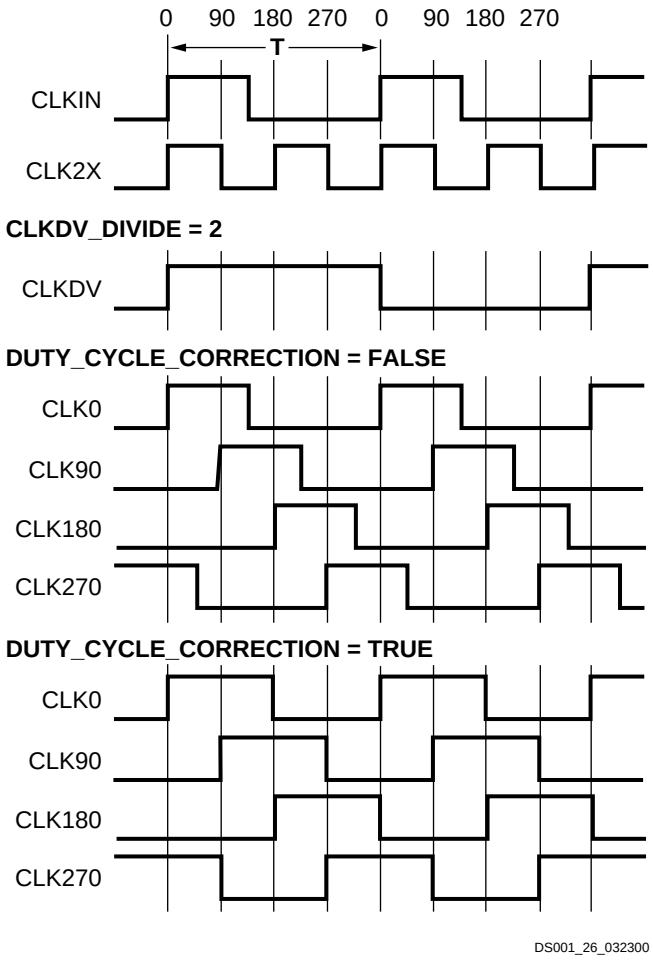

Figure 26: **DLL Output Characteristics**

Clock Divide Property

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the Startup Sequence following device configuration is paused at a user-specified point until the DLL locks. **XAPP176**: *Configuration and Readback of the Spartan-II and Spartan-IIE Families* explains how this can result in delaying the assertion of the DONE pin until the DLL locks.

DLL Location Constraints

The DLLs are distributed such that there is one DLL in each corner of the device. The location constraint LOC, attached to the DLL primitive with the numeric identifier 0, 1, 2, or 3, controls DLL location. The orientation of the four DLLs and their corresponding clock resources appears in Figure 27.

The LOC property uses the following form.

LOC = DLL2

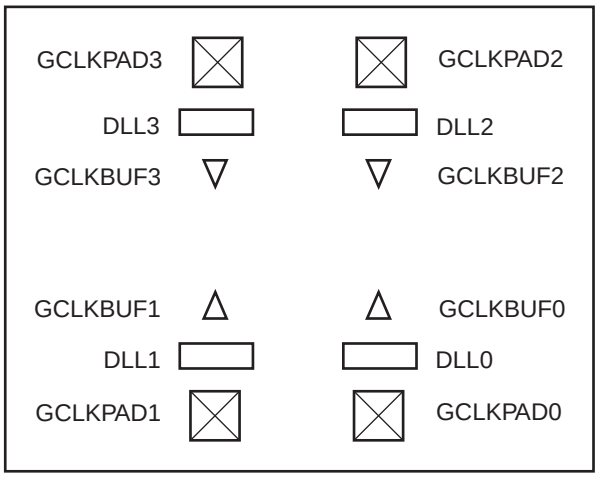

Figure 27: **Orientation of DLLs**

Design Considerations

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the "DLL Timing Parameters" section of the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock in a way that has little impact to the DLL. Stopping the clock should be limited to less than approximately 100 µs to keep device cooling to a minimum and maintain the validity of the current tap setting. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED will stay High and remain High when the clock is restored. If these conditions may not be met in the design, apply a manual reset to the DLL after re-starting the input clock, even if the LOCKED signal has not changed.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). One DLL output can drive more than one OBUF; however, this adds skew.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Table 11: **Available Library Primitives**

Primitive	Port A Width	Port B Width
RAMB4_S4 RAMB4_S4_S4 RAMB4_S4_S8 RAMB4_S4_S16	4	N/A 4 8 16
RAMB4_S8 RAMB4_S8_S8 RAMB4_S8_S16	8	N/A 8 16
RAMB4_S16 RAMB4_S16_S16	16	N/A 16

Port Signals

Each block RAM port operates independently of the others while accessing the same set of 4096 memory cells.

Table 12 describes the depth and width aspect ratios for the block RAM memory.

Table 12: **Block RAM Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A|B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A|B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A|B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A|B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 12.

Data In Bus—DI[A|B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 12.

Data Output Bus—DO[A|B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 12.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$Start = ([ADDR_{port} + 1] * Width_{port}) - 1$$

$$End = ADDR_{port} * Width_{port}$$

Table 13 shows low order address mapping for each port width.

Table 13: **Port Address Mapping**

Port Width	Port Addresses															
1	4095...	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

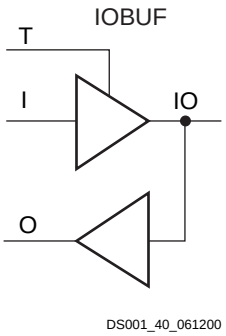

Figure 40: **Input/Output Buffer Primitiveprimitive (IOBUF)**

When the IOBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36, page 39 for a representation of the Spartan-II FPGA I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

IOB Flip-Flop/Latch Property

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified:

map -pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each Versatile I/O primitive with the location constraint LOC attached to the Versatile I/O primitive. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

LOC=A42

LOC=P37

Output Slew Rate Property

In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

Output Drive Strength Property

For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE=

SSTL3 Class I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 47. DC voltage specifications appear in Table 25 for the SSTL3_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

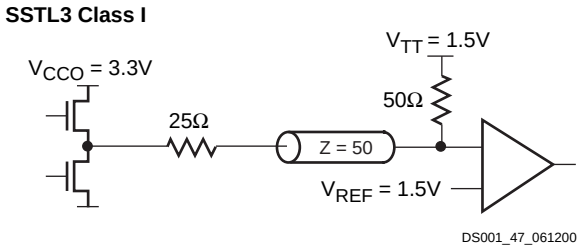

Figure 47: **Terminated SSTL3 Class I**

Table 25: **SSTL3_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.6$	1.9	-	-
$V_{OL} \leq V_{REF} - 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3.
2. V_{IL} minimum does not conform to the formula.

SSTL3 Class II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 48. DC voltage specifications appear in Table 26 for the SSTL3_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

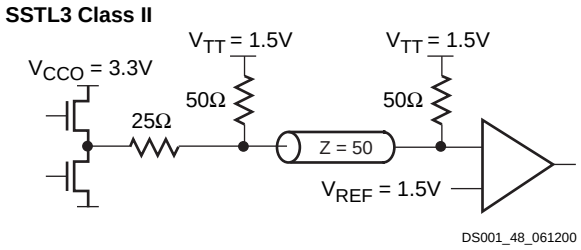

Figure 48: **Terminated SSTL3 Class II**

Table 26: **SSTL3_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} \geq V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} \leq V_{REF} - 0.2$	–0.3(2)	1.3	1.5
$V_{OH} \geq V_{REF} + 0.8$	2.1	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL} at V_{OL} (mA)	16	-	-

Notes:
1. V_{IH} maximum is V_{CCO} + 0.3
2. V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 49. DC voltage specifications appear in Table 27 for the SSTL2_I standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics

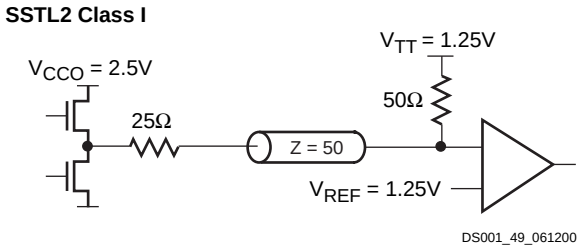

Figure 49: **Terminated SSTL2 Class I**

Table 27: **SSTL2_I Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \geq V_{REF} + 0.18$	1.33	1.43	$3.0^{(2)}$
$V_{IL} \leq V_{REF} - 0.18$	$-0.3^{(3)}$	1.07	1.17
$V_{OH} \geq V_{REF} + 0.61$	1.76	-	-
$V_{OL} \leq V_{REF} - 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL} at V_{OL} (mA)	7.6	-	-

Notes:
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

SSTL2 Class II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 50. DC voltage specifications appear in Table 28 for the SSTL2_II standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

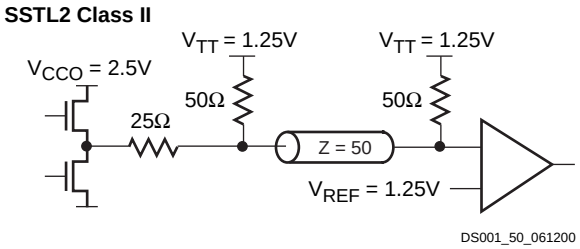

Figure 50: **Terminated SSTL2 Class II**

Table 28: **SSTL2_II Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N^{(1)}$	1.11	1.25	1.39
$V_{IH} \geq V_{REF} + 0.18$	1.33	1.43	$3.0^{(2)}$
$V_{IL} \leq V_{REF} - 0.18$	$-0.3^{(3)}$	1.07	1.17
$V_{OH} \geq V_{REF} + 0.8$	1.95	-	-
$V_{OL} \leq V_{REF} - 0.8$	-	-	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL} at V_{OL} (mA)	15.2	-	-

Notes:
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
T_J	Junction temperature(1)	Commercial	0	85	°C
		Industrial	–40	100	°C
V_{CCINT}	Supply voltage relative to GND(2,5)	Commercial	2.5 – 5%	2.5 + 5%	V
		Industrial	2.5 – 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND(3,5)	Commercial	1.4	3.6	V
		Industrial	1.4	3.6	V
T_{IN}	Input signal transition time(4)		-	250	ns

Notes:
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
2. Functional operation is guaranteed down to a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} – 10%). For every 50 mV reduction in V_{CCINT} below 2.375V (nominal V_{CCINT} – 5%), all delay parameters increase by 3%.
3. Minimum and maximum values for V_{CCO} vary according to the I/O standard selected.
4. Input and output measurement threshold is ~50% of V_{CCO}. See "Delay Measurement Methodology," page 60 for specific levels.
5. Supply voltages may be applied in any order desired.

DC Characteristics Over Operating Conditions

Symbol	Description			Min	Typ	Max	Units
V_{DRINT}	Data Retention V_{CCINT} voltage (below which configuration data may be lost)			2.0	-	-	V
V_{DRIO}	Data Retention V_{CCO} voltage (below which configuration data may be lost)			1.2	-	-	V
I_{CCINTQ}	Quiescent V_{CCINT} supply current(1)	XC2S15	Commercial	-	10	30	mA
			Industrial	-	10	60	mA
		XC2S30	Commercial	-	10	30	mA
			Industrial	-	10	60	mA
		XC2S50	Commercial	-	12	50	mA
			Industrial	-	12	100	mA
		XC2S100	Commercial	-	12	50	mA
			Industrial	-	12	100	mA
		XC2S150	Commercial	-	15	50	mA
			Industrial	-	15	100	mA
		XC2S200	Commercial	-	15	75	mA
			Industrial	-	15	150	mA
I_{CCOQ}	Quiescent V_{CCO} supply current(1)			-	-	2	mA
I_{REF}	V_{REF} current per V_{REF} pin			-	-	20	µA
I_L	Input or output leakage current(2)			–10	-	+10	µA
C_{IN}	Input capacitance (sample tested)	VQ, CS, TQ, PQ, FG packages		-	-	8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)(3)			-	-	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested)(3)			-	-	0.15	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. The I/O leakage current specification applies only when the V_{CCINT} and V_{CCO} supply voltages have reached their respective minimum Recommended Operating Conditions.
3. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not provide valid logic levels when input pins are connected to other circuits.

Clock Distribution Guidelines(1)

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
GCLK Clock Skew				
$T_{GSKEWIOB}$	Global clock skew between IOB flip-flops	0.13	0.14	ns

Notes:
1. These clock distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

T_{GPIO} is specified for LVTTL levels. For other standards, adjust T_{GPIO} with the values shown in "I/O Standard Global Clock Input Adjustments".

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
GCLK IOB and Buffer				
T_{GPIO}	Global clock pad to output	0.7	0.8	ns
T_{GIO}	Global clock buffer I input to O output	0.7	0.8	ns

I/O Standard Global Clock Input Adjustments

Delays associated with a global clock input pad are specified for LVTTL levels. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Data Input Delay Adjustments					
$T_{GPLVTTL}$	Standard-specific global clock input delay adjustments	LVTTL	0	0	ns
$T_{GPLVCMOS2}$		LVCMOS2	–0.04	–0.05	ns
$T_{GPPCI33\_3}$		PCI, 33 MHz, 3.3V	–0.11	–0.13	ns
$T_{GPPCI33\_5}$		PCI, 33 MHz, 5.0V	0.26	0.30	ns
$T_{GPPCI66\_3}$		PCI, 66 MHz, 3.3V	–0.11	–0.13	ns
T_{GPGTL}		GTL	0.80	0.84	ns
T_{GPGTLP}		GTL+	0.71	0.73	ns
T_{GPHSTL}		HSTL	0.63	0.64	ns
$T_{GPSSTL2}$		SSTL2	0.52	0.51	ns
$T_{GPSSTL3}$		SSTL3	0.56	0.55	ns
T_{GPCTT}		CTT	0.62	0.62	ns
T_{GPAGP}		AGP	0.54	0.53	ns

Notes:
1. Input timing for GPLVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.

Block RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Sequential Delays						
T_{BCKO}	Clock CLK to DOUT output	-	3.4	-	4.0	ns
Setup/Hold Times with Respect to Clock CLK (1)						
T_{BACK} / T_{BCKA}	ADDR inputs	1.4 / 0	-	1.4 / 0	-	ns
T_{BDCK}/ T_{BCKD}	DIN inputs	1.4 / 0	-	1.4 / 0	-	ns
T_{BECK}/ T_{BCKE}	EN inputs	2.9 / 0	-	3.2 / 0	-	ns
T_{BRCK}/ T_{BCKR}	RST input	2.7 / 0	-	2.9 / 0	-	ns
T_{BWCK}/ T_{BCKW}	WEN input	2.6 / 0	-	2.8 / 0	-	ns
Clock CLK						
T_{BPWH}	Minimum pulse width, High	-	1.9	-	1.9	ns
T_{BPWL}	Minimum pulse width, Low	-	1.9	-	1.9	ns
T_{BCCS}	CLKA -> CLKB setup time for different ports	-	3.0	-	4.0	ns

Notes:
1. A zero hold time listing indicates no hold time or a negative hold time.

TBUF Switching Characteristics

Symbol	Description	Speed Grade		Units
		-6	-5	
		Max	Max	
Combinatorial Delays				
T_{IO}	IN input to OUT output	0	0	ns
T_{OFF}	TRI input to OUT output high impedance	0.1	0.2	ns
T_{ON}	TRI input to valid data on OUT output	0.1	0.2	ns

JTAG Test Access Port Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Setup and Hold Times with Respect to TCK						
T_{TAPTCK} / T_{TCKTAP}	TMS and TDI setup and hold times	4.0 / 2.0	-	4.0 / 2.0	-	ns
Sequential Delays						
T_{TCKTDO}	Output delay from clock TCK to output TDO	-	11.0	-	11.0	ns
FTCK	Maximum TCK clock frequency	-	33	-	33	MHz

Introduction

This section describes how the various pins on a Spartan®-II FPGA connect within the supported component packages, and provides device-specific thermal characteristics. Spartan-II FPGAs are available in both standard and Pb-free, RoHS versions of each package, with the Pb-free version adding a “G” to the middle of the package code. Except for the thermal characteristics, all information for the standard package applies equally to the Pb-free package.

Pin Types

Most pins on a Spartan-II FPGA are general-purpose, user-defined I/O pins. There are, however, different functional types of pins on Spartan-II FPGA packages, as outlined in Table 35.

Table 35: **Pin Definitions**

Pin Name	Dedicated	Direction	Description
GCK0, GCK1, GCK2, GCK3	No	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin. It is an input for slave-parallel and slave-serial modes, and output in master-serial mode.
$\overline{\text{PROGRAM}}$	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
$\overline{\text{INIT}}$	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. This pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained. In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. This pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In Slave Parallel mode, D0-D7 are configuration data input pins. During readback, D0-D7 are output pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{\text{WRITE}}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{\text{CS}}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. This pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary Scan Test Access Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	Power supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power supply pins for output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground.
IRDY, TRDY	No	See PCI core documentation	These signals can only be accessed when using Xilinx® PCI cores. If the cores are not used, these pins are available as user I/Os.

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
V_{CCINT}	-	-	P38	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	6	-	P39	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P119	P40	GND*	GND*	-
I/O	6	P118	P41	K4	T1	314
I/O, V_{REF}	6	P117	P42	M1	R4	317
I/O	6	-	-	-	T2	320
I/O	6	P116	P43	L4	U1	323
I/O	6	-	-	M2	R5	326
I/O	6	-	P44	L3	U2	332
I/O, V_{REF}	6	P115	P45	N1	T3	335
V_{CCO}	6	-	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	-	-	GND*	GND*	-
I/O	6	-	P46	P1	T4	338
I/O	6	-	-	L5	W1	341
I/O	6	-	-	-	U4	344
I/O	6	P114	P47	N2	Y1	347
I/O	6	-	-	M4	W2	350
I/O	6	P113	P48	R1	Y2	356
I/O	6	P112	P49	M3	W3	359
M1	-	P111	P50	P2	U5	362
GND	-	P110	P51	GND*	GND*	-
M0	-	P109	P52	N3	AB2	363
V_{CCO}	6	P108	P53	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
V_{CCO}	5	P107	P53	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
M2	-	P106	P54	R3	Y4	364
I/O	5	-	-	N5	V7	374
I/O	5	P103	P57	T2	Y6	377
I/O	5	-	-	-	AA4	380
I/O	5	-	-	P5	W6	383
I/O	5	-	P58	T3	Y7	386
GND	-	-	-	GND*	GND*	-
V_{CCO}	5	-	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P102	P59	T4	AA5	389
I/O	5	-	P60	M6	AB5	392
I/O	5	-	-	T5	AB6	398
I/O	5	P101	P61	N6	AA7	401
I/O	5	-	-	-	W7	404

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
I/O, V_{REF}	5	P100	P62	R5	W8	407
I/O	5	P99	P63	P6	Y8	410
GND	-	P98	P64	GND*	GND*	-
V_{CCO}	5	-	P65	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCINT}	-	P97	P66	V_{CCINT}*	V_{CCINT}*	-
I/O	5	P96	P67	R6	AA8	413
I/O	5	P95	P68	M7	V9	416
I/O	5	-	-	-	AB9	419
I/O	5	-	P69	N7	Y9	422
I/O	5	-	P70	T6	W10	428
I/O	5	-	P71	P7	AB10	431
GND	-	-	P72	GND*	GND*	-
I/O, V_{REF}	5	P94	P73	P8	Y10	434
I/O	5	-	P74	R7	V11	437
I/O	5	-	-	T7	W11	440
I/O	5	P93	P75	T8	AB11	443
V_{CCINT}	-	P92	P76	V_{CCINT}*	V_{CCINT}*	-
I, GCK1	5	P91	P77	R8	Y11	455
V_{CCO}	5	P90	P78	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCO}	4	P90	P78	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P89	P79	GND*	GND*	-
I, GCK0	4	P88	P80	N8	W12	456
I/O	4	P87	P81	N9	U12	460
I/O	4	P86	P82	R9	Y12	466
I/O	4	-	-	N10	AA12	469
I/O	4	-	P83	T9	AB13	472
I/O, V_{REF}	4	P85	P84	P9	AA13	475
GND	-	-	P85	GND*	GND*	-
I/O	4	-	P86	M10	Y13	478
I/O	4	-	P87	R10	V13	481
I/O	4	-	P88	P10	AA14	487
I/O	4	-	-	-	V14	490
I/O	4	P84	P89	T10	AB15	493
I/O	4	P83	P90	R11	AA15	496
V_{CCINT}	-	P82	P91	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	4	-	P92	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P81	P93	GND*	GND*	-
I/O	4	P80	P94	M11	Y15	499

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name						
Function	Bank	TQ144	PQ208	FG256	FG456	Bndry Scan
I/O, V_{REF}	4	P79	P95	T11	AB16	502
I/O	4	-	-	-	AB17	505
I/O	4	P78	P96	N11	V15	508
I/O	4	-	-	R12	Y16	511
I/O	4	-	P97	P11	AB18	517
I/O, V_{REF}	4	P77	P98	T12	AB19	520
V_{CCO}	4	-	-	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	-	-	GND*	GND*	-
I/O	4	-	P99	T13	Y17	523
I/O	4	-	-	N12	V16	526
I/O	4	-	-	-	W17	529
I/O	4	P76	P100	R13	AB20	532
I/O	4	-	-	P12	AA19	535
I/O	4	P75	P101	P13	AA20	541
I/O	4	P74	P102	T14	W18	544
GND	-	P73	P103	GND*	GND*	-
DONE	3	P72	P104	R14	Y19	547
V_{CCO}	4	P71	P105	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
V_{CCO}	3	P70	P105	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
$\overline{PROGRAM}$	-	P69	P106	P15	W20	550
I/O ($\overline{INIT}$)	3	P68	P107	N15	V19	551
I/O (D7)	3	P67	P108	N14	Y21	554
I/O	3	-	-	T15	W21	560
I/O	3	P66	P109	M13	U20	563
I/O	3	-	-	-	U19	566
I/O	3	-	-	R16	T18	569
I/O	3	-	P110	M14	W22	572
GND	-	-	-	GND*	GND*	-
V_{CCO}	3	-	-	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
I/O, V_{REF}	3	P65	P111	L14	U21	575
I/O	3	-	P112	M15	T20	578
I/O	3	-	-	L12	T21	584
I/O	3	P64	P113	P16	R18	587
I/O	3	-	-	-	U22	590
I/O, V_{REF}	3	P63	P114	L13	R19	593
I/O (D6)	3	P62	P115	N16	T22	596
GND	-	P61	P116	GND*	GND*	-

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name						
Function	Bank	TQ144	PQ208	FG256	FG456	Bndry Scan
V_{CCO}	3	-	P117	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
V_{CCINT}	-	-	P118	V_{CCINT}*	V_{CCINT}*	-
I/O (D5)	3	P60	P119	M16	R21	599
I/O	3	P59	P120	K14	P18	602
I/O	3	-	-	L16	P20	605
I/O	3	-	P121	K13	P21	608
I/O	3	-	P122	L15	N18	614
I/O	3	-	P123	K12	N20	617
GND	-	-	P124	GND*	GND*	-
I/O, V_{REF}	3	P58	P125	K16	N21	620
I/O (D4)	3	P57	P126	J16	N22	623
I/O	3	-	-	J14	M19	626
I/O	3	P56	P127	K15	M20	629
V_{CCINT}	-	P55	P128	E5	V_{CCINT}*	-
I/O, TRDY(1)	3	P54	P129	J15	M22	638
V_{CCO}	3	P53	P130	V_{CCO} Bank 3*	V_{CCO} Bank 3*	-
V_{CCO}	2	P53	P130	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	P52	P131	GND*	GND*	-
I/O, IRDY(1)	2	P51	P132	H16	L20	641
I/O	2	-	P133	H14	L17	644
I/O	2	P50	P134	H15	L21	650
I/O	2	-	-	J13	L22	653
I/O (D3)	2	P49	P135	G16	K20	656
I/O, V_{REF}	2	P48	P136	H13	K21	659
GND	-	-	P137	GND*	GND*	-
I/O	2	-	P138	G14	K22	662
I/O	2	-	P139	G15	J21	665
I/O	2	-	P140	G12	J18	671
I/O	2	-	-	F16	J22	674
I/O	2	P47	P141	G13	H19	677
I/O (D2)	2	P46	P142	F15	H20	680
V_{CCINT}	-	-	P143	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	2	-	P144	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	P45	P145	GND*	GND*	-
I/O (D1)	2	P44	P146	E16	H22	683
I/O, V_{REF}	2	P43	P147	F14	H18	686
I/O	2	-	-	-	G21	689
I/O	2	P42	P148	D16	G18	692

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name						
Function	Bank	TQ144	PQ208	FG256	FG456	Bndry Scan
I/O	0	-	P188	A6	C10	107
I/O, V_{REF}	0	P12	P189	B7	A9	110
GND	-	-	P190	GND*	GND*	-
I/O	0	-	P191	C8	B9	113
I/O	0	-	P192	D7	E10	116
I/O	0	-	P193	E7	A8	122
I/O	0	-	-	-	D9	125
I/O	0	P11	P194	C7	E9	128
I/O	0	P10	P195	B6	A7	131
V_{CCINT}	-	P9	P196	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	0	-	P197	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
GND	-	P8	P198	GND*	GND*	-
I/O	0	P7	P199	A5	B7	134
I/O, V_{REF}	0	P6	P200	C6	E8	137
I/O	0	-	-	-	D8	140
I/O	0	-	P201	B5	C7	143
I/O	0	-	-	D6	D7	146
I/O	0	-	P202	A4	D6	152
I/O, V_{REF}	0	P5	P203	B4	C6	155
V_{CCO}	0	-	-	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
GND	-	-	-	GND*	GND*	-
I/O	0	-	P204	E6	B5	158
I/O	0	-	-	D5	E7	161
I/O	0	-	-	-	E6	164
I/O	0	P4	P205	A3	B4	167
I/O	0	-	-	C5	A3	170
I/O	0	P3	P206	B3	C5	176
TCK	-	P2	P207	C4	C4	-
V_{CCO}	0	P1	P208	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
V_{CCO}	7	P144	P208	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-

04/18/01

Notes:

1. IRDY and TRDY can only be accessed when using Xilinx PCI cores.
2. Pads labelled GND*, V_{CCINT}*, V_{CCO} Bank 0*, V_{CCO} Bank 1*, V_{CCO} Bank 2*, V_{CCO} Bank 3*, V_{CCO} Bank 4*, V_{CCO} Bank 5*, V_{CCO} Bank 6*, V_{CCO} Bank 7* are internally bonded to independent ground or power planes within the package.
3. See "VCCO Banks" for details on V_{CCO} banking.

Additional XC2S100 Package Pins

TQ144

Not Connected Pins					
P104	P105	-	-	-	-

11/02/00

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

11/02/00

FG256

V_{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V_{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V_{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V_{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V_{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V_{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V_{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V_{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V_{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

11/02/00

FG456

V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					

Additional XC2S100 Package Pins *(Continued)*

F10	F7	F8	F9	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U10	U7	U8	U9
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A4	A5	A6	A12	A13
A14	A15	A17	B3	B6	B8
B11	B14	B16	B19	C1	C2
C8	C9	C12	C18	C22	D1
D4	D5	D10	D18	D19	D21
E4	E11	E13	E15	E16	E17
E19	E22	F4	F11	F22	G2
G3	G4	G19	G22	H1	H21
J1	J3	J4	J19	J20	K2
K18	K19	L2	L5	L18	L19
M2	M6	M17	M18	M21	N1
N5	N19	P1	P5	P19	P22
R1	R3	R20	R22	T5	T19
U3	U11	U18	V1	V2	V10
V12	V17	V3	V4	V6	V8
V20	V21	V22	W4	W5	W9
W13	W14	W15	W16	W19	Y5
Y14	Y18	Y22	AA1	AA3	AA6
AA9	AA10	AA11	AA16	AA17	AA18
AA22	AB3	AB4	AB7	AB8	AB12
AB14	AB21	-	-	-	-

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Additional XC2S150 Package Pins

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

11/02/00

FG256

V_{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V_{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V_{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V_{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V_{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V_{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V_{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V_{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V_{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

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Additional XC2S150 Package Pins *(Continued)*

FG456

V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					
F7	F8	F9	F10	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U7	U8	U9	U10
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A6	A12	A13	A14	B11
B16	C2	C8	C9	D1	D4
D18	D19	E13	E17	E19	F11
G2	G22	H21	J1	J4	K2
K18	K19	L2	L19	M2	M17
M21	N1	P1	P5	P22	R3
R20	R22	U3	U18	V6	W4
W13	W15	W19	Y5	Y22	AA1
AA3	AA9	AA10	AA11	AA16	AB7
AB8	AB12	AB14	AB21	-	-

11/02/00

XC2S200 Device Pinouts

XC2S200 Pad Name					
Function	Bank	PQ208	FG256	FG456	Bndry Scan
GND	-	P1	GND*	GND*	-
TMS	-	P2	D3	D3	-
I/O	7	P3	C2	B1	257
I/O	7	-	-	E4	263
I/O	7	-	-	C1	266
I/O	7	-	A2	F5	269
GND	-	-	GND*	GND*	-
I/O, V_{REF}	7	P4	B1	D2	272
I/O	7	-	-	E3	275
I/O	7	-	-	F4	281
GND	-	-	GND*	GND*	-
I/O	7	-	E3	G5	284
I/O	7	P5	D2	F3	287
GND	-	-	GND*	GND*	-
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P6	C1	E2	290
I/O	7	P7	F3	E1	293
I/O	7	-	-	G4	296
I/O	7	-	-	G3	299
I/O	7	-	E2	H5	302
GND	-	-	GND*	GND*	-
I/O	7	P8	E4	F2	305
I/O	7	-	-	F1	308
I/O, V_{REF}	7	P9	D1	H4	314
I/O	7	P10	E1	G1	317
GND	-	P11	GND*	GND*	-
V_{CCO}	7	P12	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCINT}	-	P13	V_{CCINT}*	V_{CCINT}*	-
I/O	7	P14	F2	H3	320
I/O	7	P15	G3	H2	323
I/O	7	-	-	J4	326
I/O	7	-	-	H1	329
I/O	7	-	F1	J5	332
GND	-	-	GND*	GND*	-
I/O	7	P16	F4	J2	335
I/O	7	-	-	J3	338
I/O	7	-	-	J1	341
I/O	7	P17	F5	K5	344
I/O	7	P18	G2	K1	347
GND	-	P19	GND*	GND*	-

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name					
Function	Bank	PQ208	FG256	FG456	Bndry Scan
V_{CCO}	7	-	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
I/O, V_{REF}	7	P20	H3	K3	350
I/O	7	P21	G4	K4	353
I/O	7	-	-	K2	359
I/O	7	-	H2	L6	362
I/O	7	P22	G5	L1	365
I/O	7	-	-	L5	368
I/O	7	P23	H4	L4	374
I/O, IRDY(1)	7	P24	G1	L3	377
GND	-	P25	GND*	GND*	-
V_{CCO}	7	P26	V_{CCO} Bank 7*	V_{CCO} Bank 7*	-
V_{CCO}	6	P26	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
I/O, TRDY(1)	6	P27	J2	M1	380
V_{CCINT}	-	P28	V_{CCINT}*	V_{CCINT}*	-
I/O	6	-	-	M6	389
I/O	6	P29	H1	M3	392
I/O	6	-	J4	M4	395
I/O	6	-	-	N1	398
I/O	6	P30	J1	M5	404
I/O, V_{REF}	6	P31	J3	N2	407
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P32	GND*	GND*	-
I/O	6	P33	K5	N3	410
I/O	6	P34	K2	N4	413
I/O	6	-	-	P1	416
I/O	6	-	-	N5	419
I/O	6	P35	K1	P2	422
GND	-	-	GND*	GND*	-
I/O	6	-	K3	P4	425
I/O	6	-	-	R1	428
I/O	6	-	-	P5	431
I/O	6	P36	L1	P3	434
I/O	6	P37	L2	R2	437
V_{CCINT}	-	P38	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	6	P39	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P40	GND*	GND*	-
I/O	6	P41	K4	T1	440
I/O, V_{REF}	6	P42	M1	R4	443