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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	384
Number of Logic Elements/Cells	1728
Total RAM Bits	32768
Number of I/O	92
Number of Gates	50000
Voltage - Supply	2.375V ~ 2.625V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LQFP
Supplier Device Package	144-TQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xc2s50-5tq144c

Spartan-II FPGA Family: Introduction and Ordering Information

DS001-1 (v2.8) June 13, 2008

Product Specification

Introduction

The Spartan®-II Field-Programmable Gate Array family gives users high performance, abundant logic resources, and a rich feature set, all at an exceptionally low price. The six-member family offers densities ranging from 15,000 to 200,000 system gates, as shown in Table 1. System performance is supported up to 200 MHz. Features include block RAM (to 56K bits), distributed RAM (to 75,264 bits), 16 selectable I/O standards, and four DLLs. Fast, predictable interconnect means that successive design iterations continue to meet timing requirements.

The Spartan-II family is a superior alternative to mask-programmed ASICs. The FPGA avoids the initial cost, lengthy development cycles, and inherent risk of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary (impossible with ASICs).

Features

- Second generation ASIC replacement technology
  - Densities as high as 5,292 logic cells with up to 200,000 system gates
  - Streamlined features based on Virtex® FPGA architecture
  - Unlimited reprogrammability
  - Very low cost
  - Cost-effective 0.18 micron process
- System level features
  - SelectRAM™ hierarchical memory:
    - 16 bits/LUT distributed RAM
    - Configurable 4K bit block RAM
    - Fast interfaces to external RAM
  - Fully PCI compliant
  - Low-power segmented routing architecture
  - Full readback ability for verification/observability
  - Dedicated carry logic for high-speed arithmetic
  - Efficient multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with enable, set, reset
  - Four dedicated DLLs for advanced clock control
  - Four primary low-skew global clock distribution nets
  - IEEE 1149.1 compatible boundary scan logic
- Versatile I/O and packaging
  - Pb-free package options
  - Low-cost packages available in all densities
  - Family footprint compatibility in common packages
  - 16 high-performance interface standards
  - Hot swap Compact PCI friendly
  - Zero hold time simplifies system timing
- Core logic powered at 2.5V and I/Os powered at 1.5V, 2.5V, or 3.3V
- Fully supported by powerful Xilinx® ISE® development system
  - Fully automatic mapping, placement, and routing

Table 1: **Spartan-II FPGA Family Members**

Device	Logic Cells	System Gates (Logic and RAM)	CLB Array (R x C)	Total CLBs	Maximum Available User I/O(1)	Total Distributed RAM Bits	Total Block RAM Bits
XC2S15	432	15,000	8 x 12	96	86	6,144	16K
XC2S30	972	30,000	12 x 18	216	92	13,824	24K
XC2S50	1,728	50,000	16 x 24	384	176	24,576	32K
XC2S100	2,700	100,000	20 x 30	600	176	38,400	40K
XC2S150	3,888	150,000	24 x 36	864	260	55,296	48K
XC2S200	5,292	200,000	28 x 42	1,176	284	75,264	56K

Notes:

1. All user I/O counts do not include the four global clock/user input pins. See details in Table 2, page 4.

Spartan-II Product Availability

Table 2 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination. The four global clock pins are usable as additional user I/Os when not used as a global clock pin. These pins are not included in user I/O counts.

Table 2: **Spartan-II FPGA User I/O Chart(1)**

Device	Maximum User I/O	Available User I/O According to Package Type					
		VQ100 VQG100	TQ144 TQG144	CS144 CSG144	PQ208 PQG208	FG256 FGG256	FG456 FGG456
XC2S15	86	60	86	(Note 2)	-	-	-
XC2S30	92	60	92	92	(Note 2)	-	-
XC2S50	176	-	92	-	140	176	-
XC2S100	176	-	92	-	140	176	(Note 2)
XC2S150	260	-	-	-	140	176	260
XC2S200	284	-	-	-	140	176	284

Notes:
1. All user I/O counts do not include the four global clock/user input pins.
2. Discontinued by PDN2004-01.

Figure 9 is a diagram of the Spartan-II family boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

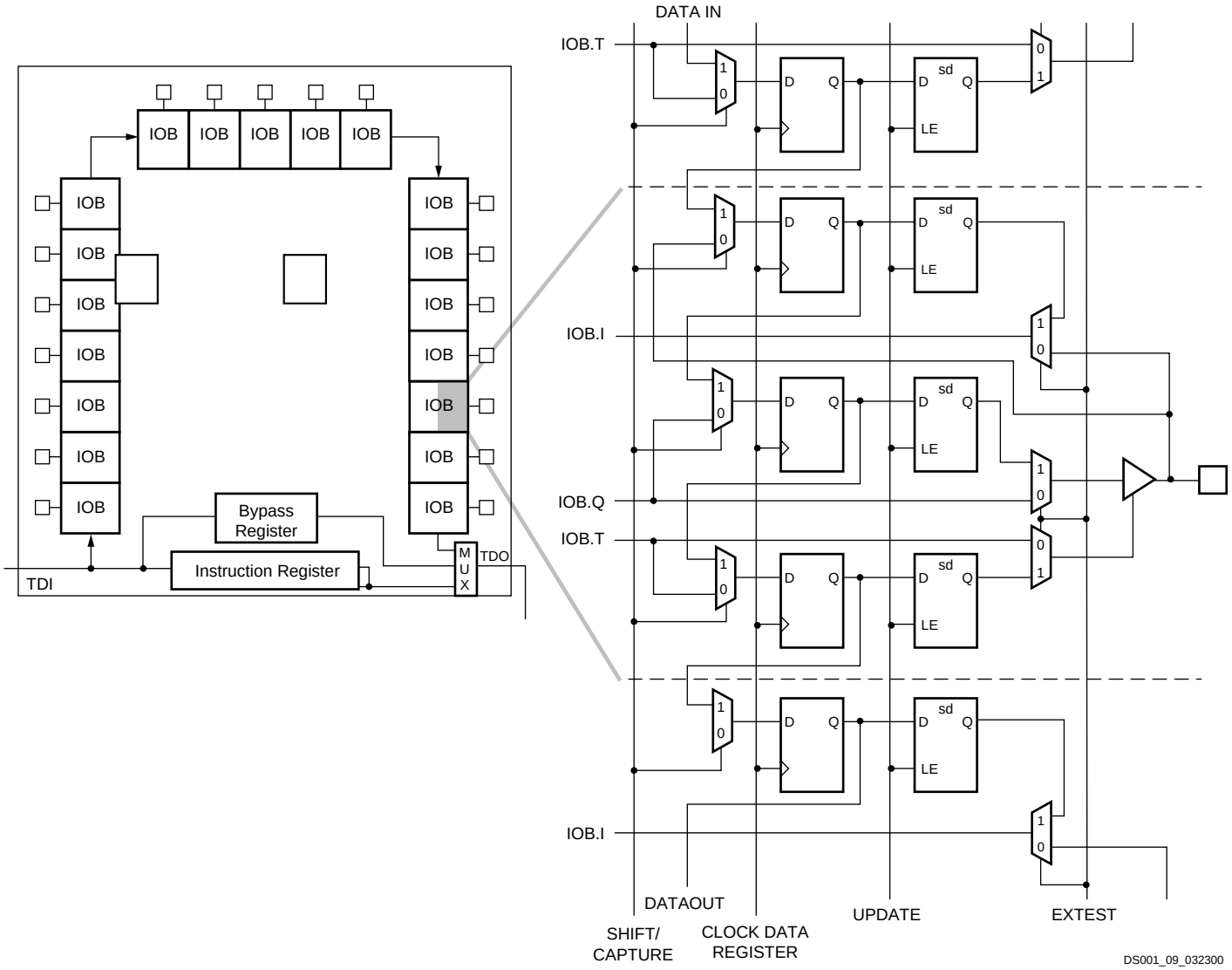


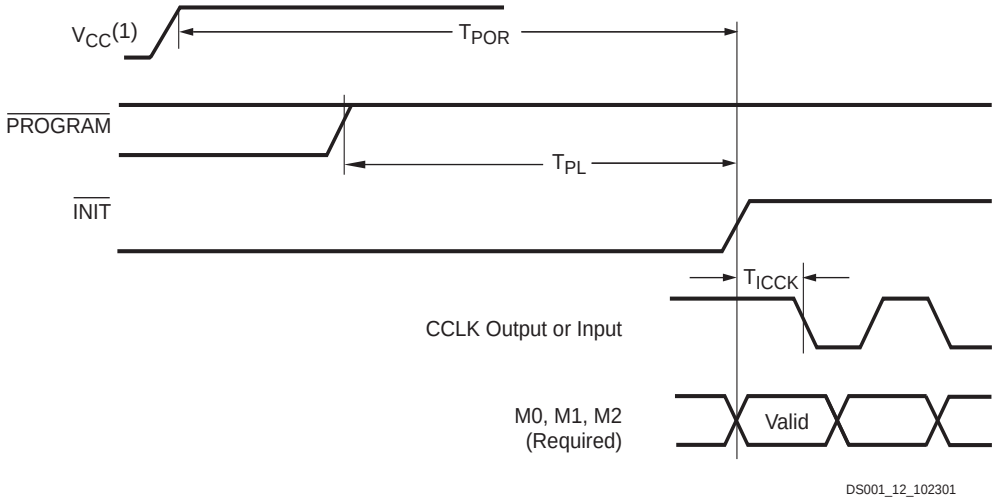
Figure 9: **Spartan-II Family Boundary Scan Logic**

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II family devices are available on the Xilinx website, in the Downloads area.



Symbol	Description	Min	Max
T_{POR}	Power-on reset	-	2 ms
T_{PL}	Program latency	-	100 µs
T_{ICCK}	CCLK output delay (Master Serial mode only)	0.5 µs	4 µs
$T_{PROGRAM}$	Program pulse width	300 ns	-

Notes: (referring to waveform above:)
1. Before configuration can begin, V_{CCINT} must be greater than 1.6V and V_{CCO} Bank 2 must be greater than 1.0V.

Figure 12: **Configuration Timing on Power-Up**

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving $\overline{INIT}$ Low. At this time, the user can delay configuration by holding either $\overline{PROGRAM}$ or $\overline{INIT}$ Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional $\overline{INIT}$ line is driving a Low logic level during memory clearing. To avoid contention, use an open-drain driver to keep $\overline{INIT}$ Low.

With no delay in force, the device indicates that the memory is completely clear by driving $\overline{INIT}$ High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data

Once $\overline{INIT}$ is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 14. Loading data using the Slave Parallel mode is shown in Figure 19, page 25.

CRC Error Checking

During the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives $\overline{INIT}$ Low to indicate that a frame error has occurred and configuration is aborted.

To reconfigure the device, the $\overline{PROGRAM}$ pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See "Clearing Configuration Memory".

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.
2. The release of the Global Three State net. This activates I/Os to which signals are assigned. The remaining I/Os stay in a high-impedance state with internal weak pull-down resistors present.
3. Negates Global Set Reset (GSR). This allows all flip-flops to change state.
4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

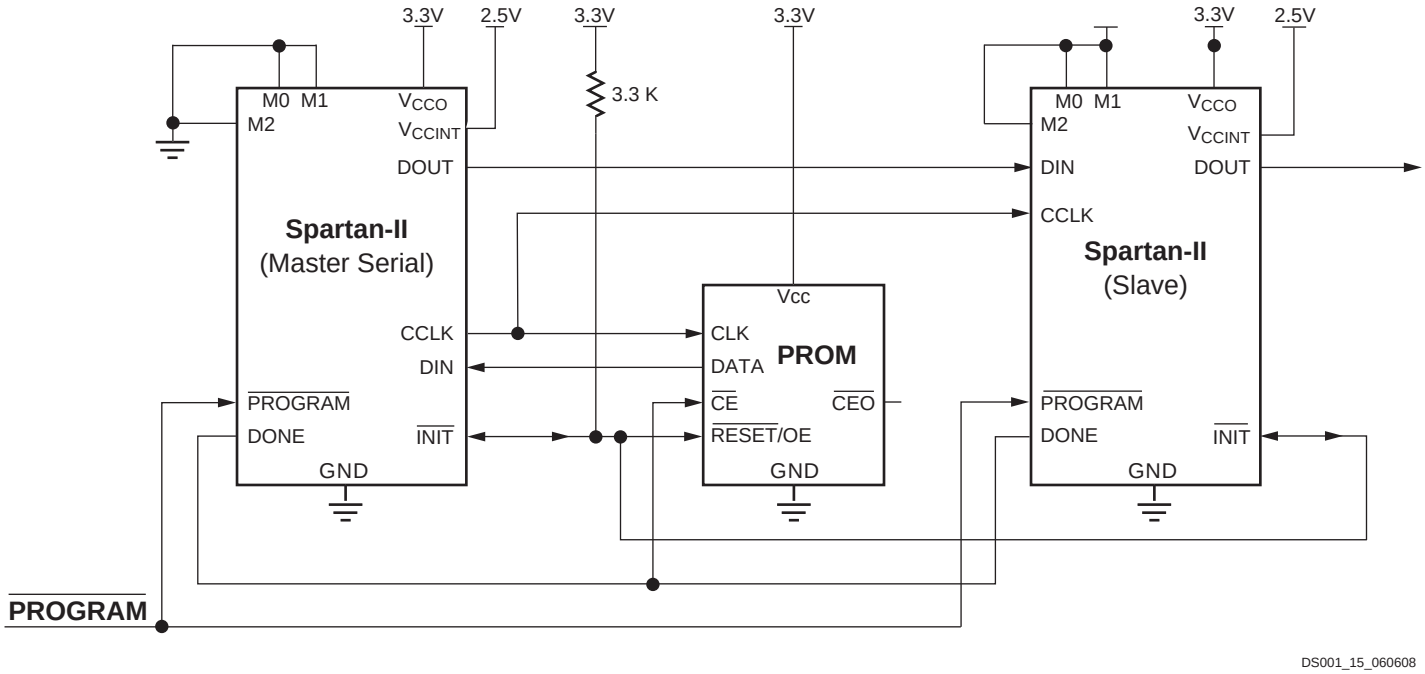
Slave Serial Mode

In Slave Serial mode, the FPGA's CCLK pin is driven by an external source, allowing FPGAs to be configured from other logic devices such as microprocessors or in a daisy-chain configuration. Figure 15 shows connections for a Master Serial FPGA configuring a Slave Serial FPGA from a PROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Slave Serial mode is selected by a <11x> on the mode pins (M0, M1, M2).

Figure 16 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs in Slave Serial mode can be daisy-chained for configuration from a single source. The maximum amount of data that can be sent to the DOUT pin for a serial daisy chain is 2^{20}-1 (1,048,575) 32-bit words, or 33,554,400 bits, which is approximately 25 XC2S200 bitstreams. The configuration bitstream of downstream devices is limited to this size.

After an FPGA is configured, data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High. For more information, see "Start-up," page 19.



Notes:
1. If the DriveDone configuration option is not active for any of the FPGAs, pull up DONE with a 330Ω resistor.

Figure 15: **Master/Slave Serial Configuration Circuit Diagram**

Design Considerations

This section contains more detailed design information on the following features:

Using Delay-Locked Loops

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

Introduction

Quality on-chip clock distribution is important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Primitives

Figure 22 shows the simplified Xilinx library DLL macro, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These primitives provide access to the complete set of DLL features when implementing more complex applications.

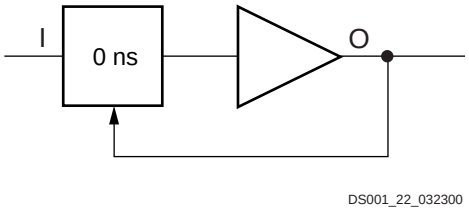


Figure 22: **Simplified DLL Macro BUFGDLL**

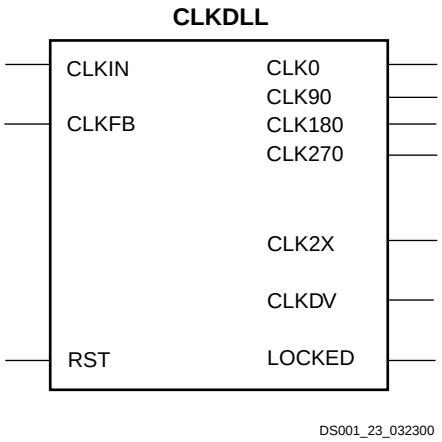


Figure 23: **Standard DLL Primitive CLKDLL**

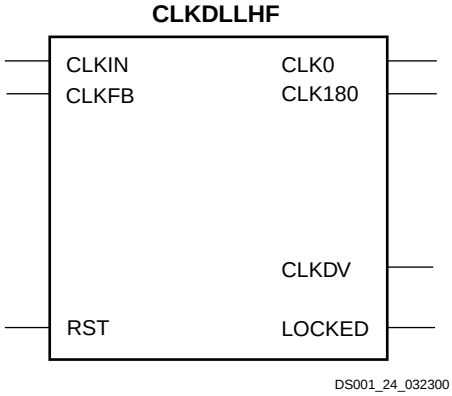


Figure 24: **High-Frequency DLL Primitive CLKDLLHF**

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 25.

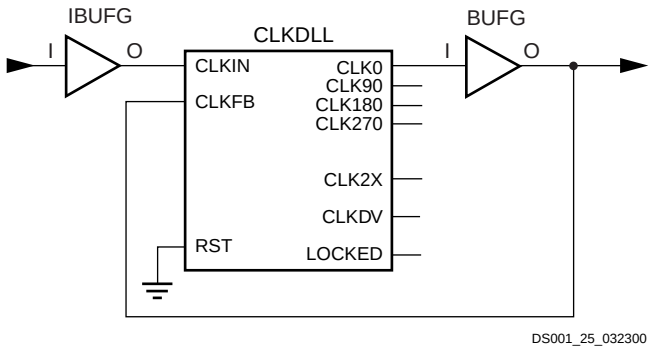


Figure 25: **BUFGDLL Block Diagram**

This macro does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This macro also does not provide access to the RST or LOCKED pins of the DLL. For access to these features, a designer must use the DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG primitive, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50/50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. Either a global clock buffer (BUFG) or one of the global clock input buffers (IBUFG) on the same edge of the device (top or bottom) must source this clock signal.

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feed back to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software to determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates, the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or be tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer deskew with respect to one another. The DLL must be reset when the input clock frequency changes, if the device is reconfigured in Boundary-Scan mode, if the device undergoes a hot swap, and after the device is configured if the input clock is not stable during the startup sequence.

2x Clock Output — CLK2X

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

Clock Divide Output — CLKDV

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction. The CLKDV output pin has a 50/50 duty cycle for all values of the

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

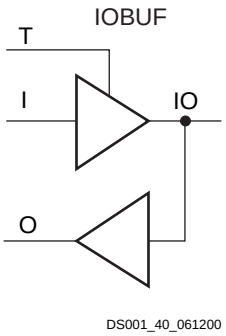


Figure 40: **Input/Output Buffer Primitiveprimitive (IOBUF)**

When the IOBUF primitive supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 36, page 39 for a representation of the Spartan-II FPGA I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate primitive to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

IOB Flip-Flop/Latch Property

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified:

map -pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each Versatile I/O primitive with the location constraint LOC attached to the Versatile I/O primitive. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form:

LOC=A42

LOC=P37

Output Slew Rate Property

In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be programmed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

Output Drive Strength Property

For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE=

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 42. Table 20 lists DC voltage specifications for the GTL standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

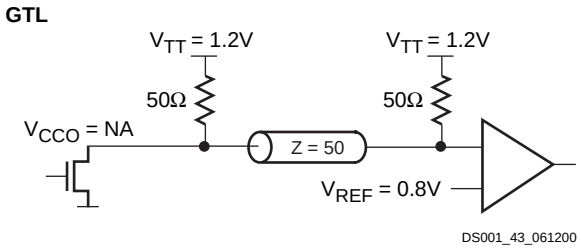


Figure 42: **Terminated GTL**

Table 20: **GTL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}$ (1)	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} \geq V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} \leq V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.4V	32	-	-
I_{OL} at V_{OL} (mA) at 0.2V	-	-	40

Notes:
1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 43. DC voltage specifications appear in Table 21 for the GTL+ standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

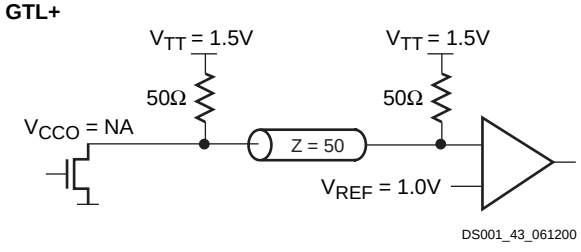


Figure 43: **Terminated GTL+**

Table 21: **GTL+ Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}$ (1)	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} \geq V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} \leq V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL} at V_{OL} (mA) at 0.6V	36	-	-
I_{OL} at V_{OL} (mA) at 0.3V	-	-	48

Notes:
1. N must be greater than or equal to 0.653 and less than or equal to 0.68.

HSTL Class I

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 44. DC voltage specifications appear in Table 22 for the HSTL_1 standard. See "DC Specifications" in Module 3 for the actual FPGA characteristics.

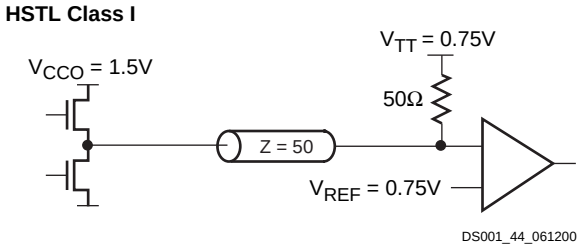


Figure 44: **Terminated HSTL Class I**

Table 22: **HSTL Class I Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	$V_{REF} + 0.1$	-	-
V_{IL}	-	-	$V_{REF} - 0.1$
V_{OH}	$V_{CCO} - 0.4$	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Revision History

Date	Version	Description
09/18/00	2.0	Sectioned the Spartan-II Family data sheet into four modules. Corrected banking description.
03/05/01	2.1	Clarified guidelines for applying power to V_{CCINT} and V_{CCO}
09/03/03	2.2	The following changes were made: • "Serial Modes," page 20 cautions about toggling $\overline{WRITE}$ during serial configuration. • Maximum V_{IH} values in Table 32 and Table 33 changed to 5.5V. • In "Boundary Scan," page 13, removed sentence about lack of INTEST support. • In Table 9, page 17, added note about the state of I/Os after power-on. • In "Slave Parallel Mode," page 23, explained configuration bit alignment to SelectMap port.
06/13/08	2.8	Added note that TDI, TMS, and TCK have a default pull-up resistor. Added note on maximum daisy chain limit. Updated Figure 15 and Figure 18 since Mode pins can be pulled up to either 2.5V or 3.3V. Updated DLL section. Recommended using property or attribute instead of primitive to define I/O properties. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, Min	V, Max	V, Min	V, Max	V, Max	V, Min	mA	mA
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note (2)	Note (2)

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.

Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, *with* DLL (Pin-to-Pin)(1)

Symbol	Description	Device	Speed Grade			Units
			All	-6	-5	
			Min	Max	Max	
$T_{ICKOFDLL}$	Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *with* DLL.	All		2.9	3.3	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. DLL output jitter is already included in the timing calculation.
4. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

Global Clock Input to Output Delay for LVTTL, *without* DLL (Pin-to-Pin)(1)

Symbol	Description	Device	Speed Grade			Units
			All	-6	-5	
			Min	Max	Max	
T_{ICKOF}	Global clock input to output delay using output flip-flop for LVTTL, 12 mA, fast slew rate, *without* DLL.	XC2S15		4.5	5.4	ns
		XC2S30		4.5	5.4	ns
		XC2S50		4.5	5.4	ns
		XC2S100		4.6	5.5	ns
		XC2S150		4.6	5.5	ns
		XC2S200		4.7	5.6	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. The 35 pF load does not apply to the Min values. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.
3. For data *output* with different standards, adjust delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59. For a global clock input with standards other than LVTTL, adjust delays with values from the "I/O Standard Global Clock Input Adjustments," page 61.

IOB Input Switching Characteristics(1)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Delay Adjustments for Different Standards," page 57.

Symbol	Description	Device	Speed Grade				Units
			-6		-5		
			Min	Max	Min	Max	
Propagation Delays							
T_{IOPI}	Pad to I output, no delay	All	-	0.8	-	1.0	ns
T_{IOPID}	Pad to I output, with delay	All	-	1.5	-	1.8	ns
T_{IOPLI}	Pad to output IQ via transparent latch, no delay	All	-	1.7	-	2.0	ns
T_{IOPLID}	Pad to output IQ via transparent latch, with delay	XC2S15	-	3.8	-	4.5	ns
		XC2S30	-	3.8	-	4.5	ns
		XC2S50	-	3.8	-	4.5	ns
		XC2S100	-	3.8	-	4.5	ns
		XC2S150	-	4.0	-	4.7	ns
		XC2S200	-	4.0	-	4.7	ns
Sequential Delays							
T_{IOCKIQ}	Clock CLK to output IQ	All	-	0.7	-	0.8	ns
Setup/Hold Times with Respect to Clock CLK(2)							
T_{IOPICK} / T_{IOICKP}	Pad, no delay	All	1.7 / 0	-	1.9 / 0	-	ns
$T_{IOPICKD}$ / $T_{IOICKPD}$	Pad, with delay(1)	XC2S15	3.8 / 0	-	4.4 / 0	-	ns
		XC2S30	3.8 / 0	-	4.4 / 0	-	ns
		XC2S50	3.8 / 0	-	4.4 / 0	-	ns
		XC2S100	3.8 / 0	-	4.4 / 0	-	ns
		XC2S150	3.9 / 0	-	4.6 / 0	-	ns
		XC2S200	3.9 / 0	-	4.6 / 0	-	ns
$T_{IOICECK}$ / $T_{IOCKICE}$	ICE input	All	0.9 / 0.01	-	0.9 / 0.01	-	ns
Set/Reset Delays							
$T_{IOSRCKI}$	SR input (IFF, synchronous)	All	-	1.1	-	1.2	ns
T_{IOSRIQ}	SR input to IQ (asynchronous)	All	-	1.5	-	1.7	ns
T_{GSRQ}	GSR to output IQ	All	-	9.9	-	11.7	ns

Notes:
1. Input timing for LVTTL is measured at 1.4V. For other I/O standards, see the table "Delay Measurement Methodology," page 60.
2. A zero hold time listing indicates no hold time or a negative hold time.

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Delay Adjustments for Different Standards," page 59.

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Propagation Delays						
T_{IOOP}	O input to pad	-	2.9	-	3.4	ns
T_{IOOLP}	O input to pad via transparent latch	-	3.4	-	4.0	ns
3-state Delays						
T_{IOTHZ}	T input to pad high-impedance(1)	-	2.0	-	2.3	ns
T_{IOTON}	T input to valid data on pad	-	3.0	-	3.6	ns
$T_{IOTLPHZ}$	T input to pad high impedance via transparent latch(1)	-	2.5	-	2.9	ns
$T_{IOTLPON}$	T input to valid data on pad via transparent latch	-	3.5	-	4.2	ns
T_{GTS}	GTS to pad high impedance(1)	-	5.0	-	5.9	ns
Sequential Delays						
T_{IOCKP}	Clock CLK to pad	-	2.9	-	3.4	ns
T_{IOCKHZ}	Clock CLK to pad high impedance (synchronous)(1)	-	2.3	-	2.7	ns
T_{IOCKON}	Clock CLK to valid data on pad (synchronous)	-	3.3	-	4.0	ns
Setup/Hold Times with Respect to Clock CLK(2)						
T_{IOOCK} / T_{IOCKO}	O input	1.1 / 0	-	1.3 / 0	-	ns
$T_{IOOCECK}$ / $T_{IOCKOCE}$	OCE input	0.9 / 0.01	-	0.9 / 0.01	-	ns
$T_{IOSRCKO}$ / $T_{IOCKOSR}$	SR input (OFF)	1.2 / 0	-	1.3 / 0	-	ns
T_{IOTCK} / T_{IOCKT}	3-state setup times, T input	0.8 / 0	-	0.9 / 0	-	ns
$T_{IOTCECK}$ / $T_{IOCKTCE}$	3-state setup times, TCE input	1.0 / 0	-	1.0 / 0	-	ns
$T_{IOSRCKT}$ / $T_{IOCKTSR}$	3-state setup times, SR input (TFF)	1.1 / 0	-	1.2 / 0	-	ns
Set/Reset Delays						
T_{IOSRP}	SR input to pad (asynchronous)	-	3.7	-	4.4	ns
T_{IOSRHZ}	SR input to pad high impedance (asynchronous)(1)	-	3.1	-	3.7	ns
T_{IOSRON}	SR input to valid data on pad (asynchronous)	-	4.1	-	4.9	ns
T_{IOGSRQ}	GSR to pad	-	9.9	-	11.7	ns

Notes:
1. Three-state turn-off delays should not be adjusted.
2. A zero hold time listing indicates no hold time or a negative hold time.

IOB Output Delay Adjustments for Different Standards(1)

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown. A delay adjusted in this way constitutes a worst-case limit.

Symbol	Description	Standard	Speed Grade		Units
			-6	-5	
Output Delay Adjustments (Adj)					
T_{OLVTTL_S2}	Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, C_{SL})	LVTTL, Slow, 2 mA	14.2	16.9	ns
T_{OLVTTL_S4}		4 mA	7.2	8.6	ns
T_{OLVTTL_S6}		6 mA	4.7	5.5	ns
T_{OLVTTL_S8}		8 mA	2.9	3.5	ns
T_{OLVTTL_S12}		12 mA	1.9	2.2	ns
T_{OLVTTL_S16}		16 mA	1.7	2.0	ns
T_{OLVTTL_S24}		24 mA	1.3	1.5	ns
T_{OLVTTL_F2}		LVTTL, Fast, 2 mA	12.6	15.0	ns
T_{OLVTTL_F4}		4 mA	5.1	6.1	ns
T_{OLVTTL_F6}		6 mA	3.0	3.6	ns
T_{OLVTTL_F8}		8 mA	1.0	1.2	ns
T_{OLVTTL_F12}		12 mA	0	0	ns
T_{OLVTTL_F16}		16 mA	–0.1	–0.1	ns
T_{OLVTTL_F24}		24 mA	–0.1	–0.2	ns
$T_{OLVCMOS2}$		LVCMOS2	0.2	0.2	ns
T_{OPCI33_3}		PCI, 33 MHz, 3.3V	2.4	2.9	ns
T_{OPCI33_5}		PCI, 33 MHz, 5.0V	2.9	3.5	ns
T_{OPCI66_3}		PCI, 66 MHz, 3.3V	–0.3	–0.4	ns
T_{OGTL}		GTL	0.6	0.7	ns
T_{OGTLP}		GTL+	0.9	1.1	ns
T_{OHSTL_I}		HSTL I	–0.4	–0.5	ns
T_{OHSTL_III}		HSTL III	–0.8	–1.0	ns
T_{OHSTL_IV}		HSTL IV	–0.9	–1.1	ns
T_{OSSTL2_I}		SSTL2 I	–0.4	–0.5	ns
T_{OSSLT2_II}		SSTL2 II	–0.8	–1.0	ns
T_{OSSTL3_I}		SSTL3 I	–0.4	–0.5	ns
T_{OSSTL3_II}		SSTL3 II	–0.9	–1.1	ns
T_{OCTT}		CTT	–0.5	–0.6	ns
T_{OAGP}		AGP	–0.8	–1.0	ns

Notes:

1. Output timing is measured at 1.4V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see the tables "Constants for Calculating TIOOP" and "Delay Measurement Methodology," page 60.

CLB Distributed RAM Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Sequential Delays						
$T_{SHCKO16}$	Clock CLK to X/Y outputs (WE active, 16 x 1 mode)	-	2.2	-	2.6	ns
$T_{SHCKO32}$	Clock CLK to X/Y outputs (WE active, 32 x 1 mode)	-	2.5	-	3.0	ns
Setup/Hold Times with Respect to Clock CLK(1)						
T_{AS} / T_{AH}	F/G address inputs	0.7 / 0	-	0.7 / 0	-	ns
T_{DS} / T_{DH}	BX/BY data inputs (DIN)	0.8 / 0	-	0.9 / 0	-	ns
T_{WS} / T_{WH}	CE input (WS)	0.9 / 0	-	1.0 / 0	-	ns
Clock CLK						
T_{WPH}	Minimum pulse width, High	-	2.9	-	2.9	ns
T_{WPL}	Minimum pulse width, Low	-	2.9	-	2.9	ns
T_{WC}	Minimum clock period to meet address write cycle time	-	5.8	-	5.8	ns

Notes:
1. A zero hold time listing indicates no hold time or a negative hold time.

CLB Shift Register Switching Characteristics

Symbol	Description	Speed Grade				Units
		-6		-5		
		Min	Max	Min	Max	
Sequential Delays						
T_{REG}	Clock CLK to X/Y outputs	-	3.47	-	3.88	ns
Setup Times with Respect to Clock CLK						
T_{SHDICK}	BX/BY data inputs (DIN)	0.8	-	0.9	-	ns
T_{SHCECK}	CE input (WS)	0.9	-	1.0	-	ns
Clock CLK						
T_{SRPH}	Minimum pulse width, High	-	2.9	-	2.9	ns
T_{SRPL}	Minimum pulse width, Low	-	2.9	-	2.9	ns

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
V_{CCINT}	-	-	P38	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	6	-	P39	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	P119	P40	GND*	GND*	-
I/O	6	P118	P41	K4	T1	314
I/O, V_{REF}	6	P117	P42	M1	R4	317
I/O	6	-	-	-	T2	320
I/O	6	P116	P43	L4	U1	323
I/O	6	-	-	M2	R5	326
I/O	6	-	P44	L3	U2	332
I/O, V_{REF}	6	P115	P45	N1	T3	335
V_{CCO}	6	-	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	-	-	GND*	GND*	-
I/O	6	-	P46	P1	T4	338
I/O	6	-	-	L5	W1	341
I/O	6	-	-	-	U4	344
I/O	6	P114	P47	N2	Y1	347
I/O	6	-	-	M4	W2	350
I/O	6	P113	P48	R1	Y2	356
I/O	6	P112	P49	M3	W3	359
M1	-	P111	P50	P2	U5	362
GND	-	P110	P51	GND*	GND*	-
M0	-	P109	P52	N3	AB2	363
V_{CCO}	6	P108	P53	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
V_{CCO}	5	P107	P53	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
M2	-	P106	P54	R3	Y4	364
I/O	5	-	-	N5	V7	374
I/O	5	P103	P57	T2	Y6	377
I/O	5	-	-	-	AA4	380
I/O	5	-	-	P5	W6	383
I/O	5	-	P58	T3	Y7	386
GND	-	-	-	GND*	GND*	-
V_{CCO}	5	-	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P102	P59	T4	AA5	389
I/O	5	-	P60	M6	AB5	392
I/O	5	-	-	T5	AB6	398
I/O	5	P101	P61	N6	AA7	401
I/O	5	-	-	-	W7	404

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
I/O, V_{REF}	5	P100	P62	R5	W8	407
I/O	5	P99	P63	P6	Y8	410
GND	-	P98	P64	GND*	GND*	-
V_{CCO}	5	-	P65	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCINT}	-	P97	P66	V_{CCINT}*	V_{CCINT}*	-
I/O	5	P96	P67	R6	AA8	413
I/O	5	P95	P68	M7	V9	416
I/O	5	-	-	-	AB9	419
I/O	5	-	P69	N7	Y9	422
I/O	5	-	P70	T6	W10	428
I/O	5	-	P71	P7	AB10	431
GND	-	-	P72	GND*	GND*	-
I/O, V_{REF}	5	P94	P73	P8	Y10	434
I/O	5	-	P74	R7	V11	437
I/O	5	-	-	T7	W11	440
I/O	5	P93	P75	T8	AB11	443
V_{CCINT}	-	P92	P76	V_{CCINT}*	V_{CCINT}*	-
I, GCK1	5	P91	P77	R8	Y11	455
V_{CCO}	5	P90	P78	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCO}	4	P90	P78	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P89	P79	GND*	GND*	-
I, GCK0	4	P88	P80	N8	W12	456
I/O	4	P87	P81	N9	U12	460
I/O	4	P86	P82	R9	Y12	466
I/O	4	-	-	N10	AA12	469
I/O	4	-	P83	T9	AB13	472
I/O, V_{REF}	4	P85	P84	P9	AA13	475
GND	-	-	P85	GND*	GND*	-
I/O	4	-	P86	M10	Y13	478
I/O	4	-	P87	R10	V13	481
I/O	4	-	P88	P10	AA14	487
I/O	4	-	-	-	V14	490
I/O	4	P84	P89	T10	AB15	493
I/O	4	P83	P90	R11	AA15	496
V_{CCINT}	-	P82	P91	V_{CCINT}*	V_{CCINT}*	-
V_{CCO}	4	-	P92	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P81	P93	GND*	GND*	-
I/O	4	P80	P94	M11	Y15	499

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
I/O	2	-	-	F12	G20	695
I/O	2	-	P149	E15	F19	701
I/O, V_{REF}	2	P41	P150	F13	F21	704
V_{CCO}	2	-	-	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
GND	-	-	-	GND*	GND*	-
I/O	2	-	P151	E14	F20	707
I/O	2	-	-	C16	F18	710
I/O	2	-	-	-	E21	713
I/O	2	P40	P152	E13	D22	716
I/O	2	-	-	B16	E20	719
I/O (DIN, D0)	2	P39	P153	D14	D20	725
I/O (DOUT, BUSY)	2	P38	P154	C15	C21	728
CCLK	2	P37	P155	D15	B22	731
V_{CCO}	2	P36	P156	V_{CCO} Bank 2*	V_{CCO} Bank 2*	-
V_{CCO}	1	P35	P156	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
TDO	2	P34	P157	B14	A21	-
GND	-	P33	P158	GND*	GND*	-
TDI	-	P32	P159	A15	B20	-
I/O ($\overline{CS}$)	1	P31	P160	B13	C19	0
I/O ($\overline{WRITE}$)	1	P30	P161	C13	A20	3
I/O	1	-	-	C12	D17	9
I/O	1	P29	P162	A14	A19	12
I/O	1	-	-	-	B18	15
I/O	1	-	-	D12	C17	18
I/O	1	-	P163	B12	D16	21
GND	-	-	-	GND*	GND*	-
V_{CCO}	1	-	-	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
I/O, V_{REF}	1	P28	P164	C11	A18	24
I/O	1	-	P165	A13	B17	27
I/O	1	-	-	D11	D15	33
I/O	1	-	P166	A12	C16	36
I/O	1	-	-	-	D14	39
I/O, V_{REF}	1	P27	P167	E11	E14	42
I/O	1	P26	P168	B11	A16	45
GND	-	P25	P169	GND*	GND*	-

XC2S100 Device Pinouts *(Continued)*

XC2S100 Pad Name		TQ144	PQ208	FG256	FG456	Bndry Scan
Function	Bank					
V_{CCO}	1	-	P170	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
V_{CCINT}	-	P24	P171	V_{CCINT}*	V_{CCINT}*	-
I/O	1	P23	P172	A11	C15	48
I/O	1	P22	P173	C10	B15	51
I/O	1	-	-	-	F12	54
I/O	1	-	P174	B10	C14	57
I/O	1	-	P175	D10	D13	63
I/O	1	-	P176	A10	C13	66
GND	-	-	P177	GND*	GND*	-
I/O, V_{REF}	1	P21	P178	B9	B13	69
I/O	1	-	P179	E10	E12	72
I/O	1	-	-	A9	B12	75
I/O	1	P20	P180	D9	D12	78
I/O	1	P19	P181	A8	D11	84
I, GCK2	1	P18	P182	C9	A11	90
GND	-	P17	P183	GND*	GND*	-
V_{CCO}	1	P16	P184	V_{CCO} Bank 1*	V_{CCO} Bank 1*	-
V_{CCO}	0	P16	P184	V_{CCO} Bank 0*	V_{CCO} Bank 0*	-
I, GCK3	0	P15	P185	B8	C11	91
V_{CCINT}	-	P14	P186	V_{CCINT}*	V_{CCINT}*	-
I/O	0	P13	P187	A7	A10	101
I/O	0	-	-	D8	B10	104

Additional XC2S100 Package Pins

TQ144

Not Connected Pins					
P104	P105	-	-	-	-

11/02/00

PQ208

Not Connected Pins					
P55	P56	-	-	-	-

11/02/00

FG256

V_{CCINT} Pins					
C3	C14	D4	D13	E5	E12
M5	M12	N4	N13	P3	P14
V_{CCO} Bank 0 Pins					
E8	F8	-	-	-	-
V_{CCO} Bank 1 Pins					
E9	F9	-	-	-	-
V_{CCO} Bank 2 Pins					
H11	H12	-	-	-	-
V_{CCO} Bank 3 Pins					
J11	J12	-	-	-	-
V_{CCO} Bank 4 Pins					
L9	M9	-	-	-	-
V_{CCO} Bank 5 Pins					
L8	M8	-	-	-	-
V_{CCO} Bank 6 Pins					
J5	J6	-	-	-	-
V_{CCO} Bank 7 Pins					
H5	H6	-	-	-	-
GND Pins					
A1	A16	B2	B15	F6	F7
F10	F11	G6	G7	G8	G9
G10	G11	H7	H8	H9	H10
J7	J8	J9	J10	K6	K7
K8	K9	K10	K11	L6	L7
L10	L11	R2	R15	T1	T16
Not Connected Pins					
P4	R4	-	-	-	-

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V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					

Additional XC2S100 Package Pins *(Continued)*

F10	F7	F8	F9	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U10	U7	U8	U9
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					
G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A4	A5	A6	A12	A13
A14	A15	A17	B3	B6	B8
B11	B14	B16	B19	C1	C2
C8	C9	C12	C18	C22	D1
D4	D5	D10	D18	D19	D21
E4	E11	E13	E15	E16	E17
E19	E22	F4	F11	F22	G2
G3	G4	G19	G22	H1	H21
J1	J3	J4	J19	J20	K2
K18	K19	L2	L5	L18	L19
M2	M6	M17	M18	M21	N1
N5	N19	P1	P5	P19	P22
R1	R3	R20	R22	T5	T19
U3	U11	U18	V1	V2	V10
V12	V17	V3	V4	V6	V8
V20	V21	V22	W4	W5	W9
W13	W14	W15	W16	W19	Y5
Y14	Y18	Y22	AA1	AA3	AA6
AA9	AA10	AA11	AA16	AA17	AA18
AA22	AB3	AB4	AB7	AB8	AB12
AB14	AB21	-	-	-	-

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XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
I/O	6	-	-	T2	449
I/O	6	P43	L4	U1	452
GND	-	-	GND*	GND*	-
I/O	6	-	M2	R5	455
I/O	6	-	-	V1	458
I/O	6	-	-	T5	461
I/O	6	P44	L3	U2	464
I/O, V_{REF}	6	P45	N1	T3	467
V_{CCO}	6	-	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
GND	-	-	GND*	GND*	-
I/O	6	P46	P1	T4	470
I/O	6	-	L5	W1	473
GND	-	-	GND*	GND*	-
I/O	6	-	-	V2	476
I/O	6	-	-	U4	482
I/O, V_{REF}	6	P47	N2	Y1	485
GND	-	-	GND*	GND*	-
I/O	6	-	M4	W2	488
I/O	6	-	-	V3	491
I/O	6	-	-	V4	494
I/O	6	P48	R1	Y2	500
I/O	6	P49	M3	W3	503
M1	-	P50	P2	U5	506
GND	-	P51	GND*	GND*	-
M0	-	P52	N3	AB2	507
V_{CCO}	6	P53	V_{CCO} Bank 6*	V_{CCO} Bank 6*	-
V_{CCO}	5	P53	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
M2	-	P54	R3	Y4	508
I/O	5	-	-	W5	518
I/O	5	-	-	AB3	521
I/O	5	-	N5	V7	524
GND	-	-	GND*	GND*	-
I/O, V_{REF}	5	P57	T2	Y6	527
I/O	5	-	-	AA4	530
I/O	5	-	-	AB4	536
I/O	5	-	P5	W6	539
I/O	5	P58	T3	Y7	542
GND	-	-	GND*	GND*	-

XC2S200 Device Pinouts *(Continued)*

XC2S200 Pad Name		PQ208	FG256	FG456	Bndry Scan
Function	Bank				
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P59	T4	AA5	545
I/O	5	P60	M6	AB5	548
I/O	5	-	-	V8	551
I/O	5	-	-	AA6	554
I/O	5	-	T5	AB6	557
GND	-	-	GND*	GND*	-
I/O	5	P61	N6	AA7	560
I/O	5	-	-	W7	563
I/O, V_{REF}	5	P62	R5	W8	569
I/O	5	P63	P6	Y8	572
GND	-	P64	GND*	GND*	-
V_{CCO}	5	P65	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCINT}	-	P66	V_{CCINT}*	V_{CCINT}*	-
I/O	5	P67	R6	AA8	575
I/O	5	P68	M7	V9	578
I/O	5	-	-	AB8	581
I/O	5	-	-	W9	584
I/O	5	-	-	AB9	587
GND	-	-	GND*	GND*	-
I/O	5	P69	N7	Y9	590
I/O	5	-	-	V10	593
I/O	5	-	-	AA9	596
I/O	5	P70	T6	W10	599
I/O	5	P71	P7	AB10	602
GND	-	P72	GND*	GND*	-
V_{CCO}	5	-	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
I/O, V_{REF}	5	P73	P8	Y10	605
I/O	5	P74	R7	V11	608
I/O	5	-	-	AA10	614
I/O	5	-	T7	W11	617
I/O	5	P75	T8	AB11	620
I/O	5	-	-	U11	623
V_{CCINT}	-	P76	V_{CCINT}*	V_{CCINT}*	-
I, GCK1	5	P77	R8	Y11	635
V_{CCO}	5	P78	V_{CCO} Bank 5*	V_{CCO} Bank 5*	-
V_{CCO}	4	P78	V_{CCO} Bank 4*	V_{CCO} Bank 4*	-
GND	-	P79	GND*	GND*	-

Additional XC2S200 Package Pins *(Continued)*

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V_{CCINT} Pins					
E5	E18	F6	F17	G7	G8
G9	G14	G15	G16	H7	H16
J7	J16	P7	P16	R7	R16
T7	T8	T9	T14	T15	T16
U6	U17	V5	V18	-	-
V_{CCO} Bank 0 Pins					
F7	F8	F9	F10	G10	G11
V_{CCO} Bank 1 Pins					
F13	F14	F15	F16	G12	G13
V_{CCO} Bank 2 Pins					
G17	H17	J17	K16	K17	L16
V_{CCO} Bank 3 Pins					
M16	N16	N17	P17	R17	T17
V_{CCO} Bank 4 Pins					
T12	T13	U13	U14	U15	U16
V_{CCO} Bank 5 Pins					
T10	T11	U7	U8	U9	U10
V_{CCO} Bank 6 Pins					
M7	N6	N7	P6	R6	T6
V_{CCO} Bank 7 Pins					

Additional XC2S200 Package Pins *(Continued)*

G6	H6	J6	K6	K7	L7
GND Pins					
A1	A22	B2	B21	C3	C20
J9	J10	J11	J12	J13	J14
K9	K10	K11	K12	K13	K14
L9	L10	L11	L12	L13	L14
M9	M10	M11	M12	M13	M14
N9	N10	N11	N12	N13	N14
P9	P10	P11	P12	P13	P14
Y3	Y20	AA2	AA21	AB1	AB22
Not Connected Pins					
A2	A6	A12	B11	B16	C2
D1	D4	D18	D19	E17	E19
G2	G22	L2	L19	M2	M21
R3	R20	U3	U18	V6	W4
W19	Y5	Y22	AA1	AA3	AA11
AA16	AB7	AB12	AB21	-	-

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Revision History

Version No.	Date	Description
2.0	09/18/00	Sectioned the Spartan-II Family data sheet into four modules. Corrected all known errors in the pinout tables.
2.1	10/04/00	Added notes requiring $\overline{PWDN}$ to be tied to V_{CCINT} when unused.
2.2	11/02/00	Removed the Power Down feature.
2.3	03/05/01	Added notes on pinout tables for IRDY and TRDY.
2.4	04/30/01	Reinstated XC2S50 V_{CCO} Bank 7, GND, and "not connected" pins missing in version 2.3.
2.5	09/03/03	Added caution about Not Connected Pins to XC2S30 pinout tables on page 76.
2.8	06/13/08	Added "Package Overview" section. Added notes to clarify shared V_{CCO} banks. Updated description and links. Updated all modules for continuous page, figure, and table numbering. Synchronized all modules to v2.8.